REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
E	Change to vendor similar part number for vendor CAGE number 61772 for devices 08KX, 09KX, 10KX, 11KX, 12KX, 13KX, 14KX, 15KX, and 16KX. Remove vendor CAGE number 61772 from devices 08YX, 09YX, 10YX, 11YX, 12YX, 13YX, 15YX, and 16YX. Change to vendor similar part number for vendor CAGE number 65786 for devices 09 and 11. Add vendor CAGE number 50088 to the drawing as a source of supply for devices 04JX and 05JX. Add vendor CAGE number 65896 to the drawing as a source of supply for devices 15 and 16. Removed 4.3.3 from drawing. Editorial changes thoughout.	92-04-27	M. A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																			
SHEET																			
REV	E	E	E	E	E	E	E	E	E	E	E								
SHEET	14	15	16	17	18	19	20	21	22	23	24								

REV STATUS OF SHEETS	REV	E	E	E	E	D	E	E	E	E	E	E	E
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
James E. Jamison

CHECKED BY
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APPROVED BY
Don Cool

DRAWING APPROVAL DATE
84-08-23

REVISION LEVEL E

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 16K (2048 X 8) BIT STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	84036

SHEET 1 OF 24

DESC FORM 193-1
JUL 91

5962-E262

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-Jan devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

84036	01	J	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Supply voltage variation	Address access time
01		10%	200 ns (synchronous)
02		10%	90 ns
03		10%	90 ns
04		10%	150 ns
05		10%	200 ns
06		10%	70 ns
07		10%	120 ns (synchronous)
08		10%	45 ns
09		10%	45 ns
10		10%	55 ns
11		10%	55 ns
12		10%	70 ns
13		10%	70 ns
14		10%	35 ns
15		10%	120 ns
16		10%	90 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-lead, 1.290" x .610" x .225"), dual-in-line package
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
X	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier package
Y	Figure 1, (24-lead, .308" x .408"), rectangular chip carrier package
Z	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier package with castellated instead of chamfered corners and extended pad metallization at terminal number 1.
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1/ Generic numbers are listed on the standardized military drawing source approval bulletin at the end of this document and will also be listed in MIL-BUL-103.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.3 V dc to +7.0 V dc 2/
Temperature under bias	-55°C to +125°C
Storage temperature range	-55°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 5 seconds)	+275°C
Thermal resistance, junction-to-case (Θ_{JC}):	See MIL-M-38510, appendix C
Case Y	30°C/W
Junction temperature (T_J)	+150°C 3/
All input or output voltages with respect to ground	-0.3 V dc to V_{CC} +0.3 V dc 4/

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Input low voltage (V_{IL}):	
Device types 01 through 16	-0.3 V dc to 0.8 V dc 2/
Input high voltage (V_{IH}):	
Device types 01, 07	2.4 V dc to V_{CC} +0.3 V dc 2/
Device types 02 through 06, 08 through 16	2.2 V dc to V_{CC} +0.3 V dc 2/
Supply voltage range (V_{CC}):	4.5 V dc to 5.5 V dc 2/
Minimum chip enable low time	40 ns 5/
Minimum chip enable high time	40 ns 5/
Maximum input rise time	40 ns
Maximum input fall time	40 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2/ All voltages referenced to V_{SS}.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
4/ Negative undershoots to a minimum of -3.0 V are allowed with a maximum of 20 ns pulse width.
5/ For device types 02, 03, and 06 only.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Block diagram. The block diagrams shall be as specified on figure 4.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-M-38510) shall be subjected to and pass the internal moisture content test (method 1018 of MIL-STD-883), the frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	I_{OH} = -1 mA	1, 2, 3	01-07, 15,16	2.4		V
		I_{OH} = -4 mA		08-14			
Low level output voltage	V_{OL}	I_{OL} = 3.2 mA	1, 2, 3	01,07		0.4	V
		I_{OL} = 4.0 mA		02,03, 06,15			
		I_{OL} = 2.0 mA		04,05,16			
		I_{OL} = 8.0 mA		08-14			
High impedance output leakage current	I_{OLZ} I_{OHZ}	$\overline{OE}$ = V_{IH}	1, 2, 3	01,02 06,07	-1.0	1.0	µA
				04,05,09, 11,13,14, 15,16	-10.0	10.0	
				03,08, 10,12	-5.0	5.0	
Input leakage current	I_{IL} I_{IH}	V_{IN} = GND V_{IN} = 5.5 V	1, 2, 3	01,02, 06,07	-1.0	1.0	µA
				04,05,15	-2.0	2.0	
				03,08,10, 12,16	-5.0	5.0	
				09,11, 13,14	-10.0	10.0	
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, f = fmax 3/ $\overline{CE}$ = V_{IL}, outputs open All other inputs at V_{IL}	1, 2, 3	01,07		10	mA
				04,05,13, 15,16		90	
				02,03,06		70	
				08,10,12		85	
				09,11		120	
				14		150	
Standby supply current	I_{CC2}	$\overline{CE}$ = $\overline{WE}$ = V_{IH}, I_O = 0	1, 2, 3	02,03,06		8	mA
				04,05		10	
				10,12, 15,16		15	
				09,11, 13,14		25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Standby supply current	I_{CC3}	$\overline{CE}$ = V_{CC} -0.3 V, I_O = 0	1, 2, 3	06,07		50	µA
				01,02		100	
				04,05		250	
				03,08,10, 12,15,16		900	
				13		10	mA
				09,11,14		20	mA
Data retention supply current	I_{CC4}	$\overline{CE}$ = V_{CC}, V_{CC} = 2.0 V	1, 2, 3	01,02		50	µA
				04,05		100	
				08,10,12, 15,16		200	
				03		300	
				06,07		25	
Input 4/ capacitance	C_I	V_I = V_{CC} or GND, f = 1 MHz See 4.3.1c	4	All		10	pF
Output 4/ capacitance	C_O	V_{IO} = V_{CC} or GND, f = 1 MHz See 4.3.1c	4	All		12	pF
Read/write cycle time	t_{AVAV}	5/ 6/	9,10,11	01	280		ns
				02,03,16	90		
				04	150		
				05	200		
				15	120		
				07	170		
				08,09	45		
				10,11	55		
				06,12,13	70		
				14	35		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Address access time	t_{AVQV}	5/ 6/	9,10,11	01		200	ns
				02,03,16		90	
				04		150	
				05		200	
				07,15		120	
				08,09		45	
				10,11		55	
				06,12,13		70	
				14		35	
Output hold after address change 4/	t_{AVQX}	5/ 6/	9,10,11	15,16	0		ns
				04,05	10		
				02,03,06, 07,08-14	5		
Output enable to output active 4/	t_{OLQX}	5/ 6/	9,10,11	01,07	10		ns
				02,03,06, 08,12,13	5		
				04,05,09, 11,14,15, 16	0		
Output enable access time	t_{OLQV}	5/ 6/	9,10,11	01,07,15		80	ns
				02,03,16		65	
				04		60	
				05		70	
				08,09		25	
				10,11		40	
				06,12,13		50	
				14		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Chip enable to output active 4/	t_{ELQX}	5/ 6/	9,10,11	01,07	10		ns
				02,03,06, 08-14	5		
				04,05, 15,16	0		
Chip enable access time	t_{ELQV}	5/ 6/	9,10,11	01		200	ns
				02,03,16		90	
				04		150	
				05		200	
				07,15		120	
				08,09		45	
				10,11		55	
				06,12,13		70	
				14		35	
Chip enable to output in high Z 4/	t_{EHQZ}	5/ 6/	9,10,11	01		80	ns
				02,03,07, 15,16		50	
				04,05		60	
				08,09		25	
				10,11		30	
				06,12,13		35	
				14		15	
Write recovery time	t_{WHAV}	5/ 6/	9,10,11	02,03,04, 05,06,15, 16	10		ns
				09,11,14	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Chip enable to end-of-write	t_{ELWH}	5/ 6/	9,10,11	01	200		ns
				02,03,16	55		
				04	90		
				05,07	120		
				06	45		
				08,09,14	30		
				10-13	40		
				15	70		
Address valid to end-of-write	t_{AVWH}	5/ 6/	9,10,11	02,03, 12,13	65		ns
				04	100		
				05	130		
				15	105		
				06	50		
				08,09,14	30		
				10,11	45		
				16	80		
Address to $\overline{WE}$ setup time	t_{AVWL}	5/ 6/	9,10,11	02-06, 15,16	10		ns
				07,08,09, 11,14	0		
				10	5		
				12,13	15		
Address to $\overline{CE}$ setup time	t_{AVEL}	5/ 6/	9,10,11	01,07	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output enable to output in high Z 4/	t_{OHQZ}	5/ 6/	9,10,11	01		80	ns
				02,03, 15,16		40	
				04,07		50	
				05		60	
				08,09		25	
				10,11		30	
				06,12,13		35	
				14		15	
Write enable pulse width	t_{WLWH}	5/ 6/	9,10,11	01	200		ns
				02,03,16	55		
				04	90		
				05,07	120		
				15	70		
				08,11	25		
				06,10, 12,13	40		
				09,14	20		
Data setup to end-of-write	t_{DVWH}	5/ 6/	9,10,11	01	80		ns
				02,03,06, 12,13,16	30		
				04,07	50		
				05	70		
				08,09	20		
				10,11	25		
				15	35		
				14	15		

See footnotes at end of table.

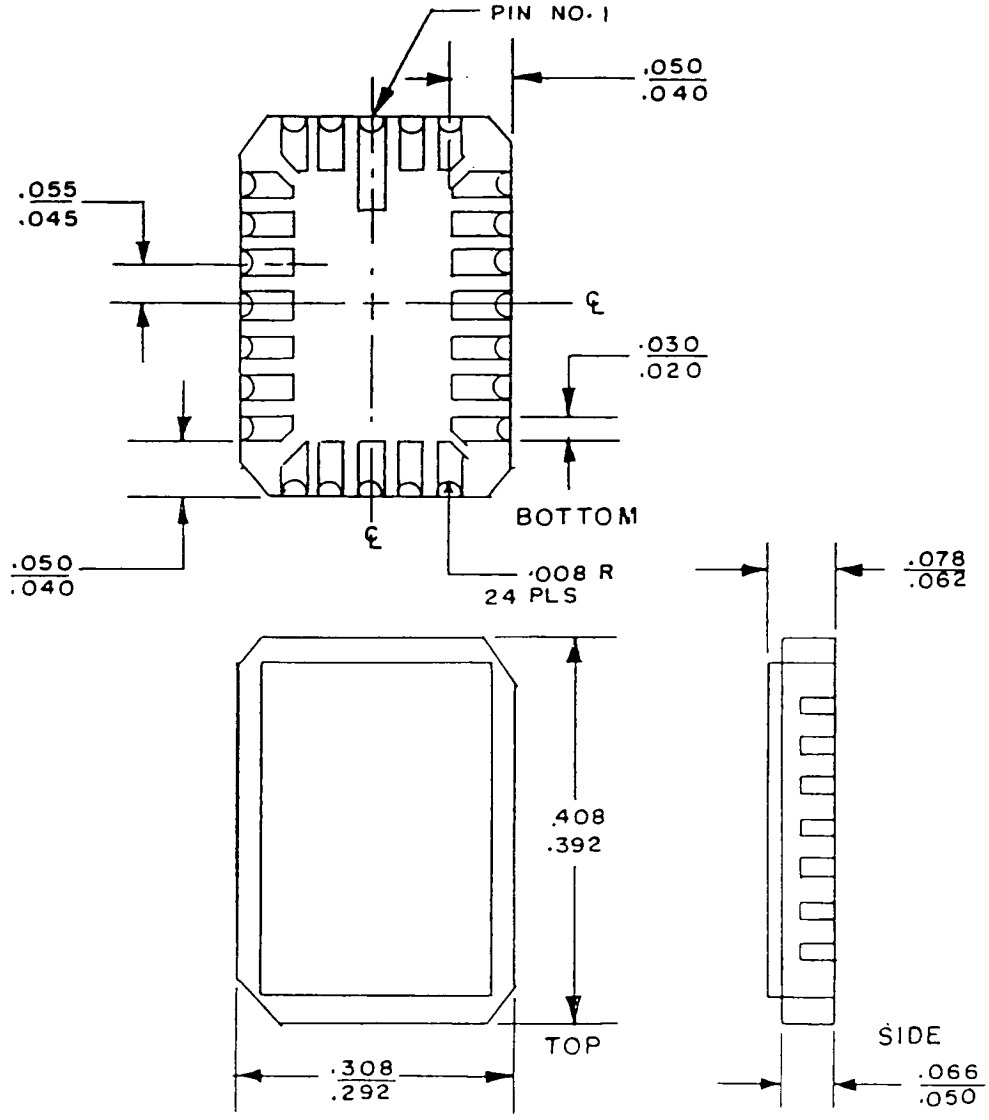
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Data hold after end-of-write	t_{WHDX}	5/ 6/	9,10,11	01,06,07	10		ns
				02,03,04, 05,15,16	15		
				08,09, 11,14	0		
				10,12,13	5		
Minimum chip-enable high time after write	t_{EHEL}	5/ 6/	9,10,11	01	80		ns
				07	50		
Address hold time after CE low	t_{ELAX}	5/ 6/	9,10,11	01	50		ns
				07	30		
Chip-enable pulse width during write	t_{ELEH}	5/ 6/	9,10,11	01	200		ns
				07	120		
Write enable pulse setup time	t_{WLEH}	5/ 6/	9,10,11	01	200		ns
				02,03,16	55		
				04	90		
				05,07	120		
				08	30		
				06,10, 12,13	40		
				09,14	20		
				11	25		
				15	70		

1/ All voltages referenced to V_{SS}.
2/ Negative undershoots to a minimum of -0.3 V are allowed with a maximum of 20 ns pulse width.
3/ fmax = $1/t_{AVAV}$.
4/ Tested initially, and after any design or process change which could affect these parameters.
5/ AC measurements assume transition time ≤ 5 ns and input levels are from V_{SS} to 3.0 V. Output load is specified on figure 5. Reference timing levels are at 1.5 V.
6/ For timing waveforms, see figure 6.

Inches	mm
.008	0.20
.020	0.50
.030	0.76
.040	1.01
.045	1.14
.050	1.27
.055	1.39
.062	1.57
.065	1.67
.078	1.98
.292	7.41
.308	7.82
.392	9.95
.408	10.36

24 PIN RECTANGULAR LEADLESS CHIP CARRIER

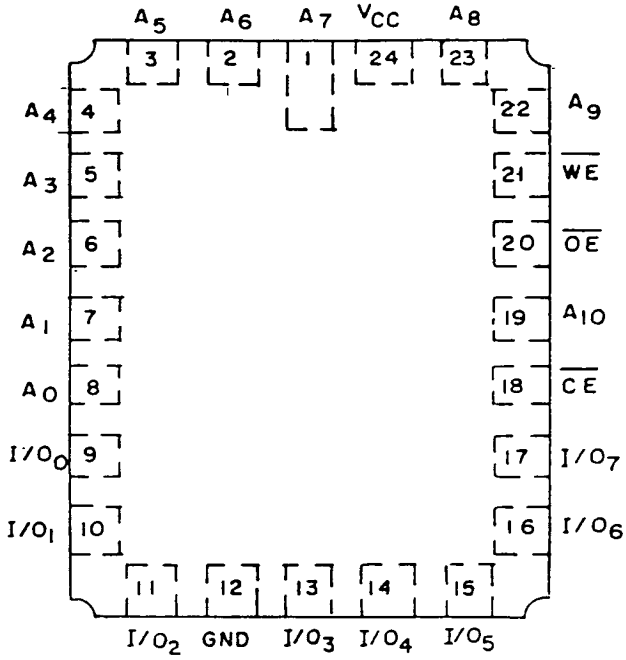


NOTES:
1. Dimensions are in inches.
2. Metric equivalents are for general information only.

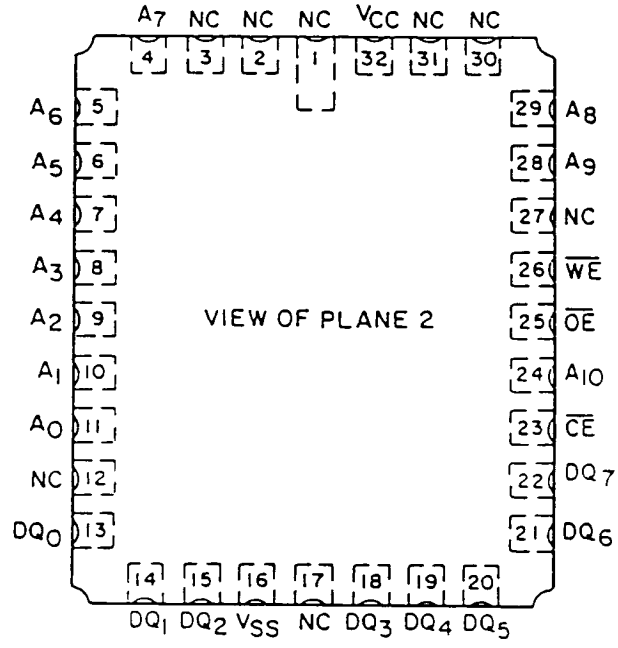
FIGURE 1. Case outline Y (24-lead, .308 x .408", rectangular chip carrier package).

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84036
		REVISION LEVEL E	SHEET 12

Case Y

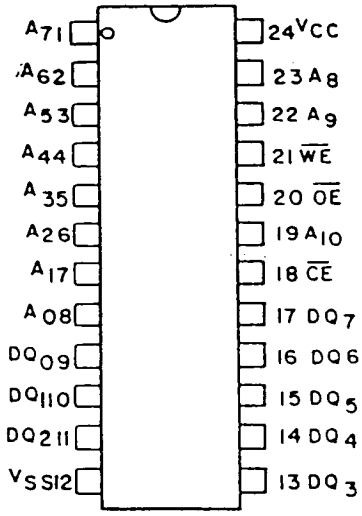


Cases X and Z



Option A with active terminals on plane 1

Cases J, K, and L



Pin names

A_0 - A_{10}	Address inputs
$\overline{CE}/\overline{E}$	Chip enable/power down for O2 - O5
V_{SS}	Ground
DQ_0 - DQ_7 IO_0 - IO_7	Data in/data out
V_{CC}	Power (+.5 V)
$\overline{WE}/\overline{W}$	Write enable
$\overline{OE}/\overline{G}$	Output enable

FIGURE 2. Terminal connections.

Case 3

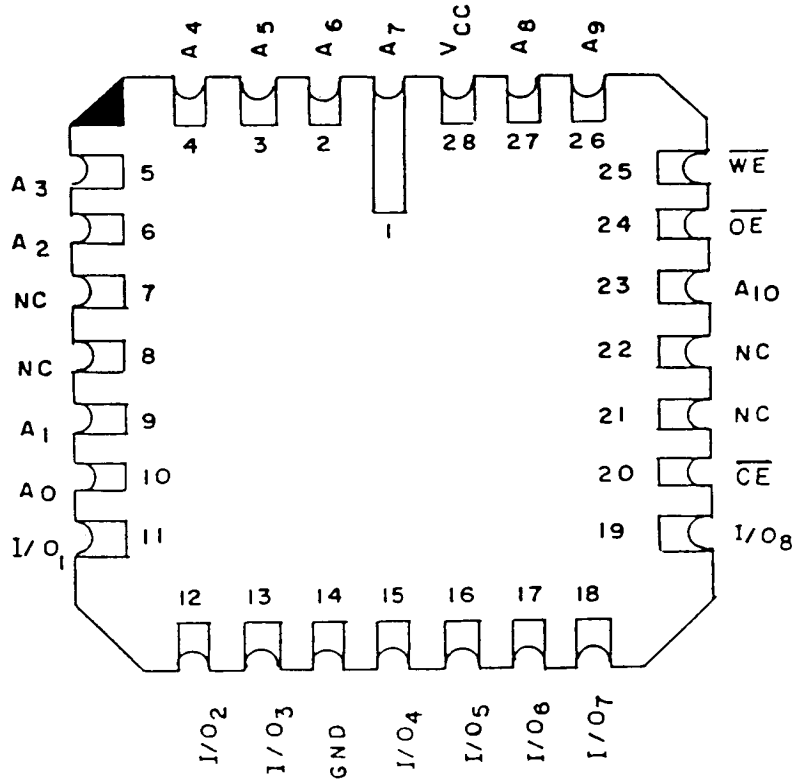


FIGURE 2. Terminal connection. - Continued

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84036
		REVISION LEVEL E	SHEET 14

Device types 01 and 07

Read cycle

Time reference	Inputs					Function
	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	A	DQ	
-1	H	X	X	X	Z	Memory disabled
0	↘	H	X	V	Z	Cycle begins, addresses are latched
1	L	H	L	X	X	Output enabled
2	L	H	L	X	V	Output valid
3	↗	H	X	X	V	Read accomplished
4	H	X	X	X	Z	Prepare for next cycle (same as -1)
5	↘	H	X	V	Z	Cycle ends, next cycle begins (same as 0)

Write cycle

Time reference	Inputs					Function
	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	A	DQ	
-1	H	X	H	X	X	Memory disabled
0	↘	X	H	V	X	Cycle begins, addresses are latched
1	L	L	H	X	X	Write period begins
2	L	↗	H	X	V	Data is written
3	↗	H	H	X	X	Write completed
4	H	X	H	X	X	Prepare for next cycle (same as -1)
5	↘	X	H	V	X	Cycle ends, next cycle begins (same as 0)

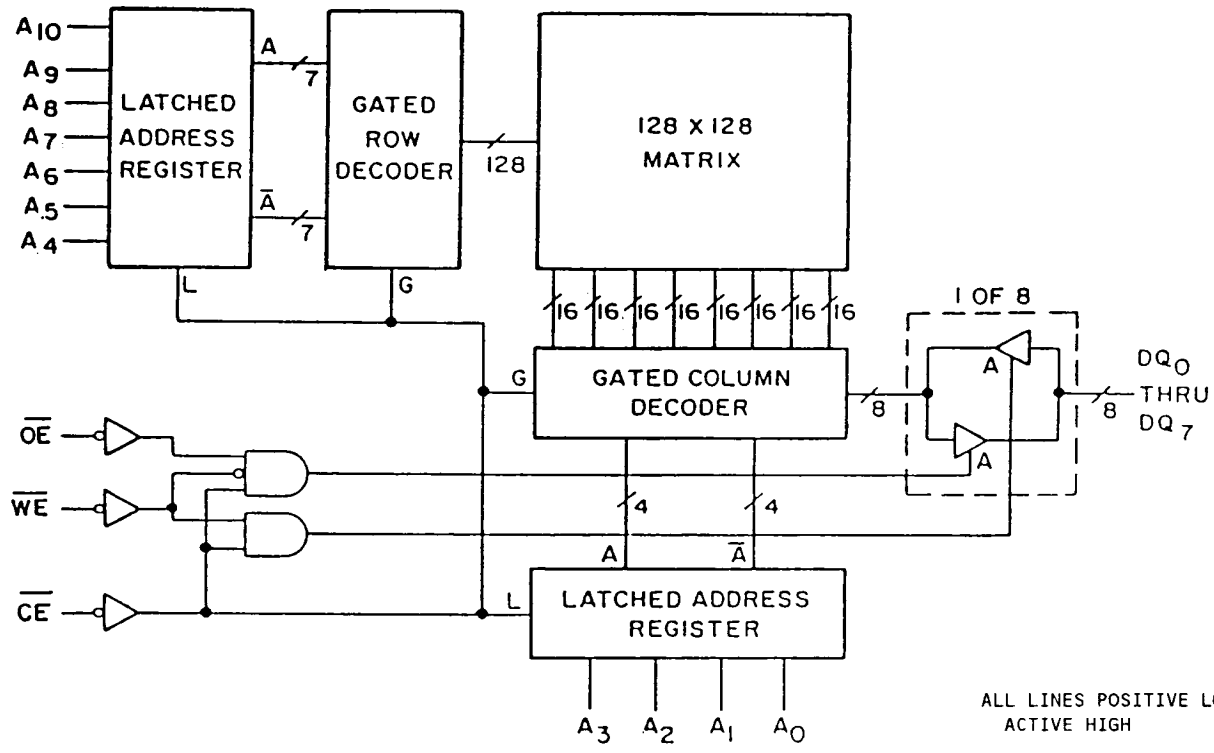
Device types 02 - 06 and 08 - 16

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't care

FIGURE 3. Truth table.

Device types 01 and 07.



ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE-STATE BUFFERS:
A HIGH - OUTPUT ACTIVE

ADDRESS LATCHED AND GATED

DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

FIGURE 4. Block diagram.

Device types 02 - 06 and 08 - 16

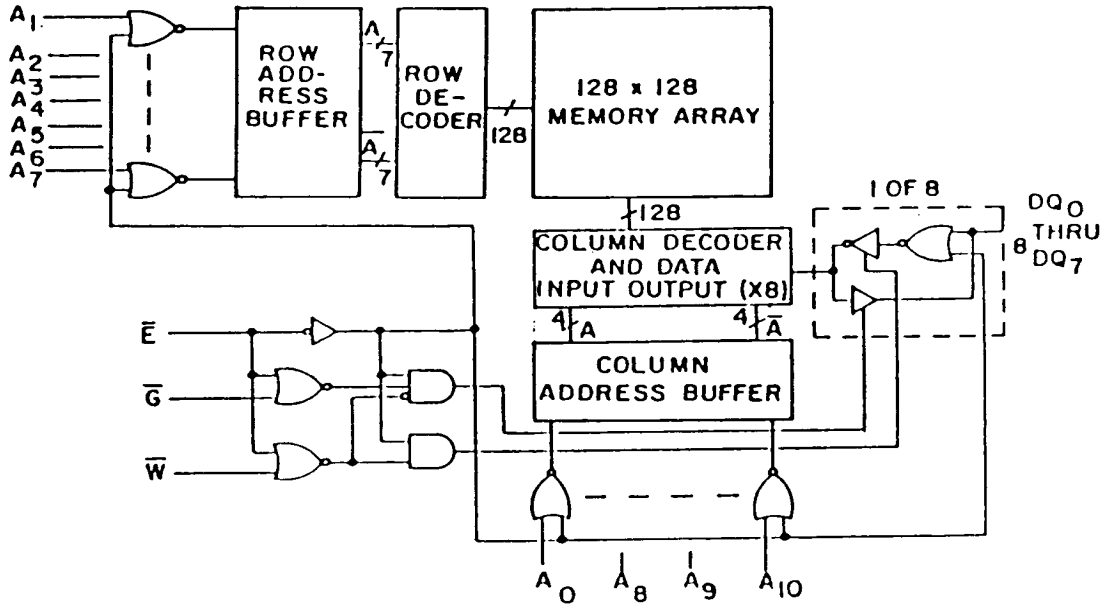
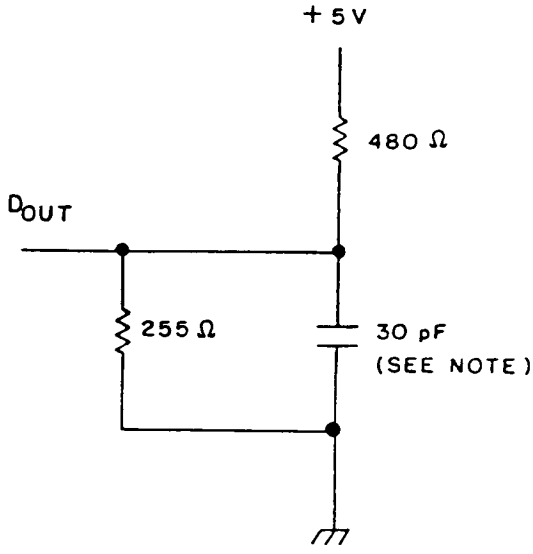
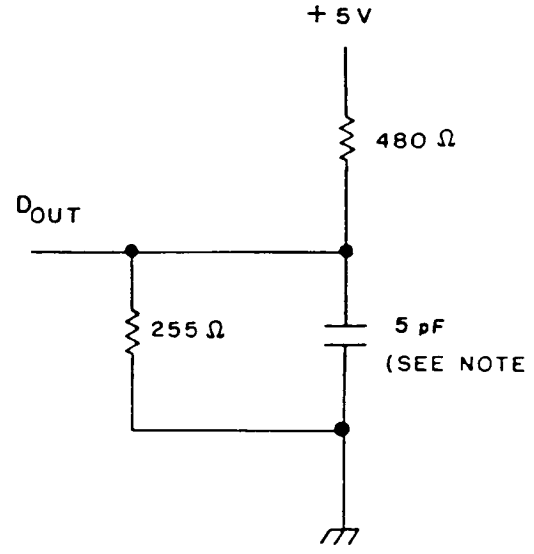


FIGURE 4. Block diagram - Continued.



Circuit A or equivalent circuit

For all other switching parameters.



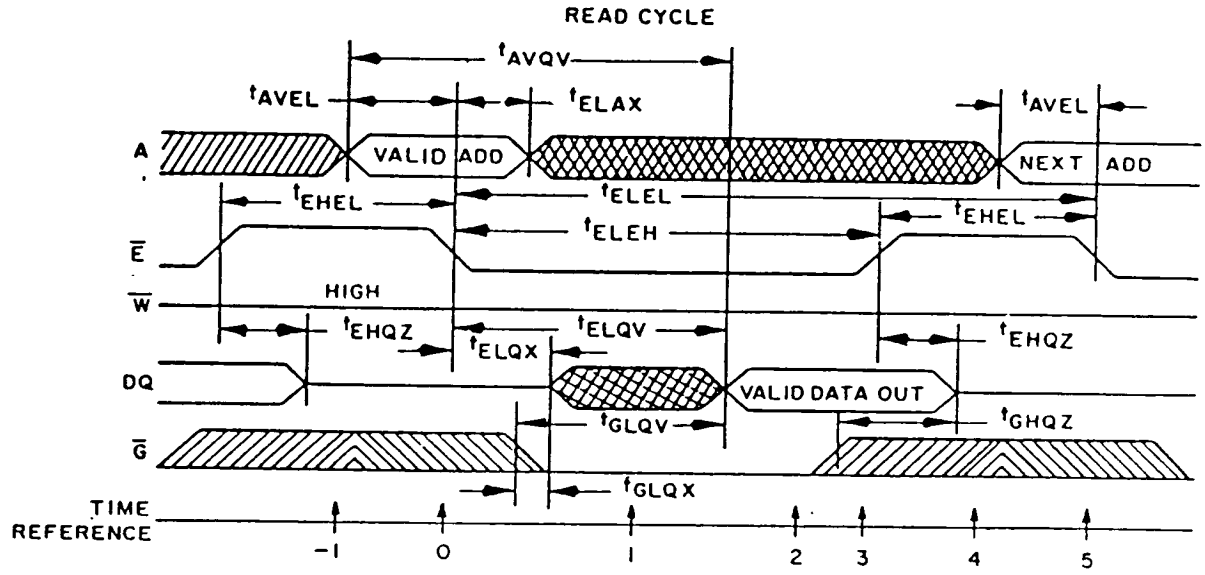
Circuit B or equivalent circuit

for t_{OLQX}, t_{ELQX}, t_{EHQZ}, and t_{OHQZ}.

NOTE:
1. Including scope and jig capacitance.

FIGURE 5. Output loading.

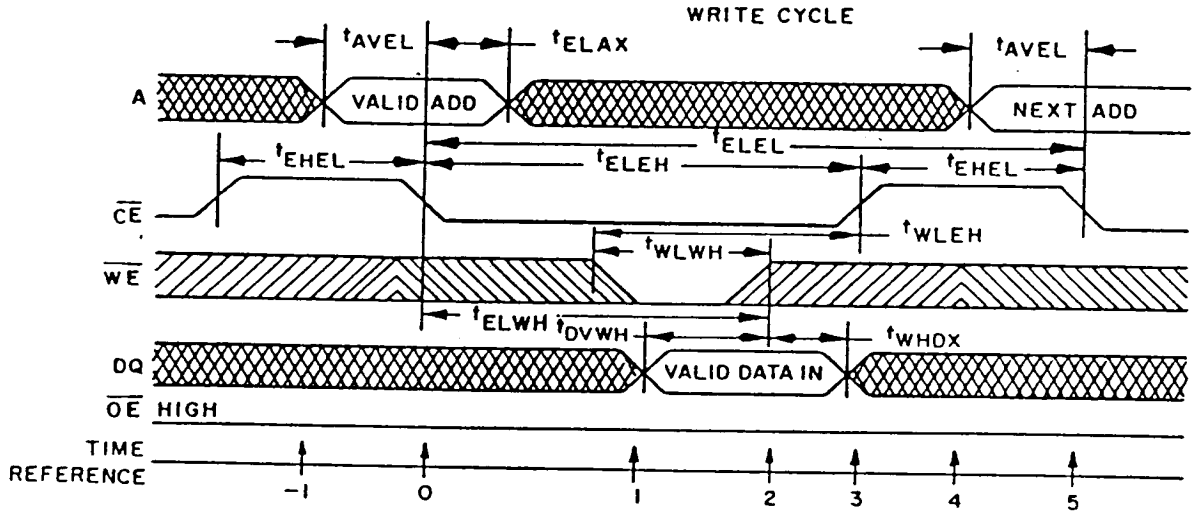
FIGURE 5. Output loading.
Device types 01 and 07



The address information is latched in the on chip registers on the falling edge of CE (t = 0), minimum address setup and hold time requirements must be met. After the required hold time, the address may change state without affecting device operation. During time (t = 1), the outputs become enabled but data is not valid until time (t = 2), WE must remain high throughout the read cycle. After the data has been read, CE may return high (t = 3). This will force the output buffers into a high impedance mode at time (t = 4). OE is used to disable the output buffers when in a logical "1" state (t = -1, 0, 3, 4, 5). After (t = 4) time, the memory is ready for the next cycle.

FIGURE 6. Timing waveforms.

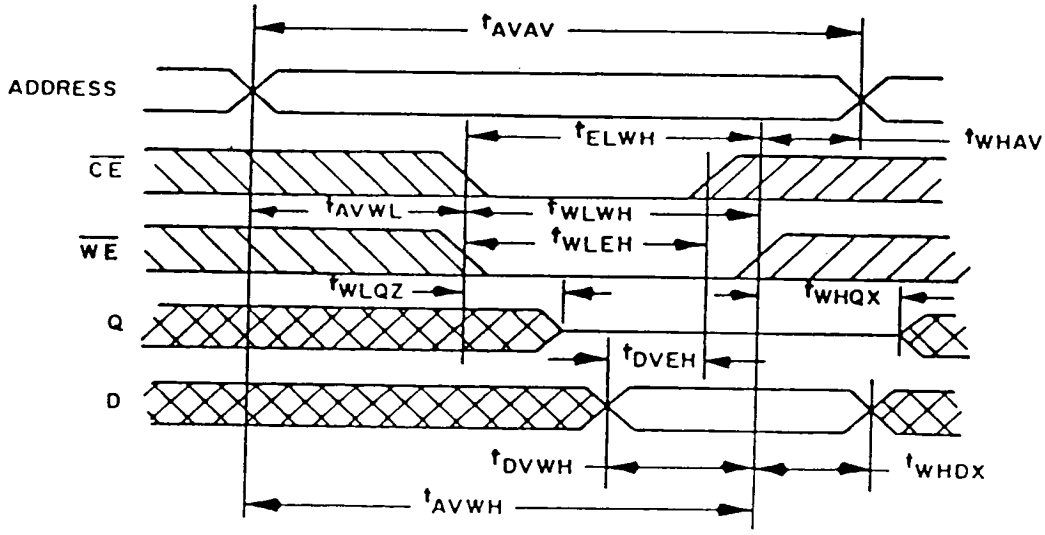
Device types 01 and 07



The write cycles is initiated on the falling edge of $\overline{CE}$ (t = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, OE can be held high (inactive). Parameter t_{DVHW} and t_{WHDX} must be met for proper device operation regardless of OE. If CE and OE fall before WE falls (read mode), a possible bus conflict may exist. If CE rises before WE rises, reference data setup and hold times to the CE rising edge. The write operation is terminated by the first rising edge of WE (t = 2) or CE (t = 3). After the minimum CE high time (t_{EHEL}), the next cycle may begin. If a series of consecutive write cycles are to be performed, the WE line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising of CE.

FIGURE 6. Timing waveforms - Continued.

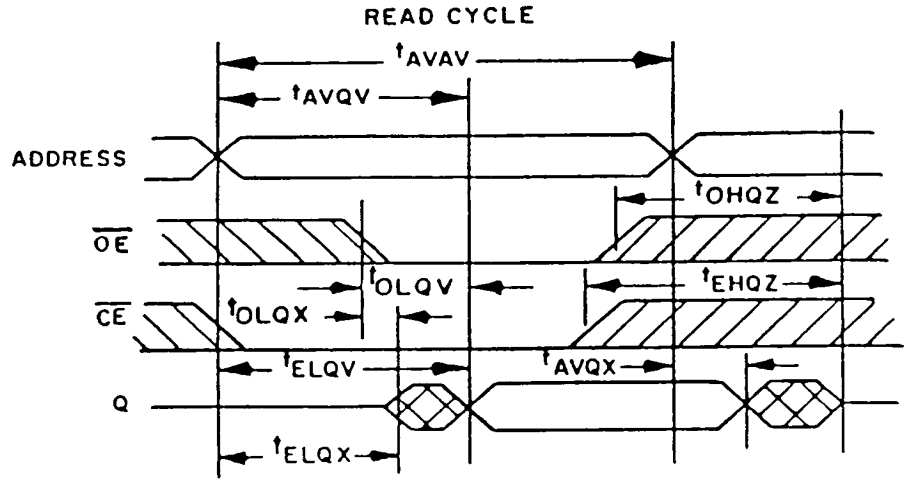
WRITE CYCLE I



NOTE: $\overline{G}$ is low throughout write cycle.

To write, addresses must be stable, $\overline{CE}$ low and $\overline{WE}$ falling low for a period no shorter than t_{WLWH}. Data is in referenced with the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first (t_{DVWH} and t_{WHDX}). While addresses are changing, $\overline{WE}$ must be high. When $\overline{WE}$ falls low, the I/O pins are still in the output state for a period of t_{WLQZ} and input data of the opposite phase to the outputs must not be applied (bus contention). If $\overline{CE}$ transitions low simultaneously with $\overline{WE}$ line transitioning low or after the $\overline{WE}$ transition, the output will remain in a high impedance state. $\overline{OE}$ is held continuously low.

FIGURE 6. Timing waveforms - Continued.



NOTE: $\overline{W}$ is high for a read cycle.

Addresses must remain stable for the duration of the read cycle. To read, $\overline{OE}$ and $\overline{CE}$ must be $\leq V_{IL}$ and $\overline{WE} \geq V_{IH}$. The output buffers can be controlled independently by $\overline{OE}$ while $\overline{CE}$ is low. To execute consecutive read cycles, $\overline{CE}$ may be tied low continuously until all desired locations are accessed. When $\overline{CE}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance stated.

FIGURE 6. Timing waveforms - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 7, 9

* PDA applies to subgroup 1.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Test shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroup 7 and 8 tests shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/2910XB--.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.