046600

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Revise table I conditions. Make editorial changes.	1985 NOV 15	M.A. Frye
B	Convert to military drawing format. Changes to 1.3 and 1.4. Changes to table I. Vendor CAGE 34649 added. Editorial changes throughout.	1987 MAY 21	M.A. Frye
C	Remove vendor CAGE 34649 from device 01. Add device 02. Changes to absolute max ratings. Change drawing CAGE. Editorial changes throughout.	1988 APR 8	M.A. Frye

CURRENT CAGE CODE 67268

REV																								
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REV STATUS OF SHEETS	REV	C	C	B	C	C	B	B	C	B	B	B	B	B	B	C	B	C						
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17						

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Greg A. Pitz

CHECKED BY: Ray Monnin

APPROVED BY: M.A. Frye

DRAWING APPROVAL DATE: 26 November 1984

REVISION LEVEL: C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, CMOS, CLOCK GENERATOR DRIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	84068

SHEET 1 OF 17

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

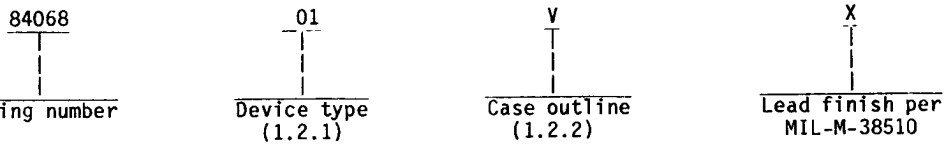
5962-E794

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-833, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit
01	82C84A	25 MHz	CMOS monolithic clock generator driver
02	82C84A	25 MHz	CMOS monolithic clock generator driver

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
V	D-6 (18-lead, .960" x .310" x .200"), dual-in-line package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage (referenced to ground)	+8.0 V dc maximum
Storage temperature range	-65°C to +150°C
Input, output, or I/O voltage applied	GND -0.5 V dc to V_{CC} +0.5 V dc
Maximum power dissipation (P_D)	1 W
Lead temperature (soldering 10 seconds)	+275°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases V and 2	(See MIL-M-38510, appendix C)

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Frequency of operation	25 MHz maximum
Case operating temperature range (T_C)	-55°C to +125°C

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Subgroups 7 and 8 shall consist of verifying the functionality of the device. It forms a part of the vendor's test tape and shall be maintained and available from the approved sources of supply.

TABLE I. Electrical performance characteristics.

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Input high voltage	V_{IH}	V_{CC} = 5.5 V 1/ 2/	All	1, 2, 3	2.2		V
Input low voltage	V_{IL}	V_{CC} = 4.5 V 1/ 2/ 3/	All	1, 2, 3		0.8	V
Output high voltage	V_{OH}	I_{OH} = -4.0 mA CLK output I_{OH} = -2.5 mA all others V_{CC} = 4.5 V 4/	All	1, 2, 3	V_{CC} -0.4		V
Output low voltage	V_{OL}	I_{OL} = +4.0 mA CLK output I_{OL} = +2.5 mA all others V_{CC} = 4.5 V 4/	All	1, 2, 3		0.4	V
Reset input high voltage	V_{IHR}	V_{CC} = 5.5 V	All	1, 2, 3	V_{CC} -0.8		V
Reset input low voltage	V_{ILR}	V_{CC} = 4.5 V	All	1, 2, 3		0.5	V
Reset input hysteresis	$V_{T+}-V_{T-}$	V_{CC} = 4.5 V and 5.5 V	01	1, 2, 3	.2 V_{CC}		V
			02		100		mV
Input leakage current	I_{IL}	V_{IN} = 0 V or V_{CC}, does not include ASYNC, X1 V_{CC} = 5.5 V 5/	All	1, 2, 3	-1.0	1.0	µA
Power supply current	I_{CC}	V_{CC} = 5.5 V Crystal Outputs open 6/	All	1, 2, 3		40	mA
Input capacitance	C_{IN}	Frequency = 1 MHz T_C = +25°C V_{CC} = GND = 0 V V_{IN} = +5 V or GND See 4.3.1c	All	4		10	pF
Output capacitance	C_{OUT}			4		15	
Functional tests		See 4.3.1d	All	7, 8			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 4.5$ V unless otherwise specified 7/ 8/ 9/	Figure no.	Reference no. 10/	Group A subgroups	Limits Min	Limits Max	Unit
External frequency HIGH time	t_{EHEL}	90% - 90% V_{IN} 11/	3	1	9,10,11	13		ns
External frequency LOW time	t_{ELEH}	10% - 10% V_{IN} 11/	3	2	9,10,11	13		
EFI period	t_{ELEL}	11/	3	3	9,10,11	36		
XTAL frequency		12/				2.4	25	MHz
RDY1, RDY2 active setup to CLK	t_{R1VCL}	ASYNC = HIGH 11/	3	4	9,10,11	35		ns
RDY1, RDY2 active setup to CLK	t_{R1VCH}	ASYNC = LOW	3	5		35		
RDY1, RDY2 inactive setup to CLK	t_{R1VCL}		3	4		35		
RDY1, RDY2 hold to CLK	t_{CLR1X}	11/	3	6		0		
ASYNC setup to CLK	t_{AYVCL}		3	7		50		
ASYNC hold to CLK	t_{CLAYX}		3	8		0		
AEN1, AEN2 setup to RDY1, RDY2	t_{A1VR1V}		3	9		15		
AEN1, AEN2 hold to CLK	t_{CLA1X}	11/	3	10		0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 4.5$ V unless otherwise specified 7/ 8/ 9	Figure no.	Reference no. 10/	Group A subgroups	Limits Min	Limits Max	Unit
CSYNC setup to EFI	t_{YHEH}		3	11	9,10,11	20		ns
CSYNC hold to EFI	t_{EHYL}		3	12		20		
CSYNC width	t_{YHYL}	11/	3	13		2 t_{ELEL}		
RES setup to CLK	t_{I1HCL}	13/	3	14		65		
RES hold to CLK	t_{CLI1H}	11/ 13/	3	15		20		
CLK cycle period	t_{CLCL}	11/	3	16		125		
CLK HIGH time	t_{CHCL}	11/	3,4,5	17		$(1/3t_{CLCL})$ +2.0		
CLK LOW time	t_{CLCH}	11/	3,4,5	18		$(2/3t_{CLCL})$ -15		
PCLK HIGH time	t_{PHPL}	11/	3	19		t_{CLCL} -20		
PCLK LOW time	t_{PLPH}	11/	3	20		t_{CLCL} -20		
Ready inactive to CLK 14/	t_{RYLCL}	11/	3,5,7	21		-8		
Ready active to CLK 15/	t_{RYHCH}	11/	3,6,7	22		$(2/3t_{CLCL})$ -15		
CLK to reset delay	t_{CLIL}		3	23			40	
CLK to PCLK HIGH delay	t_{CLPH}		3	24			22	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 4.5$ V unless otherwise specified 7/ 8/ 9/	Figure no.	Reference no. 10/	Group A subgroups	Limits Min	Limits Max	Unit
CLK to PCLK LOW delay	t_{CLPL}		3	25	9,10,11		22	ns
OSC to CLK HIGH delay	t_{OLCH}	11/	3	26		-5	22	
OSC to CLK LOW delay	t_{OLCL}	11/	3	27		2	35	
CLK rise or fall time	t_{CH1CH2} t_{CL2CL1}	+1.0 V to +3.5 V 11/	3	28			10	

1/ F/$\overline{C}$ pin is a strap option and should be held either $\le$0.8 volt or $\ge$2.2 volts. Does not apply to X1 or X2 pin.

2/ Due to test equipment limitations related to noise, the actual tested value may differ from that specified, but the specified limit is guaranteed.

3/ CSYNC pin is tested with $V_{IL} \le$0.8 volt.

4/ Interchanging of force and sense conditions are permitted.

5/ $\overline{ASYNC}$ pin includes an internal 17.5 kΩ nominal pull-up resistor. For $\overline{ASYNC}$ input at GND, $\overline{ASYNC}$ input leakage current = 130 μA nominal.
X1 - crystal feedback input.

6/ f = 25 MHz may be tested using the extrapolated value based on measurements taken at f = 2 MHz and f = 10 MHz.

7/ Unless otherwise specified, all timing delays are measured at 1.5 volts.

8/ Input signals must switch between V_{IL} maximum -.4 volt and V_{IH} minimum +.4 volt. $\overline{RES}$ and F/C must switch between 0.4 V and V_{CC} - 0.4 V. T_R and T_F typically equal to 1 ns/V. $V_{IL} \le V_{IL}$ (max) -.4 V for CSYNC pin.

9/ All ac parameters apply to device types 01 and 02 and are tested per circuit on figure 8.

10/ The reference number refers to the parameter being measured on figure 3.

11/ Not tested but characterized at initial design and major process design changes.

12/ Tested using EFI or X1 input pin.

13/ Setup and hold necessary only to guarantee recognition at next clock.

14/ Applies only to T2 states.

15/ Applies only to T3 TW states.

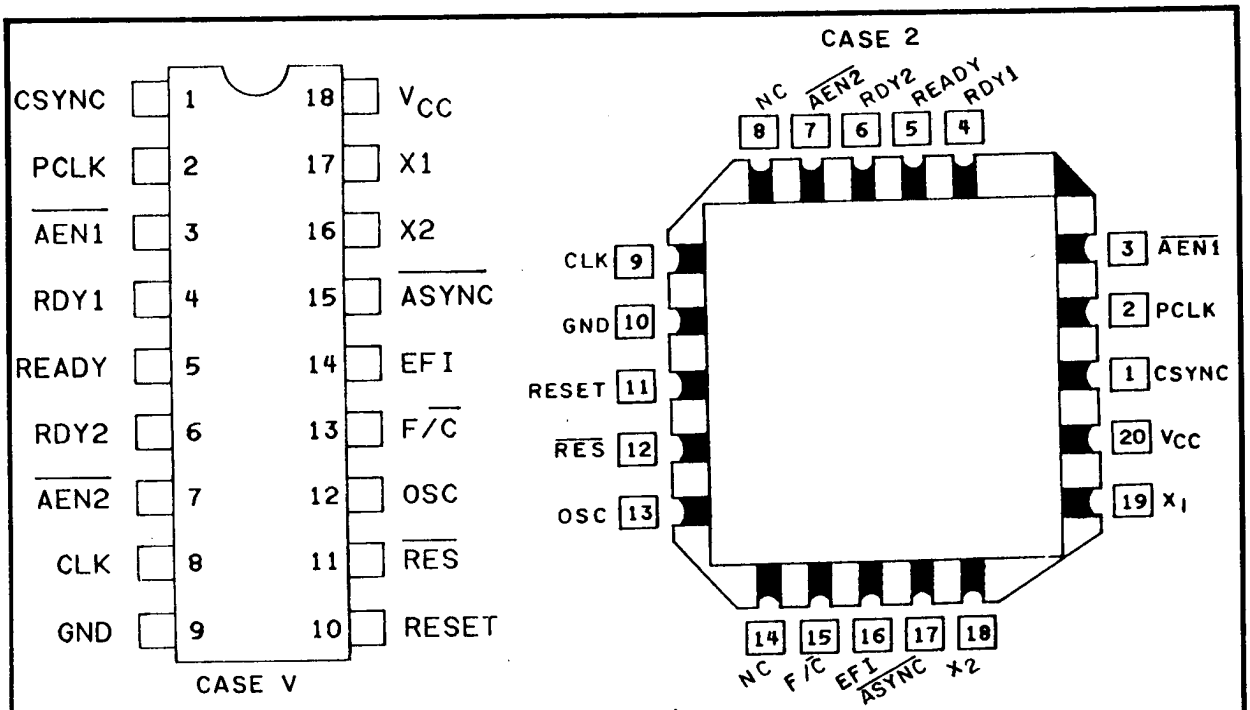

FIGURE 1. Terminal connections.

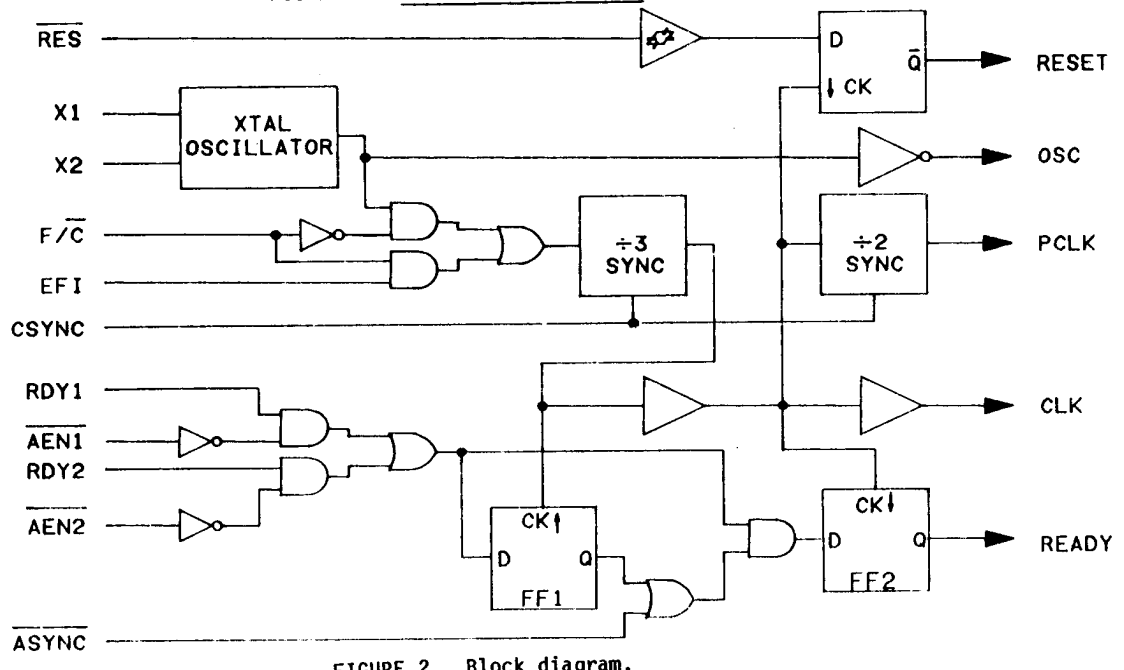

FIGURE 2. Block diagram.

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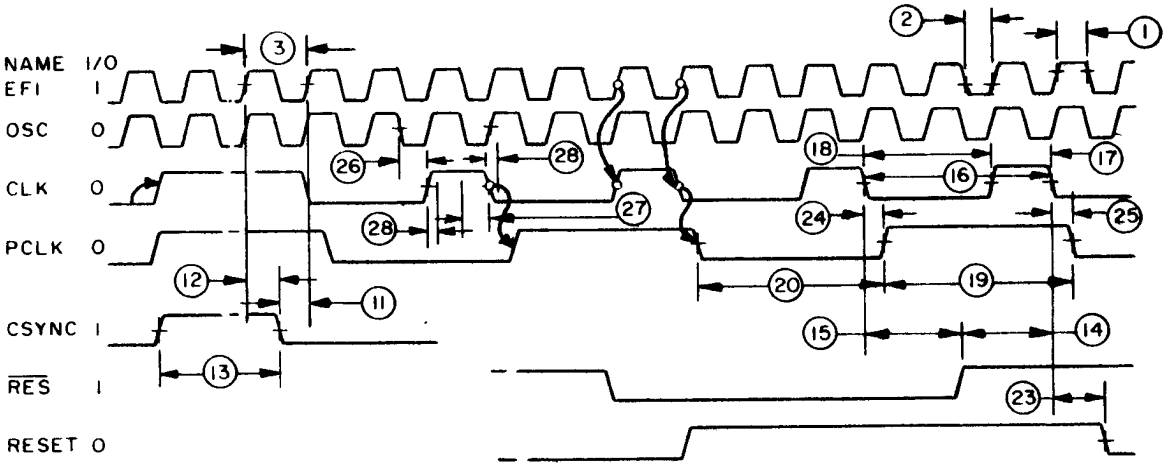

NOTE: ALL TIMING MEASUREMENTS ARE MADE AT 1.5 VOLTS, UNLESS OTHERWISE NOTED.

Waveforms for clocks and reset signals

FIGURE 3. Waveforms.

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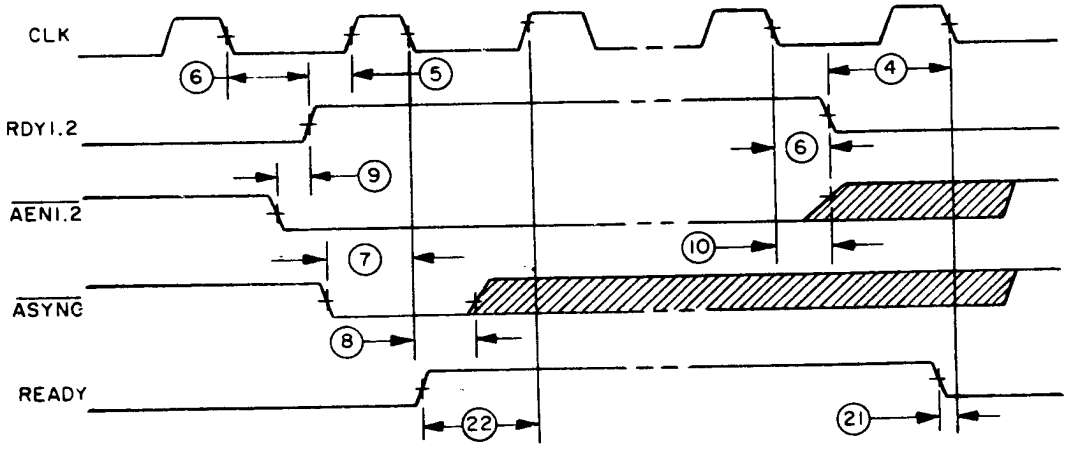
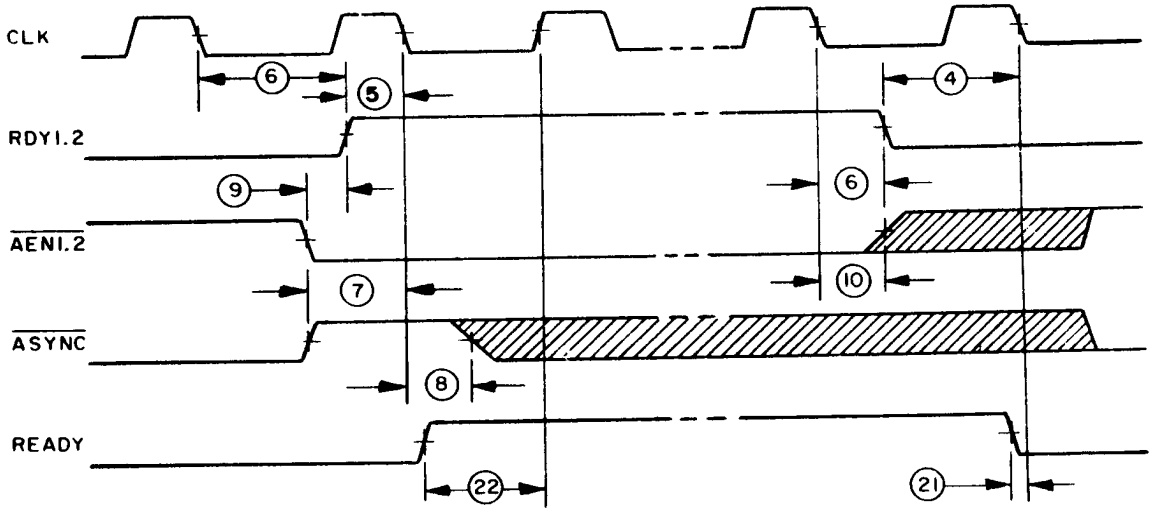


Waveforms for ready signals (for asynchronous devices)



Waveforms for ready signals (for synchronous devices)

FIGURE 3. Waveforms - Continued.

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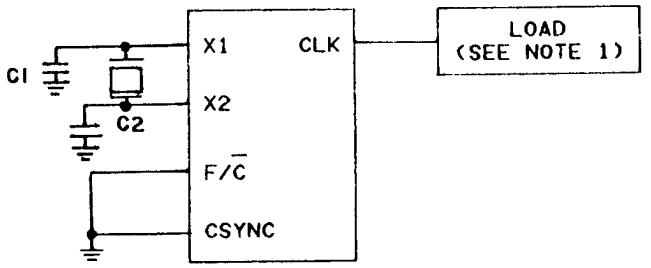
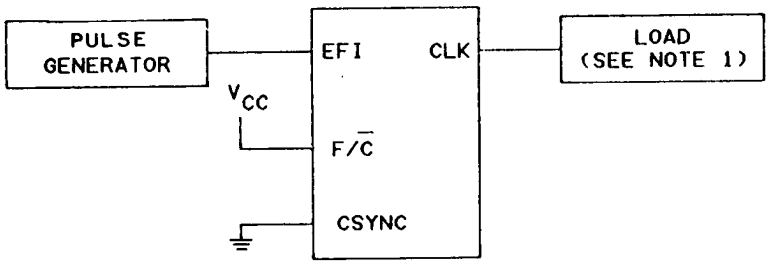


NOTES:
1. C_L = 100 pF.

FIGURE 4. Clock high and low times (using X1 and X2).



NOTES:
1. C_L = 100 pF.

FIGURE 5. Clock high and low times (using EFI).

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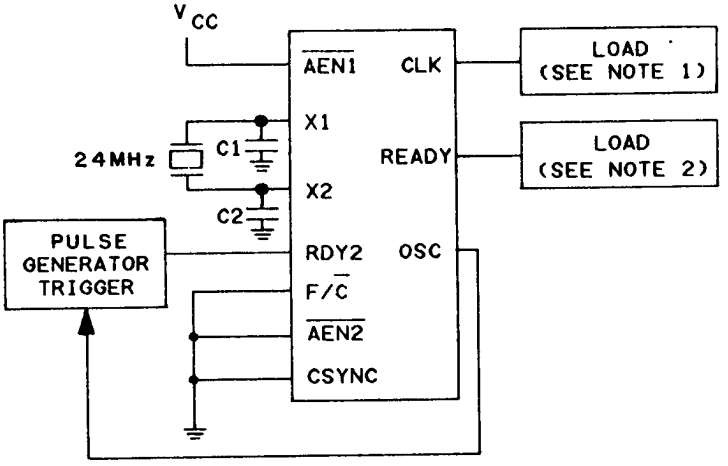
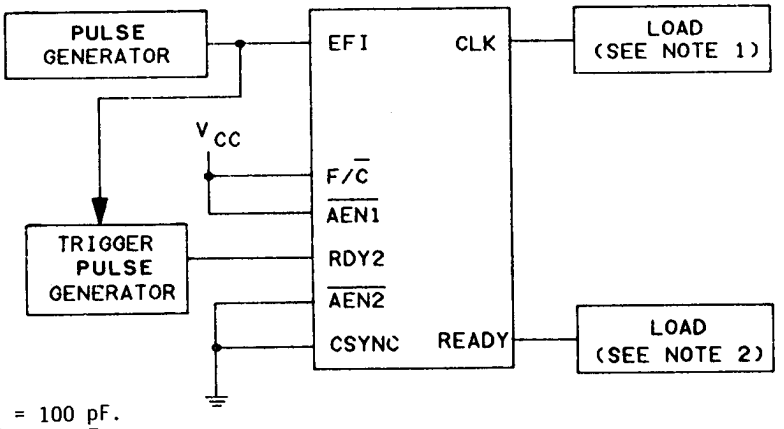


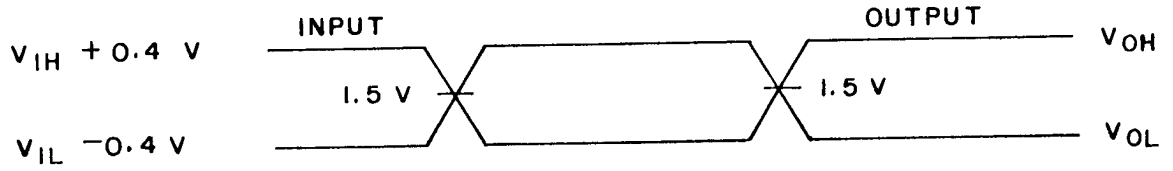
NOTES:
1. C_L = 100 pF.
2. C_L = 30 pF.

FIGURE 6. Ready to clock (using X1 and X2).

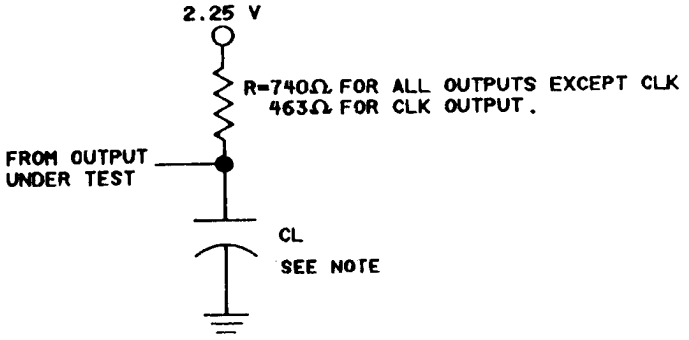


NOTES:
1. C_L = 100 pF.
2. C_L = 30 pF.

FIGURE 7. Ready to clock (using EFI).



AC testing: All input signals must switch between V_{IL} (max) -0.4 V and V_{IH} (min) +0.4 V. $\overline{RES}$ and F/$\overline{C}$ must switch between 0.4 V and V_{CC} -0.4 V. T_R and T_F typically equal 1 ns/V. $V_{IL} \leq$ VIL (max) -0.4 V for CSYNC pin.



NOTE: C_L includes test fixture capacitance.

FIGURE 8. AC test circuit.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,9
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11**
Groups C and D end-point electrical parameters (method 5005)	2,8 (+125°C only)
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Terminal and functional definitions. Terminal and functional definitions and descriptions for this device shall be as follows:

Symbol	Definition
$\overline{AEN1}$, $\overline{AEN2}$	ADDRESS ENABLE. $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or $\overline{RDY2}$). AEN1 validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non-Multi-Master configurations, the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	BUS READY (transfer complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by AEN1 while RDY2 is qualified by AEN2.
$\overline{ASYNC}$	READY SYNCHRONIZATION SELECT. $\overline{ASYNC}$ is an input which defines the synchronization mode of the $\overline{READY}$ logic. When ASYNC is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH, a single stage of READY synchronization is provided.
READY	READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	CRYSTAL IN. X1 and X2 are the pins to which a crystal is attached. The crystal frequency is three times the desired processor clock frequency.
F/$\overline{C}$	FREQUENCY/CRYSTAL SELECT. F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	EXTERNAL FREQUENCY IN. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave three times the frequency of the desired CLK output.
CLK	PROCESSOR CLOCK. CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is one-third of the crystal or EFI input frequency and a one-third duty cycle.
PCLK	PERIPHERAL CLOCK. PCLK is a peripheral clock signal whose output frequency is one-half that of CLK and has a 50 percent duty cycle.
OSC	OSCILLATOR OUTPUT. OSC is the output of the internal oscillator circuitry; its frequency is equal to that of the crystal.
$\overline{RES}$	RESET IN. $\overline{RES}$ is an active LOW signal which is used to generate RESET. The device provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.

RESET	RESET is an active HIGH signal which is used to reset the processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	CLOCK SYNCHRONIZATION. CSYNC is an active HIGH signal which allows multiple devices to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator, CSYNC should be hardwired to ground.
GND	Ground.
V_{CC}	+5 V supply.

6.5 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
8406801VX	34371	MD82C84A/883	---
84068012X	34371	MR82C84A/883	---
8406802VX	34649	MD82C84A/B	

1/ Caution. Do not use this number for item aquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P.O. Box 883 Melbourne, FL 32901
34649	Intel Corporation 5000 W. Williams Field Road Chandler, AZ 85224