REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
B	Convert to military drawing format. Add vendor CAGE no. 27014 to case 2.	1988 FEB 12	M.A. Frye

CURRENT CAGE CODE 67268

REV																									
SHEET																									
REV																									
SHEET																									
REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13											

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: James E. Jamison

CHECKED BY: Charles Reusing

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 28 September 1984

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, HIGH-SPEED CMOS, 4-BIT SYNCHRONOUS BCD COUNTER WITH SYNCHRONOUS RESET, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	84094

SHEET 1 OF 13

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E769

1. SCOPE

1.1 Scope. This drawing describes device requirements for clas B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

84094	01	E	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC162	4-bit synchronous BCD counter with synchronous reset

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
F	F-5 (16-lead, 1/4" x 3/8"), flat package
2	C-2 (20-terminal, .350" x .350"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
DC input voltage	-0.5 V dc to V_{CC} +0.5 V dc
DC output voltage	-0.5 V dc to V_{CC} +0.5 V dc
Clamp diode current	±20 mA
DC output current (per pin)	±25 mA
DC V_{CC} or GND current (per pin)	±50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation, P_D	500 mW 2/
Lead temperature (soldering, 10 seconds)	260°C
Thermal resistance, junction to case (θ_{JC}):	
Case outlines E, F, and 2	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage	+2.0 V dc to +6.0 V dc
Case operating temperature range	-55°C to +125°C
Input rise or fall time:	
V_{CC} = 2.0 V	0 to 500 ns
V_{CC} = 4.5 V	0 to 500 ns
V_{CC} = 6.0 V	0 to 400 ns

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ For T_C = +100°C to +125°C, derate lineraly at 12 mW/°C.

Minimum recovery time, clear to clock (t_{REC}) 3/:

at 25°C	
V_{CC} = 2.0 V	125 ns
V_{CC} = 4.5 V	25 ns
V_{CC} = 6.0 V	21 ns
at -55°C to +125°C	
V_{CC} = 2.0 V	186 ns
V_{CC} = 4.5 V	37 ns
V_{CC} = 6.0 V	32 ns

Minimum setup time, load, clear or data, to clock (t_S) 3/:

at 25°C	
V_{CC} = 2.0 V	150 ns
V_{CC} = 4.5 V	30 ns
V_{CC} = 6.0 V	26 ns
at -55°C to +125°C	
V_{CC} = 2.0 V	225 ns
V_{CC} = 4.5 V	45 ns
V_{CC} = 6.0 V	38 ns

Minimum setup time, enable to clock (t_S):

at 25°C	
V_{CC} = 2.0 V	175 ns
V_{CC} = 4.5 V	35 ns
V_{CC} = 6.0 V	30 ns
at -55°C to +125°C	
V_{CC} = 2.0 V	260 ns
V_{CC} = 4.5 V	52 ns
V_{CC} = 6.0 V	44 ns

Minimum pulse width, load, clear or clock (t_W) 3/:

at 25°C	
V_{CC} = 2.0 V	100 ns
V_{CC} = 4.5 V	20 ns
V_{CC} = 6.0 V	17 ns
at -55°C to +125°C	
V_{CC} = 2.0 V	150 ns
V_{CC} = 4.5 V	30 ns
V_{CC} = 6.0 V	26 ns

Minimum hold time, data from clock (t_H) 3/:

at 25°C	
V_{CC} = 2.0 V	50 ns
V_{CC} = 4.5 V	10 ns
V_{CC} = 6.0 V	9 ns
at -55°C to +125°C	
V_{CC} = 2.0 V	75 ns
V_{CC} = 4.5 V	15 ns
V_{CC} = 6.0 V	13 ns

Minimum hold time, enable, load, or clear from clock (t_H):

at 25°C	
V_{CC} = 2.0 V	25 ns
V_{CC} = 4.5 V	5 ns
V_{CC} = 6.0 V	5 ns
at -55°C to +125°C	
V_{CC} = 2.0 V	40 ns
V_{CC} = 4.5 V	8 ns
V_{CC} = 6.0 V	7 ns

See footnote on next page.

Maximum clock frequency (f_{CL}) 3/:

at 25°C	
V_{CC} = 2.0 V	5 MHz
V_{CC} = 4.5 V	25 MHz
V_{CC} = 6.0 V	29 MHz
at -55°C to +125°C	
V_{CC} = 2.0 V	3.4 MHz
V_{CC} = 4.5 V	17 MHz
V_{CC} = 6.0 V	20 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table and logic diagram. The truth table and logic diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3/ See figure 3.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 20$ µA	V_{CC} = 2.0 V	1,2,3	1.9		V
			V_{CC} = 4.5 V		4.4		
			V_{CC} = 6.0 V		5.9		
		$\lvert I_O \rvert \le 4.0$ mA	V_{CC} = 4.5 V		3.7		
		$\lvert I_O \rvert \le 5.2$ mA	V_{CC} = 6.0 V		5.2		
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 20$ µA	V_{CC} = 2.0 V	1,2,3		0.1	V
			V_{CC} = 4.5 V			0.1	
			V_{CC} = 6.0 V			0.1	
		$\lvert I_O \rvert \le 4.0$ mA	V_{CC} = 4.5 V			0.4	
		$\lvert I_O \rvert \le 5.2$ mA	V_{CC} = 6.0 V			0.4	
High-level input voltage 2/	V_{IH}		V_{CC} = 2.0 V	1,2,3	1.5		V
			V_{CC} = 4.5 V		3.15		
			V_{CC} = 6.0 V		4.2		
Low-level input voltage 2/	V_{IL}		V_{CC} = 2.0 V	1,2,3		0.3	V
			V_{CC} = 4.5 V			0.9	
			V_{CC} = 6.0 V			1.2	
Input capacitance	C_{IN}	V_{IN} = 0 V, T_C = +25°C See 4.3.1c		4		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions		Group A subgroups	Limits Min	Limits Max	Unit
Quiescent current	I_{CC}	V_{CC} = 6.0, V_{IN} = V_{CC} or GND		1,2,3		160	µA
Input leakage current	I_{IN}	V_{CC} = 6.0, V_{IN} = V_{CC} or GND		1,2,3		±1	µA
Functional tests		See 4.4.1d		7			
Propagation delay, clock to carry 3/	t_{PHL1}, t_{PLH1}	T_C = +25°C, C_L = 50 pF ±10% See figure 3	V_{CC} = 2.0 V	9		225	ns
			V_{CC} = 4.5 V			43	
			V_{CC} = 6.0 V			37	
		T_C = -55°C, +125°C, C_L = 50 pF ±10% See figure 3	V_{CC} = 2.0 V	10,11		340	ns
			V_{CC} = 4.5 V			65	
			V_{CC} = 6.0 V			55	
Propagation delay, clock to Q 3/	t_{PHL2}, t_{PLH2}	T_C = +25°C, C_L = 50 pF ±10% See figure 3	V_{CC} = 2.0 V	9		205	ns
			V_{CC} = 4.5 V			42	
			V_{CC} = 6.0 V			35	
		T_C = -55°C, +125°C, C_L = 50 pF ±10% See figure 3	V_{CC} = 2.0 V	10,11		310	ns
			V_{CC} = 4.5 V			62	
			V_{CC} = 6.0 V			53	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions		Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay, ENT to carry 3/	t_{PHL3}, t_{PLH3}	T_C = +25°C, C_L = 50 pF ±10%, See figure 3	V_{CC} = 2.0 V	9		195	ns
			V_{CC} = 4.5 V			39	
			V_{CC} = 6.0 V			33	
		T_C = -55°C, +125°C, C_L = 50 pF ±10%, See figure 3	V_{CC} = 2.0 V	10,11		295	ns
			V_{CC} = 4.5 V			59	
			V_{CC} = 6.0 V			50	
Transition time 4/	t_{THL}, t_{TLH}	T_C = +25°C, C_L = 50 pF ±10%, See figure 3	V_{CC} = 2.0 V	9		75	ns
			V_{CC} = 4.5 V			15	
			V_{CC} = 6.0 V			13	
		T_C = -55°C, +125°C, C_L = 50 pF ±10%, See figure 3	V_{CC} = 2.0 V	10,11		110	ns
			V_{CC} = 4.5 V			22	
			V_{CC} = 6.0 V			19	

1/ For a power supply of 5 V ±10%, the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage currents (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 90 pF, determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}{}^2f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

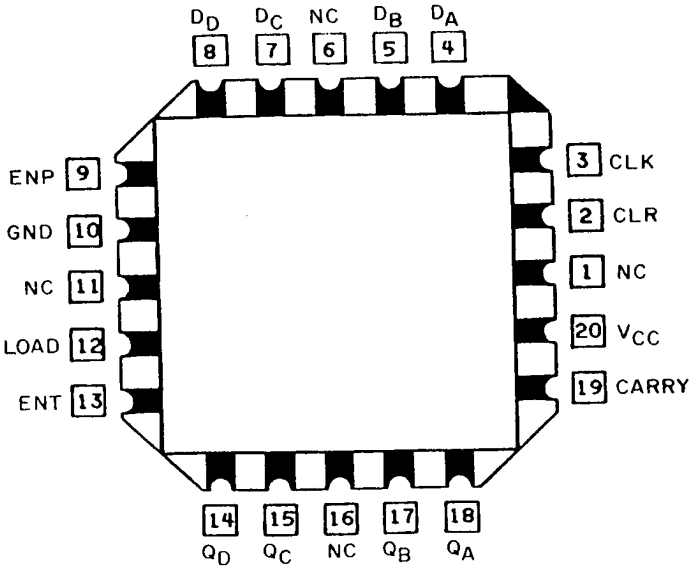
2/ V_{IH} and V_{IL} test not required if applied as forcing function for V_{OH} and V_{OL}.

3/ AC testing at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested, to the specified parameters.

4/ Transition times (t_{THL}, t_{TLH}), if not tested, shall be guaranteed to the specified parameters.

Device type 01

Case 2



Cases E and F

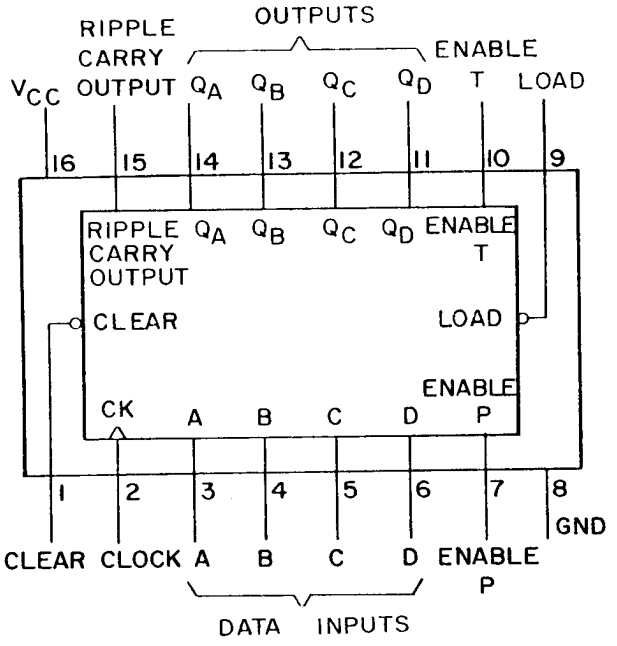


FIGURE 1. Terminal connections (top view).

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84094
		REVISION LEVEL B	SHEET 8

Device type 01

CLK	CLR	ENP	ENT	Load	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count and RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count and RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

H = high level, L = low level
X = don't care ↑ = low to high transition

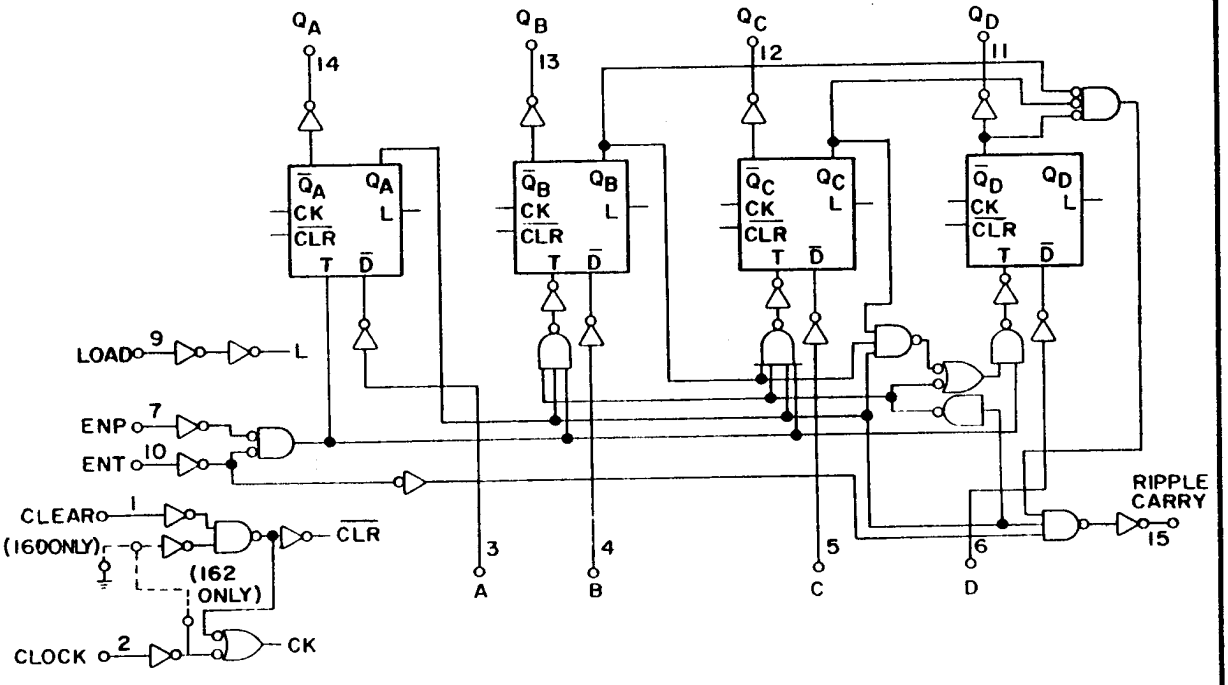


FIGURE 2. Truth table and logic diagram.

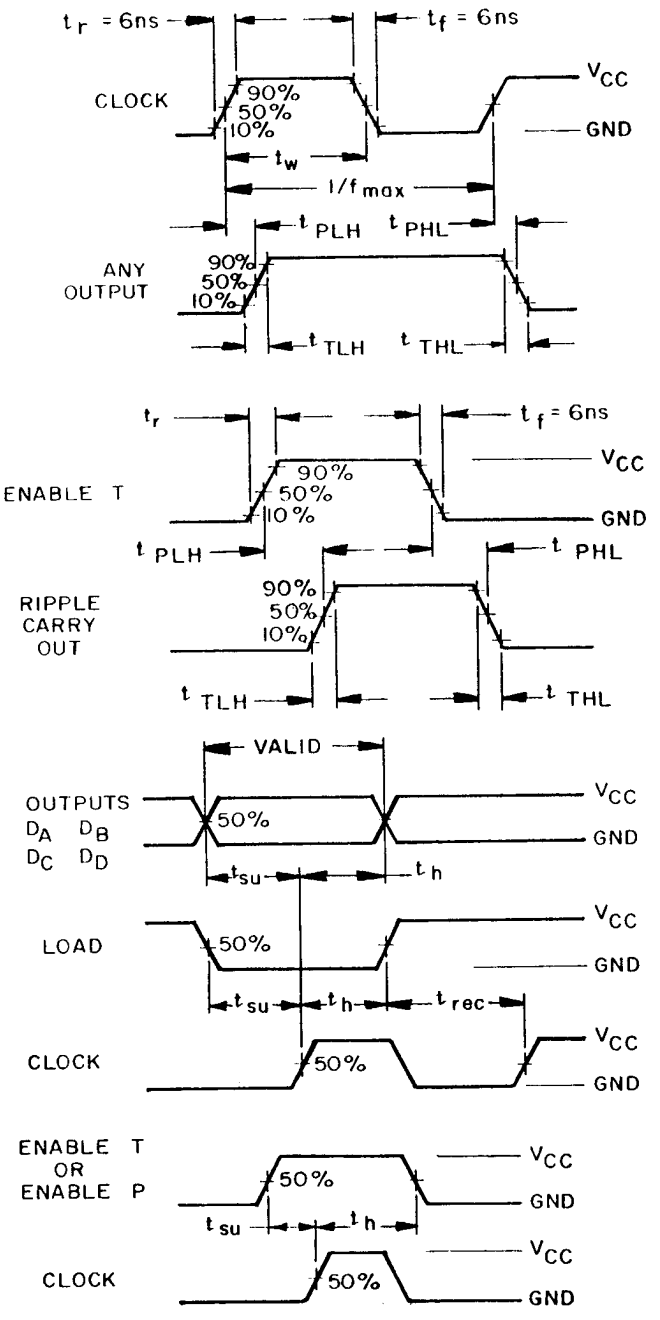


FIGURE 3. Switching waveform.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84094
		REVISION LEVEL B	SHEET 10

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroup 7 test sufficient to verify the truth table.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

*PDA applies to subgroup 1.
**Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/66303B--.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
8409401EX	01295	SNJ54HC162J	M38510/66303BEX
	04713	54HC162/BEAJC	
	27014	MM54HC162J/883	
	18714	CD54HC162F/3A	
8409401FX	01295	SNJ54HC162W	M38510/66303BFX
84094012X	01295	SNJ54HC162FK	M38510/66303B2X
	04713	54HC162M/B2CJC	
	27014	MM54HC162E/883	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. P.O. Box 6448 Midland, TX 79701
04713	Motorola, Inc. 7402 S. Price Road Tempe, AZ 85283
18714	GE/RCA Corp. Route 202 Somerville, NJ 08876
27014	National Semiconductor 2900 Semiconductor Drive Santa Clara, CA 95051