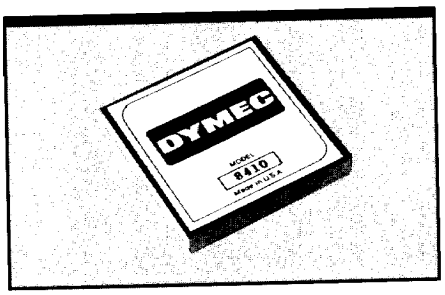
DYMEC

A Subsidiary of
SILICON TRANSISTOR CORP.

MODELS

8410, 8411, 8412, 8413, 8414, 8415, 8416, 8417

1MHz Voltage-to-Frequency Converter Family



Description

The **8410 Series** are high performance, high precision 1MHz full scale Voltage-to-Frequency Converters intended for applications which require high resolution, very high linearity, and a six decade dynamic range. Units are available with varying gain drift performance over temperature in both single-ended and differential input configurations. The Single-ended analog voltage input of all units is 10μV to 10V full scale with a 10% overange capability. The differential input signal is either a positive or negative 10μV to 10V full scale, with common-mode signals attenuated by 60dB minimum. The input signal is converted to an output proportional to the full scale frequency, within 0.001% linearity, utilizing the long-proven charge balance technique. A buffered TTL-compatible frequency output with a 10 TTL-load fanout is provided that will drive up to 200pF capacitive loads.

Stability of the **8410 Series** over temperature is excellent, with a 40μV/°C maximum offset and 15ppm/°C maximum (**8413**) gain tempco. Warmup time to 0.02% accuracy is less than two (2) minutes.

In applications that require slightly different specifications such as different full scale output frequency, or where fixed offset or different full scale voltages would be convenient, **custom frequencies** and/or **custom trimming** can be easily accommodated. Other varia-

Features

- **Guaranteed Minimum/ Maximum Specifications**
- **Wide Dynamic Range**
  >1,000,000:1
  >120dB
- **Excellent Linearity**
  0.001% FS ±0.02% of input
- **Excellent Stability**
  10μV/°C offset
  10ppm/°C gain
- **Buffered Frequency Output**
  10 TTL loads
- **Self-contained Subsystem**
  2" x 2" x 0.4" module
- **Low Power**
  <0.95W

Applications

- **Analytical Instrumentation**
- **Medical Instrumentation**
- **Telemetry**
- **Data Recording**
- **Weighing Systems**

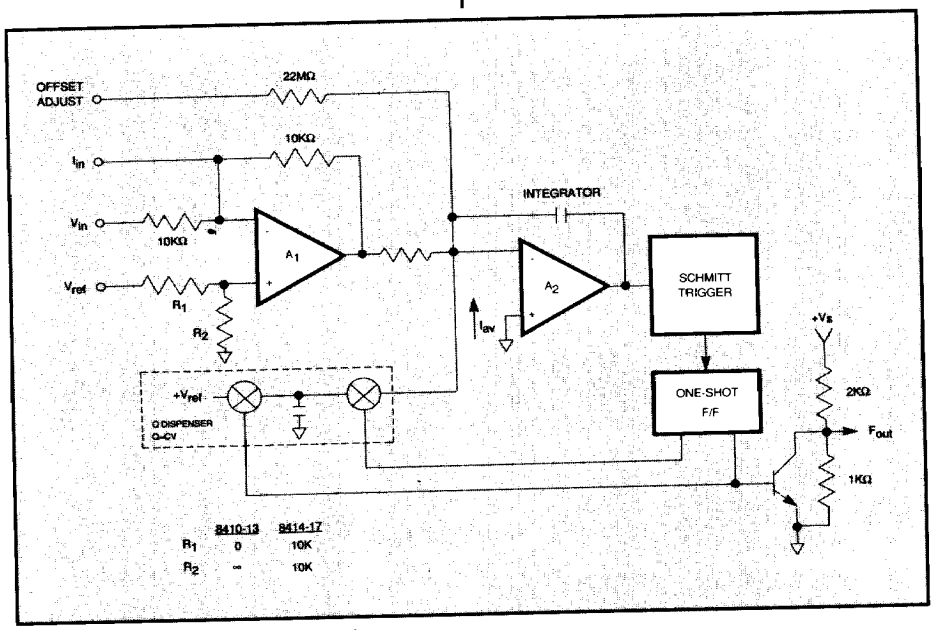


Figure 1. 8410 Series Block Diagram

Specifications

All Specifications Guaranteed at 25°C Unless Otherwise Noted

Analog Input

Input Range
±10μV to ±10V
Current Range
+1nA to +1mA
Overrange
10% minimum
Configuration
8410, 8411, 8412, 8413
Single-ended
8414, 8415, 8416, 8417
Differential
Common-Mode Voltage Range
8414, 8415, 8416, 8417
±10V minimum
Common-Mode Rejection Ratio
8414, 8415, 8416, 8417
60dB minumum, 66dB typical; See Note 1
Offset Voltage
±3mV typical; ±10mV maximum; adjustable to zero
Input Bias Current
100nA maximum
Impedance ($+V_{in}$)
10KΩ, ±1%
Impedance (V_{ref})
8410, 8411, 8412, 8413
500KΩ minimum
Impedance (Differential)
8414, 8415, 8416, 8417
40KΩ, ±1%
Overvoltage Protection (I_{IN} Terminal)
$\pm V_S$ without damage
Overvoltage Protection (V_{ref} Terminal)
$\pm 2V_S$ without damage

Transfer Characteristics

Full Scale Frequency Output (F_{out})
1MHz +10% overrange
Transfer Characteristic
1MHz (V_{in}/10V)
Full Scale Factor
1mA ±0.1%, or 10V trimmable to 1MHz
Non-Linearity
±0.001% FS, ±0.02% of input maximum;
not specified under overrange conditions
Full Scale Step Response (to 0.01%)
2 cycles of new frequency plus 15μs
Overload Recovery
6 cycles of new frequency

Stability

Gain - Tempco

8410, 8414	**8411, 8415**
60ppm FS/°C typical	35ppm FS/°C typical
100ppm FS/°C maximum	50ppm FS/°C maximum
8412, 8416	**8413, 8417**
15ppm FS/°C typical	10ppm FS/°C typical
25ppm FS/°C maximum	15ppm FS/°C maximum

Gain - PS Sensitivity
100ppm/1% change in supply voltage
Gain - Drift Per Day
±100ppm FS maximum
Gain - Drift Per Month
±200ppm FS maximum
Offset - Tempco
±10μV typical; ±40μV maximum
Offset - PS Sensitivity
20μV/V change in supply voltage
Offset - Drift Per Day
±10μV typical
Offset - Drift Per Month
±20μV typical
Warmup Time
≤2 minutes to 0.02% accuracy

Output

Pulse Polarity
Positive
Pulse Width
500ns ±100ns
Logic Levels

Logic "1" (High)	**Logic "0" (Low)**
+4.0V ±0.5V	<0.4V @ 16mA sink

Load
≤200pF for rated performance
Fanout
10 TTL loads
Short Circuit Protection
Indefinite to ground without damage

Power Requirements

($+V_S$) +15V, ±5%	**($-V_S$) -15V, ±5%**
40mA maximum	20mA maximum

Power Dissipation
0.95W maximum

Environmental and Mechanical

Operating Temperature
(to Rated Performance)
0°C to +70°C
Operating Temperature
(to 50% Derated TC, Linearity, and Fanout)
-25°C to +85°C
Storage Temperature
-55°C to +125°C
Humidity
0-85%, non-condensing up to 40°C
Dimensions
2.00" x 2.00" x 0.40"
(50.8 x 50.8 x 10.16mm)

Note 1: CMRR specification given assumes zero (0) ohms for GAIN ADJUST potentiometer. With GAIN ADJUST potentiometer at 200Ω, CMRR is 34dB.

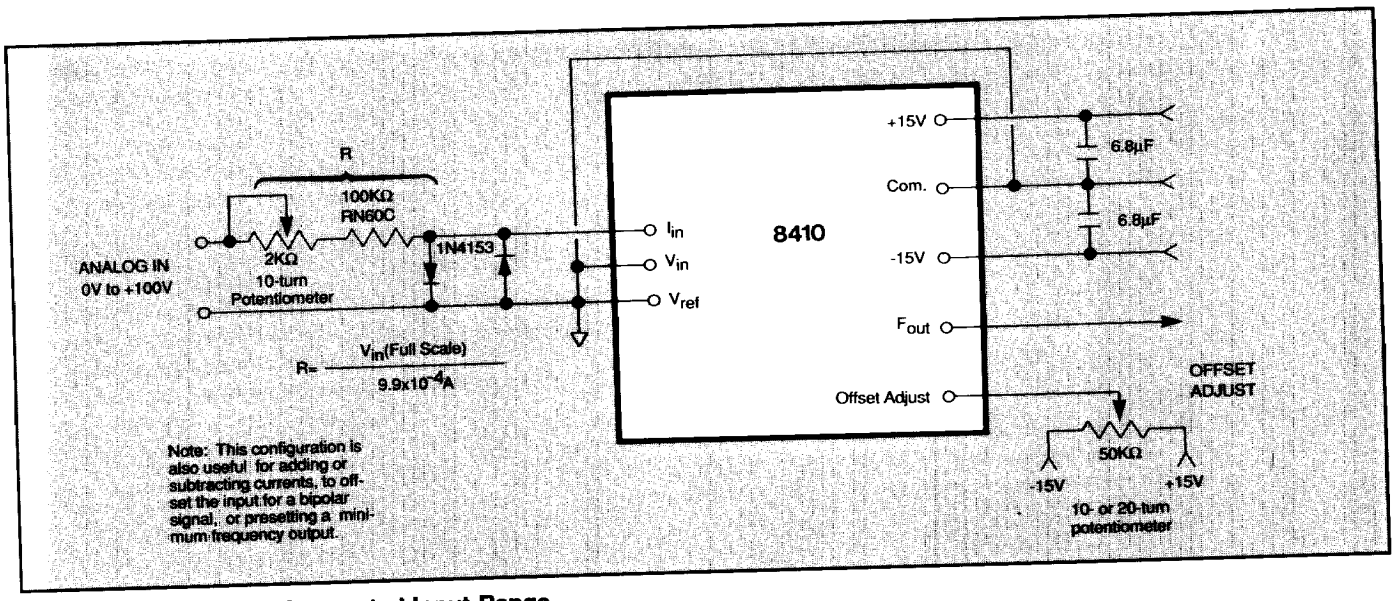


Figure 3. Expanded or Contracted Input Range

frequency approximately 10kHz above 1MHz. The GAIN ADJUST potentiometer will only trim the output frequency higher.

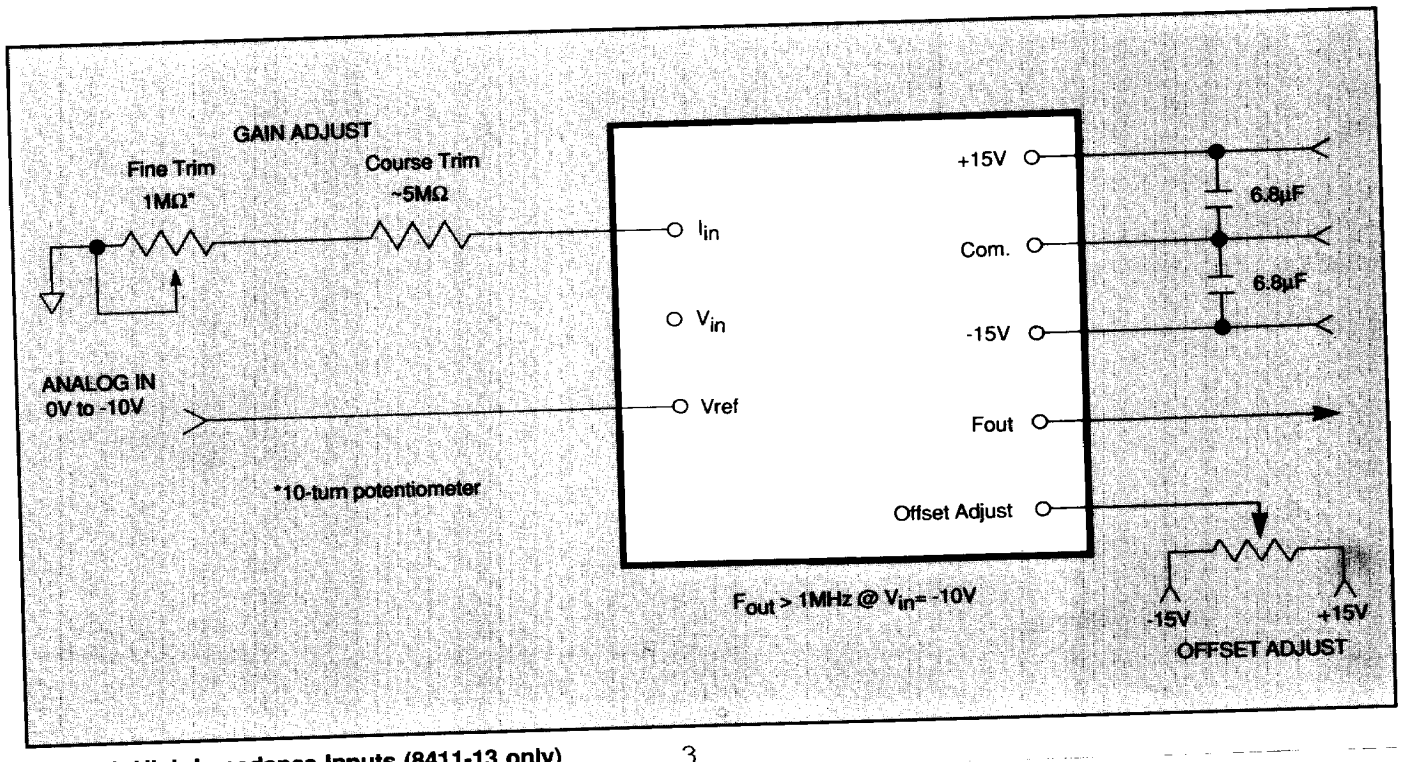
Differential Inputs

The input can be configured as a differential input as shown in Figure 5. The differential input impedance is 40KΩ. The maximum common mode voltage is ±10V.

Negative Input Currents (8410-8413 only)

Figure 6 shows the input configuration for negative input currents. No degradation in performance will occur for full scale frequencies of 1MHz with input voltages ($-I_{in}*R_L$) from -10V down to -1V.

If some degradation of dynamic range and stability can be tolerated, an input voltage as low as -1mV can be used. This degradation is due to the input voltage drift and bias current when compared to signal voltage and current levels. The input configuration is differential, referred to the Vref input.



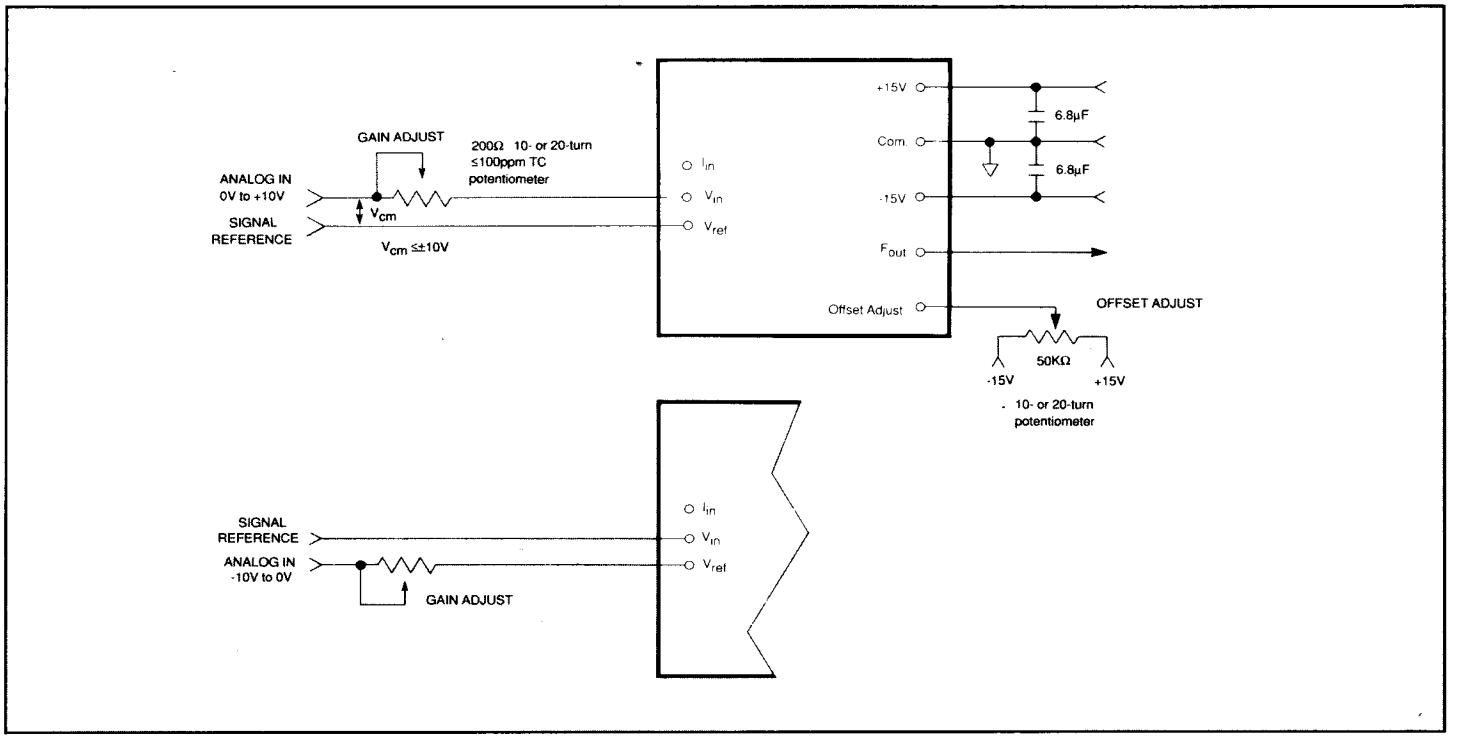


Figure 5. Differential Inputs (8414-17 only)

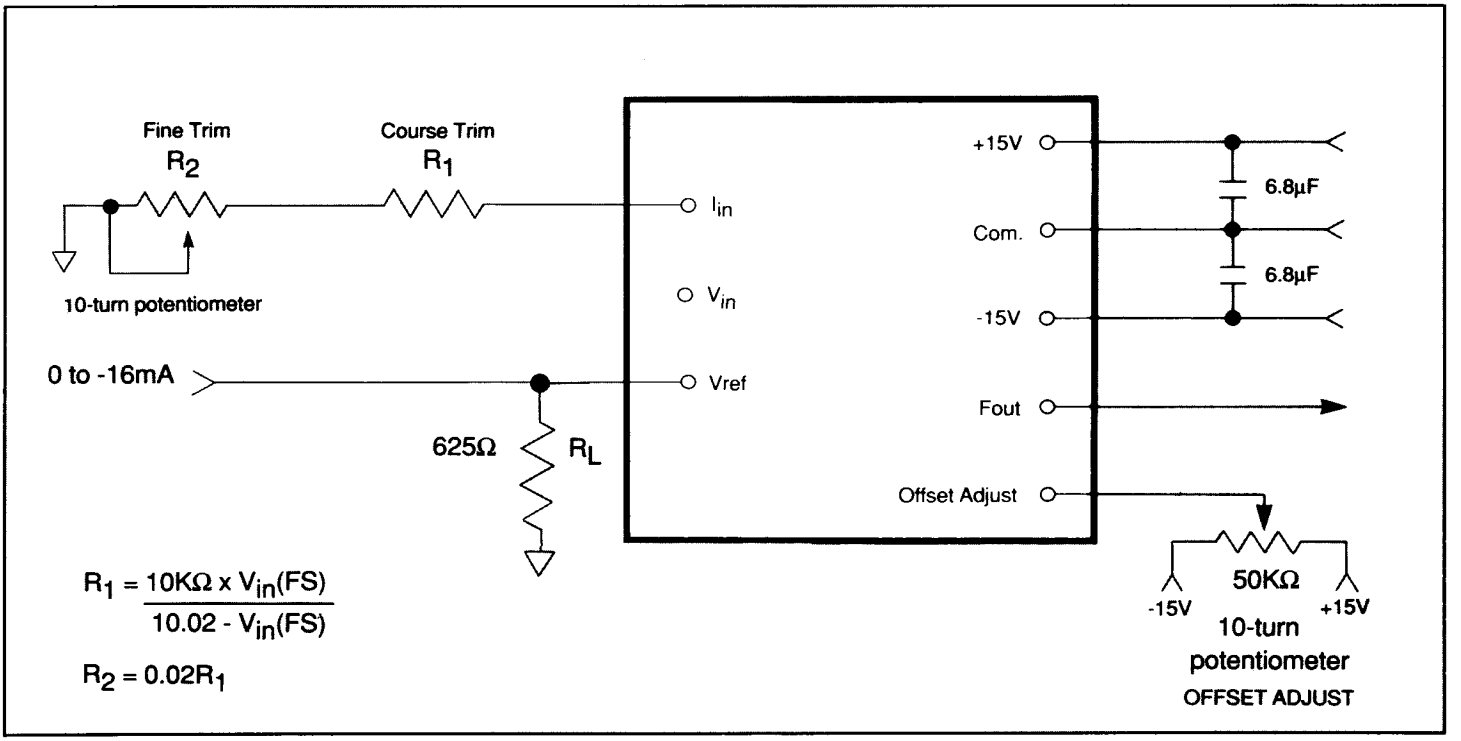


Figure 6. Negative Input Currents (8410-13 only)

Description (continued)

tions such as ratiometric operation, FET input opamp, or extended temperature range can also be accommodated. Please contact the factory to discuss your specific requirements.

The **8410 Series** are packaged in a 2.00" x 2.00" x 0.40" modular package. Power dissipation is less than 0.95W maximum, and operation to rated performance is over the 0°C to +70°C temperature range.

Using the 8410 Family of V/F Converters

General Considerations

Figure 2 depicts a typical circuit configuration for the **8410 Series**. The layout should be clean, with output pulses routed as far away from the input analog signals as possible. For maximum performance, bypass capacitors, as shown in Figure 2, should be mounted right at the appropriate pins of the **8410**.

For positive input signals, use the connections as shown. For negative input voltages, Vin should be grounded and the negative-going voltage should be connected to the Vref input.

Grounding

The Analog and Digital grounds are internally separate in the **8410 Series**. The use of ground plane is not necessary for proper operation; however, a ground plane is recommended with any analog signal conditioning circuitry that may be used in front of the V/F, especially if this circuitry involves high gains. Any amplifiers used in front of the **8410** should be decoupled to eliminate potential problems with the high frequency output of the V/F.

Offset and Gain Trimming

The OFFSET adjustment potentiometer should be a 50KΩ, 10-turn unit. With this pot in the circuit, initial offsets of up to ±10mV may be trimmed to zero.

The GAIN adjustment potentiometer should be a 200Ω, 10-turn unit with a recommended temperature coefficient of 100ppm or better. With this pot in the circuit, initial gain errors of up to ±2% may be trimmed to zero.

Offset and Gain Calibration

Offset Calibration

Offset calibration should be performed prior to gain calibration. With a +1mV analog signal at the inplut of the 8410 Series, adjust the OFFSET potentiometer until a frequency of 100Hz is observed on the output pin.

Gain Calibration

With a full scale analog input voltage of +10.00V, adjust the GAIN potentiometer until a full scale frequency of 1.000MHz is observed on the output pin.

Input Considerations Single-ended Inputs

The Vin pin accepts a 0V to +10V analog input, and has an impedance of 10KΩ. Figure 3 provides a recommended configuration for expanded or contracted input ranges.

High Impedance Inputs (8410 - 8413 only)

Figure 4 shows the input configuration for a high impedance, 0V to -10V input. This configuration is differential, referenced to the Vref input. An input of -10V will produce a

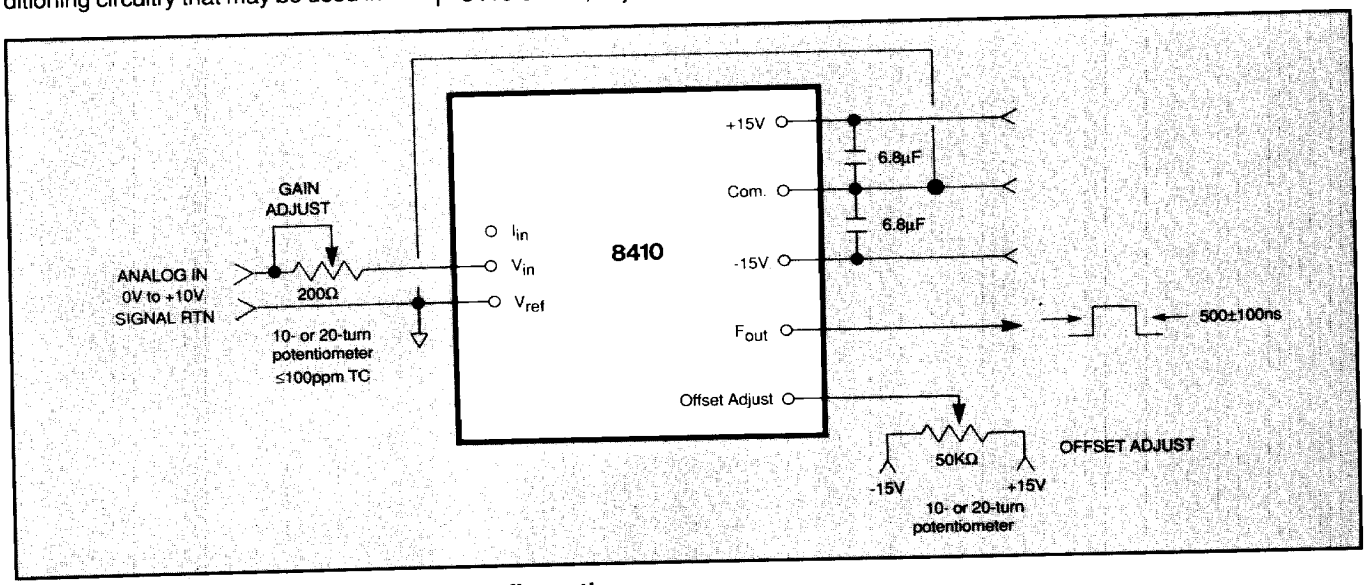
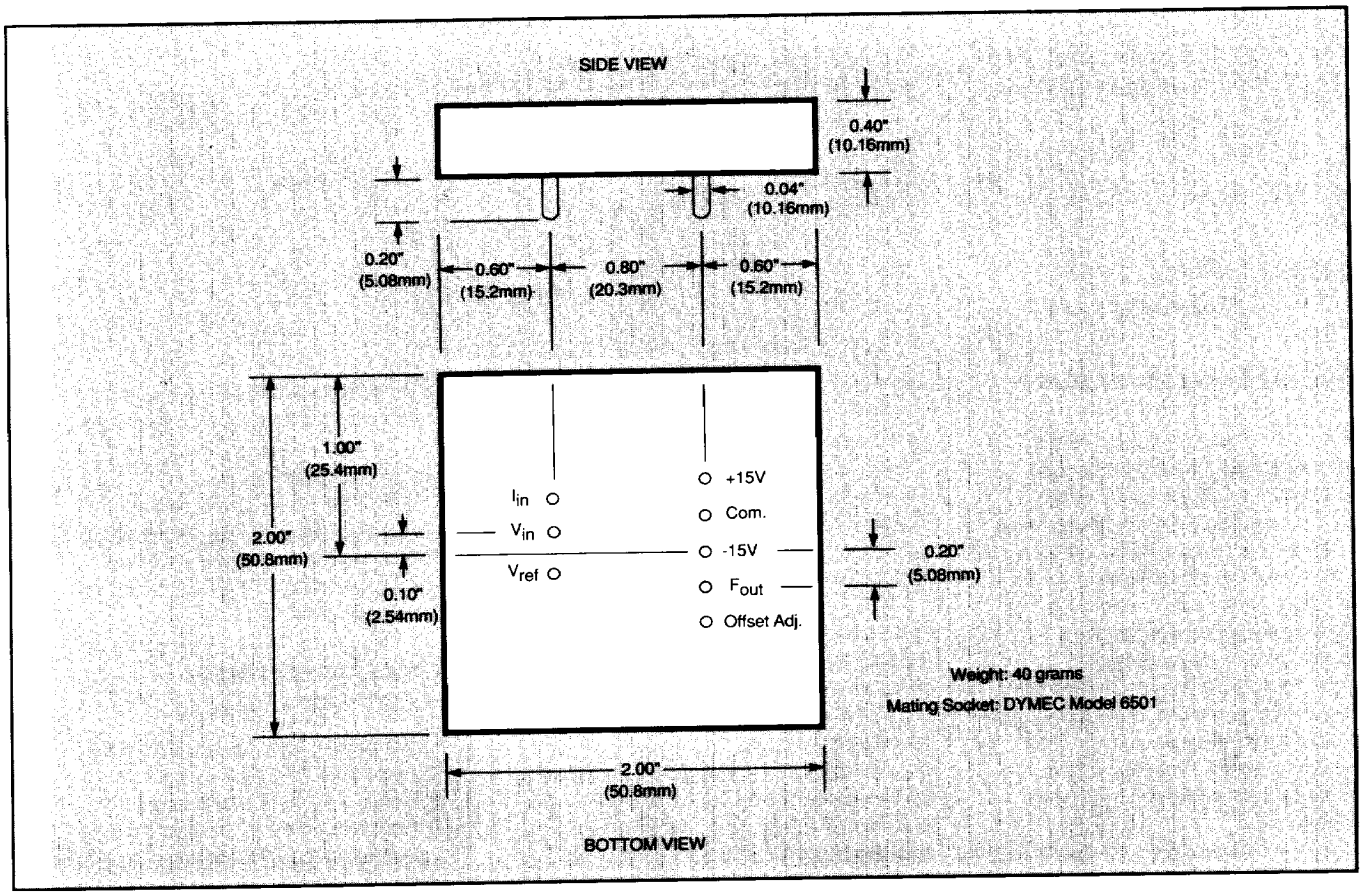


Figure 2. Normal 8410 Series Input Configuration

Mechanical Dimensions & Pinout



Mechanical Dimensions & Pinout

ORDERING INFORMATION

For Single-ended Input Configuration and:	Specify:
100ppm FS/°C maximum Gain Drift	**8410**
50ppm FS/°C maximum Gain Drift	**8411**
25ppm FS/°C maximum Gain Drift	**8412**
15ppm FS/°C maximum Gain Drift	**8413**

For Differential Input Configuration and:	Specify:
100ppm FS/°C maximum Gain Drift	**8414**
50ppm FS/°C maximum Gain Drift	**8415**
25ppm FS/°C maximum Gain Drift	**8416**
15ppm FS/°C maximum Gain Drift	**8417**

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Bulletin No. 86078410 REV.0

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