REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Convert to military drawing format. Change drawing CAGE code to 67268. Add vendor CAGE 01295. Minor changes to table I and table II. Editorial changes throughout. Add device type 05.	1987 OCT 13	
D	Deleted CAGE 01295. Editorial changes throughout. Made technical changes to table I, margin test method C (step 4), paragraph 4.3.1 (step C), table II, figure 5, paragraph 4.2, margin test method B (step 3), paragraph 1.2.2, paragraph 1.3, paragraph 1.4, figure 6, and table III. Added footnote 3, removed vendor name and address under vendor name and address, and added M38510/22403BYX to 8411104YX.	1989 JAN 11	

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	REV	D	D	D	D	C	C	C	C	D	D	D	D	D	D	D	D	D						
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17						

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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CHECKED BY: Ray Monnin

APPROVED BY:

DRAWING APPROVAL DATE: 18 OCTOBER 1984

REVISION LEVEL: D

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, 262,144 (32K X 8) UV ERASABLE PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	84111

SHEET 1 OF 17

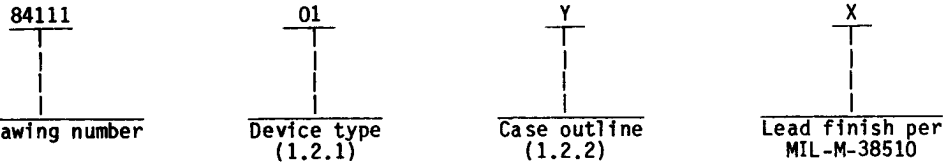
DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access
01	27256-35	32K X 8-bit UV EPROM	350 ns
02	27256-25	32K X 8-bit UV EPROM	250 ns
03	27256-20	32K X 8-bit UV EPROM	200 ns
04	27256-17	32K X 8-bit UV EPROM	170 ns
05	27256-30	32K X 8-bit UV EPROM	300 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Y	D-10 (28-pin, 1.490" x .610" x .232"), dual-in-line package 1/
Z	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier package 1/

1.3 Absolute maximum ratings.

Supply voltage (V_{CC}) 2/	-0.6 V dc to +6.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C
All input or output voltages with respect to ground	-0.6 V dc to +6.5 V dc
Voltage on pin A_9 with respect to ground	-0.6 V dc to +13.5 V dc
V_{PP} supply voltage with respect to ground	-0.6 V dc to +13.0 V dc

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ All voltages referenced to V_{SS}.

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Input low voltage (V_{IL})	-0.1 V dc to +0.8 V dc
Input high voltage (V_{IH})	2.0 V dc to V_{CC} +1 V dc
Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High level program input voltage $V_{IN(PR)}$	12.5 V dc ±0.3 V dc (program method B)

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{CC} = 5.50 V I_{OH} = -400 µA	1,2,3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 5.50 V I_{OL} = 2.1 mA	1,2,3	All		0.45	V
Output leakage current	I_{OL}	V_{CC} = 5.5 V V_{OUT} = 5.5 V	1,2,3	All		10	µA
High level input current 1/	I_{IH}	V_{CC} = 5.50 V, Outputs deselected V_{IN} = 5.50 V	1,2,3	All		10	µA
Vpp supply current read/standby 2/	I_{PP}	V_{PP} = 5.5 V	1,2,3	All		5	mA
Supply current (standby)	I_{CC1}	V_{CC} = 5.50 V, $\overline{CE}$ = V_{IH} Outputs open	1,2,3	All		50	mA
Supply current 2/	I_{CC2}	V_{CC} = 5.50 V, $\overline{OE}$ = $\overline{CE}$ = V_{IL} O_0-O_7 = 0 mA	1,2,3	01, 02, 03, 05 04		125 140	mA
Input capacitance 1/	C_I	V_{IN} = 0 V, f = 1 MHz T_C = +25°C, see 4.3.1c	4	All		6	pF
Output capacitance	C_O	V_{OUT} = 0 V, f = 1 MHz T_C = +25°C, see 4.3.1c	4	All		12	pF
Address access time	t_{AVQV}	V_{CC} = 5.50 V 1/ see figure 4 $\overline{CE}$ = $\overline{OE}$ = V_{IL}	9,10,11	01 02 03 04 05		350 250 200 170 300	ns
Chip enable access time	t_{ELQV}	$\overline{OE}$ = V_{IL}	9,10,11	01 02 03 04 05		350 250 200 170 300	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$		Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output enable data on time	t_{OLQV}	V_{CC} = 5.50 V 1/ see figure 4	$\overline{CE} = V_{IL}$	9,10,11	01		130	ns
					02		100	
					03		75	
					04		65	
					05		120	
Output enable to high Z	t_{EHQZ} 3/		$\overline{CE} = V_{IL}$	9,10,11	01		110	ns
					02		60	
					03		55	
					04		55	
					05		105	
Output hold from address change	t_{AXQX} 3/		$\overline{CE} = \overline{OE} = V_{IL}$	9,10,11	All	0		ns

1/ Outputs shall be loaded per figure 5.
2/ V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC2} and Ipp.
3/ Tested initially and after any design changes.

3.5 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4 herein.

3.5.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.5.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

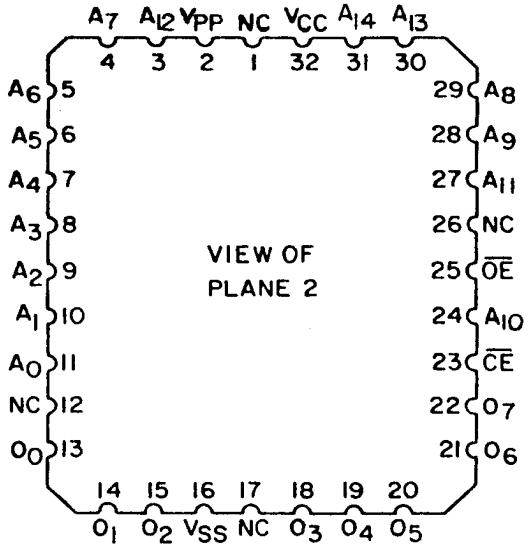
3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-833 (see 3.1 herein).

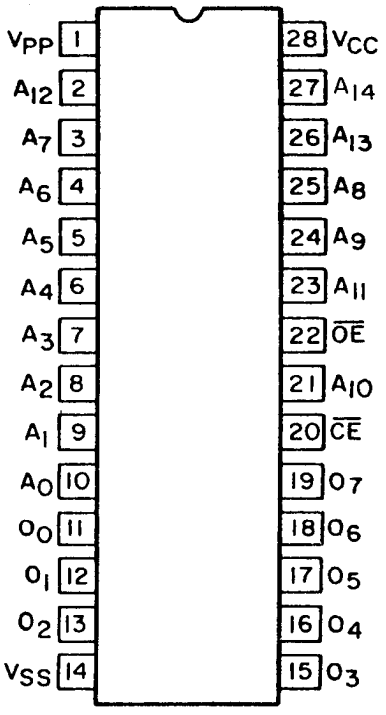
3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Case Z



OPTION A WITH ACTIVE TERMINALS ON PLANE 1.

Case Y



Pin Names

A_0-A_{14}	Addresses
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
O_{0-7}	Outputs

FIGURE 1. Terminal connections.

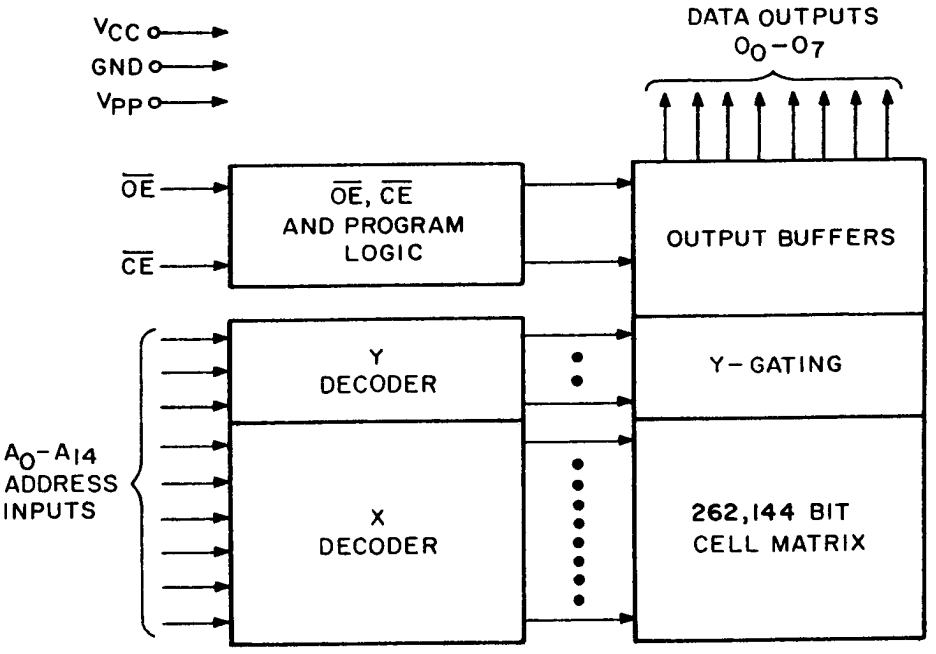
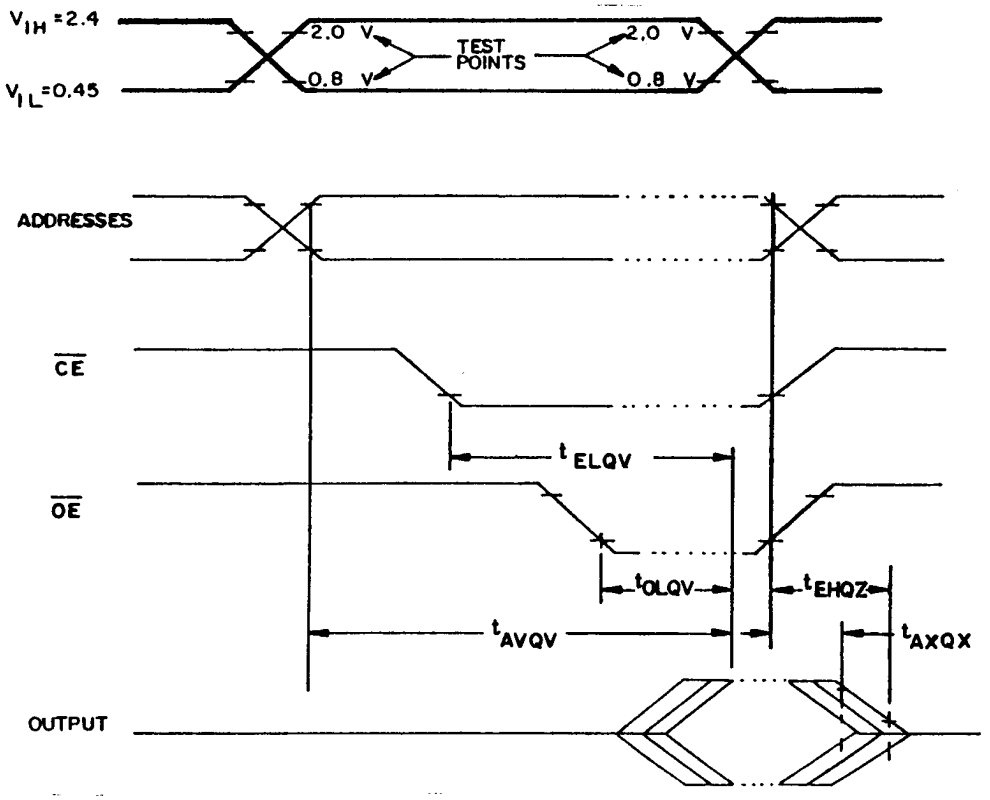


FIGURE 2. Block diagram.

Mode/pins	$\overline{CE}$	$\overline{OE}$	A_9	V_{PP}	V_{CC}	Outputs
Programming Method	B	B	B	B	B	B
Deselect Output disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Program Verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Intelligent Identifier	V_{IL}	V_{IL}	V_H	V_{CC}	V_{CC}	Code
Intelligent Programming	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}

NOTES:
1. It is recommended that verification for Method B devices be performed after the completion of programming all bytes.
2. X means the input is a "don't care".
3. Using the intelligent programming algorithm (Method B) allows the device to be programmed in a faster time.
4. V_H = 12 V±0.5 V.

FIGURE 3. Truth table.



NOTES:
1. $\overline{OE}$ may be delayed up to $t_{AVQV} - t_{OLQV}$ after falling edge of $\overline{CE}$ without impact on t_{AVQV}.
2. t_{EHQZ} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

FIGURE 4. Timing diagrams.

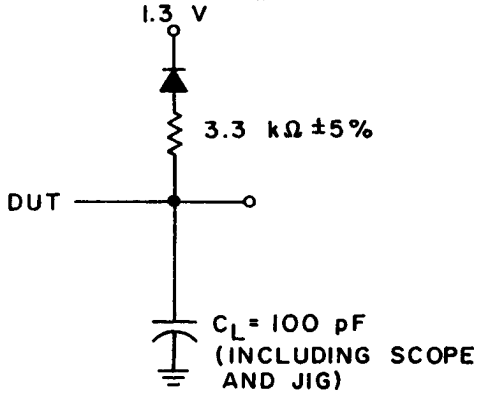


FIGURE 5. Output load circuit or equivalent.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

d. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2).

(2) Bake, unbiased, for 12 hours at +200°C.

(3) Perform a margin test using $V_m = V_{CC}$ = 6.0 V at +25°C using loose timing.

(4) Erase device, then program 45 to 50 percent of the bits to a worst case speed pattern.

(5) Perform dynamic burn-in (see 4.2a).

(6) Perform a margin test using $V_m = V_{CC}$ = 6.0 V at +25°C.

(7) Perform 100 percent electrical testing at +25°C, +125°C and -55°C.

(8) Erase device (see 3.5.1), except devices submitted for groups A, B, C, and D.

(9) Verify erasure (see 3.5.3).

Margin test method B

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = +6.0 V at +25°C using loose timing (i.e., t_{AVQV} = 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at V_m = 6.0 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.5.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.5.3).

Margin test method C

I. Wafer margin test method:

(1) Program at +25°C with a greater than 95 percent pattern, (example, all "0's").

(2) Measure V_{CCMAX} and store in die signature row.

(3) Unbiased bake for 2 hours at +250°C.

(4) Test at +25°C. Measure V_{CCMAX} and compare to V_{CCMAX} store in die. Any die with a delta greater than 0.66 V constitutes a failure and is removed from the lot.

II. Back end margin test method:

(1) Program at +25°C with a greater than 95 percent pattern (example, all "0's") (see 3.5.2).

(2) Test at +25°C (8.0 V), V_{CCMAX} range (6.0 V). Measure and record V_{CCMAX} in signature row.

(3) Unbiased bake for 32 hours at +200°C.

(4) Test at +25°C (see I, step 4 above).

(5) Erase (see 3.5.1).

(6) Program at +25°C with a 50 percent pattern (example checkerboard bar) (see 3.5.2).

(7) Test at +25°C (see 3.5.3)

(8) Burn-in (see 4.2a).

(9) Test at +25°C (see 3.5.3).

(10) Test at +125°C (see 3.5.3).

(11) Test at -55°C (see 3.5.3).

(12) Erase (see 3.5.1). Devices may be submitted for groups A, B, C, and D testing at this point.

(13) Verify erasure at +25°C (see 3.5.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurement) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 7, or 2, 8(Hot), 10

1/ (*) Indicates PDA applies to subgroup 1 (see 4.2).
2/ Any or all subgroups may be combined when using a high speed tester.
3/ Subgroups 7 and 8 shall consist of verifying the pattern specified.
4/ For all electrical tests, the device shall be programmed to the pattern specified.
5/ (**) See 4.3.1c.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

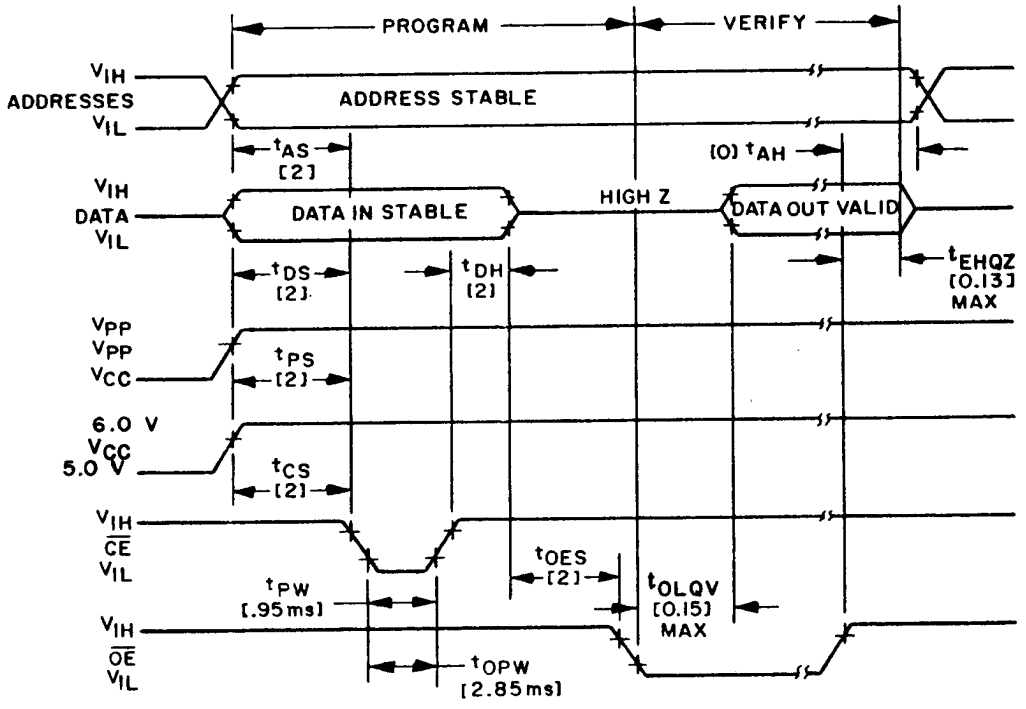
4.4 Erasing procedure. The device is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 W-s/cm^2. An example of an ultraviolet source which can erase the device in 30 minutes is the model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about 1 inch away from the lamp tubes. After erasure, all bits are in the high state.

4.5 Programming procedures for method B. The programming characteristics in table III and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration for programming. The waveforms of figure 6 and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

c. Programming occurs when V_{pp} is 12.5 V ±0.3 V and chip enable is brought low.



NOTES:
1. All times shown in are minimum and in µs unless otherwise specified.
2. The input and output timing reference level is 0.8 V for a V_{IL} and 2 V for V_{IH}.
3. t_{OLOV} and t_{EHQZ} are characteristics of the device but must be accommodated by the programmer.
4. When programming a 0.1 µF capacitor is required accross V_{PP} and ground to suppress spurious voltage transients which can damage the device.

FIGURE 6. Programming timing diagram for method B.

TABLE III. Programming characteristics for method B.

Test	Symbol	Conditions 1/ V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V T_A = +25°C	Limits		Unit
			Min	Max	
Input current (all inputs)	I_{IN}	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
Input low level (all inputs)	V_{IL}		-0.1	0.8	V
Input high level	V_{IH}		2.0	V_{CC}-1	V
Output low voltage during verify	V_{OL}	I_{OL} = 2.1 mA		0.45	V
Output high voltage during verify	V_{OH}	I_{OH} = -400 µA	2.4		V
V_{CC} supply current (program and verify)	I_{CC}			125	mA
V_{PP} supply current (program)	I_{PP}	$\overline{CE} = V_{IL}$		50	mA
A_9 intelligent identifier voltage	V_{ID}		11.5	12.5	V
Address setup time	t_{AS}		2		µs
$\overline{OE}$ setup time	t_{OES}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		0		µs
Data hold time	t_{DH}		2		µs
Output enable to output float delay	t_{EHQZ}		0	130	ns
V_{PP} setup time	t_{PS}		2		µs

See footnotes at end of table.

TABLE III. Programming characteristics for method B - Continued.

Test	Symbol	Conditions 1/ V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V T_A = +25°C	Limits		Unit
			Min	Max	
V_{CC} setup time	t_{CS}		2		µs
$\overline{CE}$ initial program pulse width	t_{PW}	2/	0.95	1.05	ms
$\overline{CE}$ overprogram pulse width	t_{OPW}	3/	2.85	78.75	ms
Data valid from $\overline{OE}$	t_{OLQV}			150	ns

1/ V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2/ Initial program pulse width tolerance is 1 ms ±5%.
3/ The length of the overprogram pulse may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/2240XBYX.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number	Program method	Margin test method
8411101YX	34649	MD27256-35/B		B	B
	34335	AM27256-35/BXA		B	A
8411101ZX	34649	MR27256-35/B		B	B
	34335	AM27256-35/BUA		B	A
8411102YX 2/	34649	MD27256-25/B	M38510/22401BYX	B	B
	34335	AM27256-25/BXA		B	A
	3/	SMJ27256-25JM		B	C
8411102ZX	34649	MR27256-25/B		B	B
	34335	AM27256-25/BUA		B	A
8411103YX 2/	34649	MD27256-20/B	M38510/22402BYX	B	B
	34335	AM27256-20/BXA		B	A
	3/	SMJ27256-20JM		B	C
8411103ZX	34649	MR27256-20/B		B	B
	34335	AM27256-20/BUA		B	A
8411104YX	34649	MD27256-17/B	M38510/22403BYX	B	B
8411105YX	3/	SMJ27256-30JM		B	C

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Inactive for new design. Use M38510/2240XBYX.

3/ Not available from approved source.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Incorporated 901 Thompson Place Sunnyvale, CA 94088
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051

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