

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Convert to military drawing format. Add vendor CAGE 01295. Changes to table I. Delete subgroup 9 from final electrical test parameters. Add case outline X. Added four devices 09 through 12.	1987 JUL 06	<i>M.d. Lge</i>
D	Update part numbers for vendor CAGE number 01295. Correction on page 18, terminal connections. Editorial changes throughout. Add vendor CAGE number 01295 as a supplier of the K package for device types 01 through 08. Changes to pages 5 and 6 table I. Changes to pages 10 and 11 terminal connections. Changes on pages 21-28.	1988 MAY 06	<i>M.d. Lge</i>

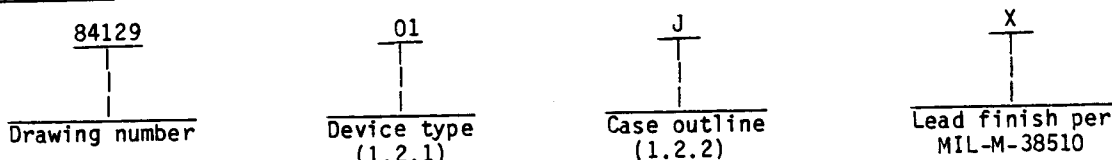
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DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall be as follows:

Device type	Generic number	Circuit
01, 09	PAL20L8A, L8A-2	20-input 8-output AND-OR invert gate array
02, 10	PAL20R8A, R8A-2	20-input 8-output registered AND-OR gate array
03, 11	PAL20R6A, R6A-2	20-input 6-output registered AND-OR gate array
04, 12	PAL20R4A, R4A-2	20-input 4-output registered AND-OR gate array
05	PAL20L10A	20-input 10-output AND-OR invert gate array
06	PAL20X8A	20-input 8-output registered AND-OR-XOR gate array
07	PAL20X10A	20-input 10-output registered AND-OR-XOR gate array
08	PAL20X4A	20-input 4-output registered AND-OR-XOR gate array

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-lead, 1.290" x .610" x .225"), dual-in-line package
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
X	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package 1/
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package 1/

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	- - - - -	-0.5 V dc to +12.0 V dc
Input voltage range	- - - - -	-1.5 V dc to +5.5 V dc
Storage temperature range	- - - - -	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	- - - - -	+260°C
Thermal resistance, junction-to-case (θ_{JC}): 2/ 3/ Cases J, K, L, X, and 3	- - - - -	(See MIL-M-38510, appendix C)
Output voltage applied	- - - - -	-1.5 V dc to +12 V dc
Output sink current	- - - - -	100 mA
Maximum power dissipation (P_D) 3/	- - - - -	1.2 W
Maximum junction temperature (T_J)	- - - - -	+175°C

1/ See figure 1.

2/ Heat sinking is recommended to reduce the junction temperature.

3/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

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1.4 Recommended operating conditions.

Supply voltage (V_{CC})	- - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	- - - - -	2.0 V dc
Maximum low level input voltage (V_{IL})	- - - - -	0.8 V dc
Case operating temperature range (T_C)	- - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth tables for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.2.2 Programmed devices. The truth tables for programmed devices shall be as specified by an attached altered item drawing.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $\frac{1}{-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}}$	Group A sub-groups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V_{IC}	$V_{CC} = 4.5 \text{ V}, I_I = -18 \text{ mA}$	1	A11		-1.5	V
High level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V}, V_{IL} \leq 0.8 \text{ V}, V_{IH} \geq 2.0 \text{ V}, I_{OH} = -2 \text{ mA}$	1,2,3	A11	2.4		V
Low level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}, V_{IL} \leq 0.8 \text{ V}, V_{IH} \geq 2.0 \text{ V}, I_{OL} = 12 \text{ mA}$	1,2,3	A11		0.5	V
High level input voltage	V_{IH}	$V_{CC} = 5.5 \text{ V } \underline{2/}$	1,2,3	A11	2.0		V
Low level input voltage	V_{IL}	$V_{CC} = 5.5 \text{ V } \underline{2/}$	1,2,3	A11		0.8	V
High level input current	I_{IH}	$V_{CC} = 5.5 \text{ V}, V_I = 2.4 \text{ V } \underline{3/}$	1,2,3	A11		40	μA
		$\overline{OE}$ others				25	
Low level input current	I_{IL}	$V_{CC} = 5.5 \text{ V}, V_I = 0.4 \text{ V } \underline{3/}$	1,2,3	A11		-0.25	mA
Output short circuit current	I_{OS}	$V_{CC} = 5.5 \text{ V}, V_O = .5 \text{ V } \underline{4/}$	1,2,3	01-08 09,10, 11,12	-30	-250	mA
						-130	
Input current	I_I	$V_{CC} = 5.5 \text{ V}, V_I = 5.5 \text{ V}$	1,2,3	A11		1.0	mA
Off-state output current	I_{OZL}	$V_{CC} = 5.5 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{IH} = 2.4 \text{ V}, V_O = 0.4 \text{ V } \underline{3/}$	1,2,3	A11		-250	μA
Off-state output current	I_{OZH}	$V_{CC} = 5.5 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{IH} = 2.4 \text{ V}, V_O = 2.4 \text{ V } \underline{3/}$	1,2,3	A11		100	μA
Supply current	I_{CC}	$V_{CC} = 5.5 \text{ V}$	1,2,3	01,02, 03,04		210	mA
				05		165	
				06,07, 08		180	
				09,10, 11,12		105	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _C ≤ +125°C	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay data input to output	t _{PHL}	V _{CC} = 5.0 V, C _L = 50 pF ±10%, R ₁ = 390Ω, ±5%, R ₂ = 750Ω ±5% (or equivalent load circuit) Unless otherwise specified	9,10,11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		50	
Propagation delay data input to output	t _{PLH}		9,10,11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		50	
Propagation delay high impedance to output high	t _{PZH}		9, 10, 11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		45	
Propagation delay high impedance to output low	t _{PZL}		9,10,11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		45	
Propagation delay output high to high impedance ^{5/}	t _{PHZ}		9,10,11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		45	
Propagation delay output low to high impedance ^{5/}	t _{PLZ}		9,10,11	01,03, 04		30	ns
				05,06, 08		35	
				09,11, 12		45	
Propagation delay high impedance to output high OE to all output pins	t _{PZH}		9,10,11	02,03, 04,06, 07,08, 10,11, 12		25	ns
Propagation delay high impedance to output low OE to all output pins	t _{PZL}		9,10,11	02,03, 04,06, 07,08, 10,11, 12		25	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $\frac{1}{-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}}$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay output high to high impedance OE to all output pins <u>5/</u>	t _{PHZ}	V _{CC} = 5.0 V, C _L = 50 pF ±10%, R ₁ = 390Ω, ±5%, R ₂ = 750Ω, ±5% (or equivalent load circuit) Unless otherwise specified	9,10,11	02,03, 04,06, 07,08, 10,11, 12		25	ns
Propagation delay output low to high impedance OE to all output pins <u>5/</u>	t _{PLZ}		9,10,11	02,03, 04,06, 07,08, 10,11, 12		25	ns
Clock to output	t _{PCH}		9,10,11	02,03, 04		20	ns
	t _{PCL}			06,07, 08,09, 10,11, 12		25	
Minimum clock pulse width	t _p (CL)		9,10,11	02,03, 04	20		ns
				06,07, 08	35		
				09,10, 11,12	25		
Minimum setup time <u>2/</u>	t _{su}		9,10,11	02,03, 04	30		ns
				06,07, 08	40		
				09,10, 11,12	50		
Minimum hold time <u>2/</u>	t _H		9,10,11	02,03, 04,06, 07,08, 09,10, 11,12	0		ns
Maximum clock frequency <u>2/</u>	f _{MAX}		9,10,11	02,03, 04	20		MHz
				06,07, 08,09, 10,11, 12	15.3		

1/ Unless otherwise specified V_{CC} is 4.5 V to 5.5 V.2/ Tested only initially and after any design change, or used as setup condition, therefore guaranteed if not tested.3/ I/O terminal leakage is the worst case of I_{IX} or I_{OZX}.4/ Only one output shorted at a time.5/ C_L = 5 pF.**STANDARDIZED
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3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.9 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.9.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.9.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

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4.3.1 Group A inspection.

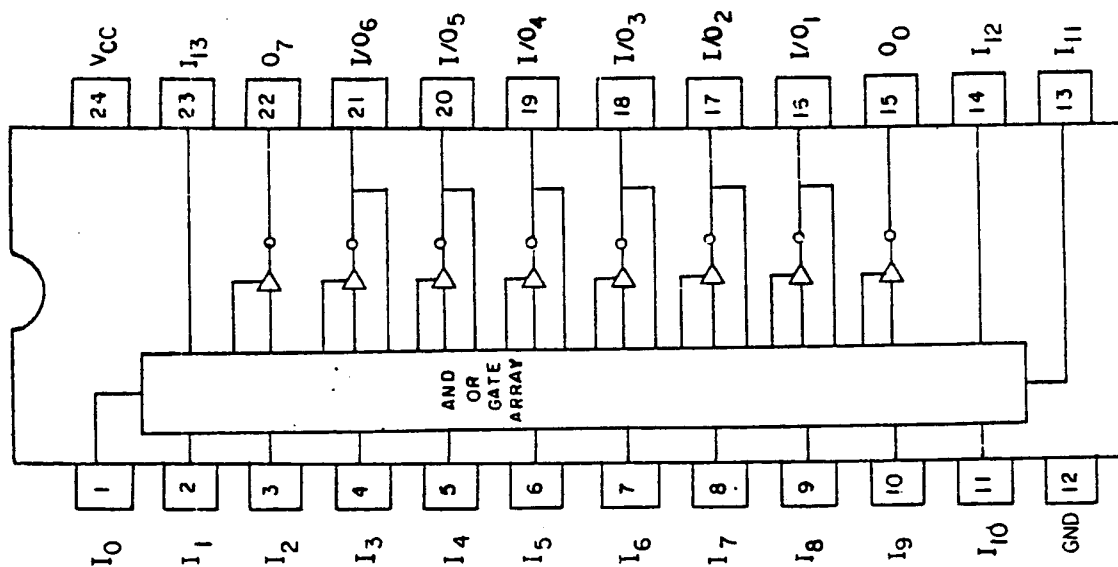
- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroup 9. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowed.
- d. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of group A, subgroup 9. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the same may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883:
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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Device types 01 and 09
Cases J, K, and L



Device types 01 and 09
Case 3

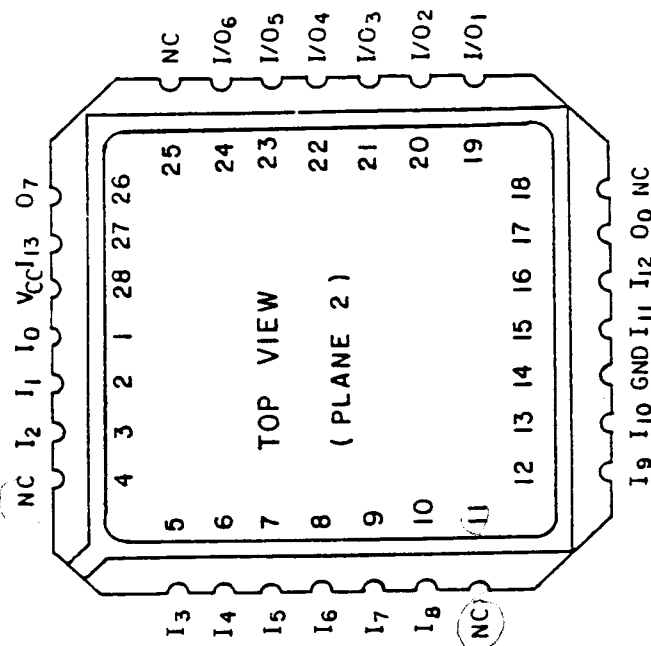


FIGURE 1. Terminal connections.

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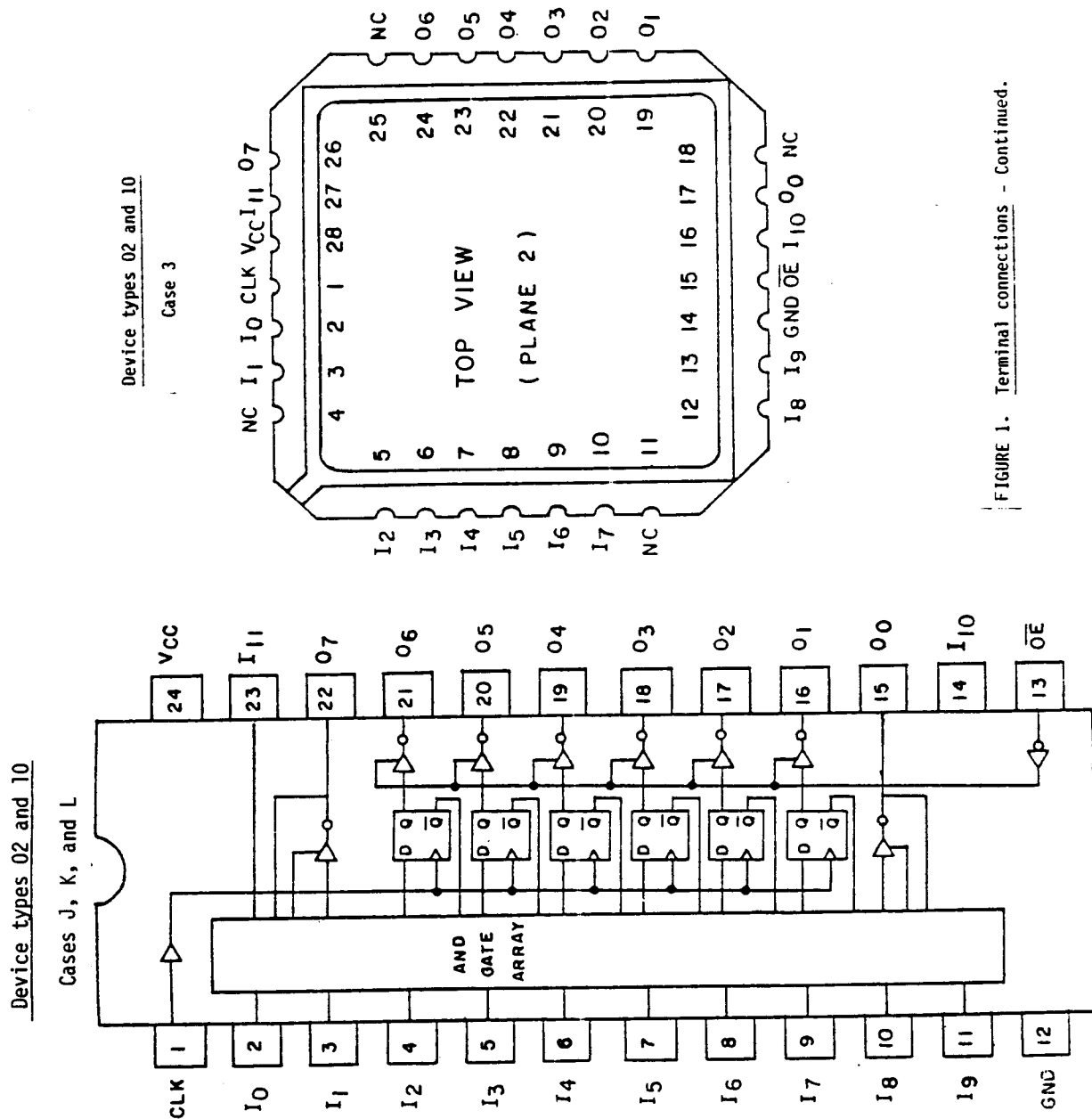
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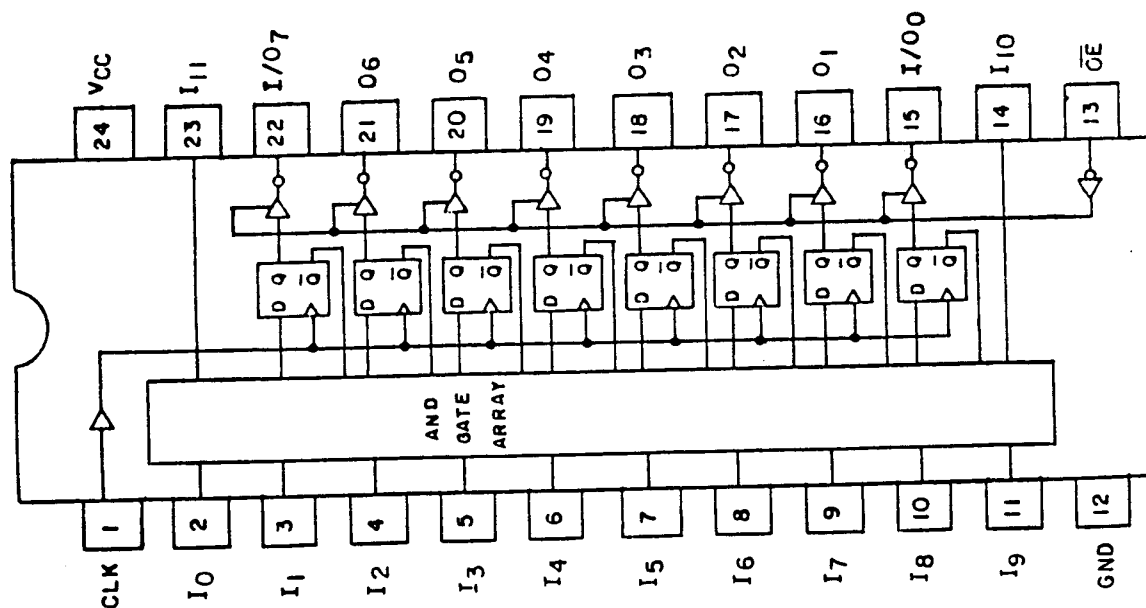
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Cases J, K, and L



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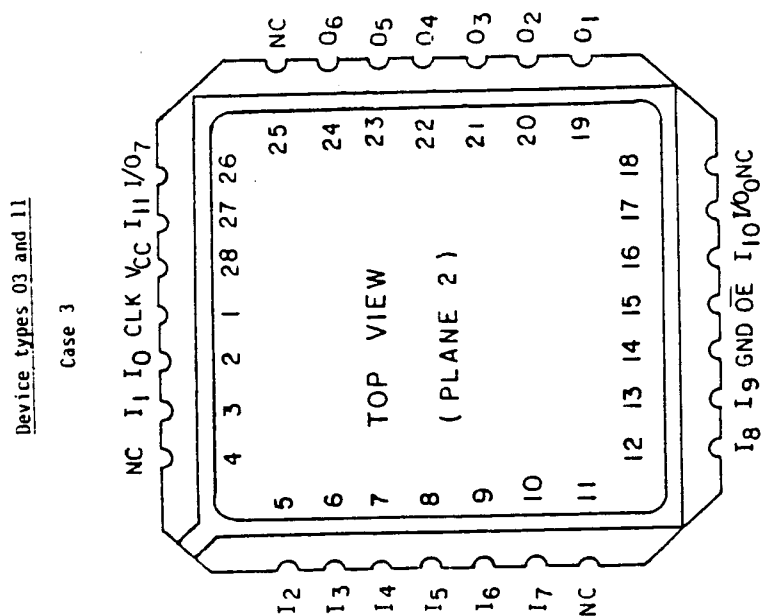
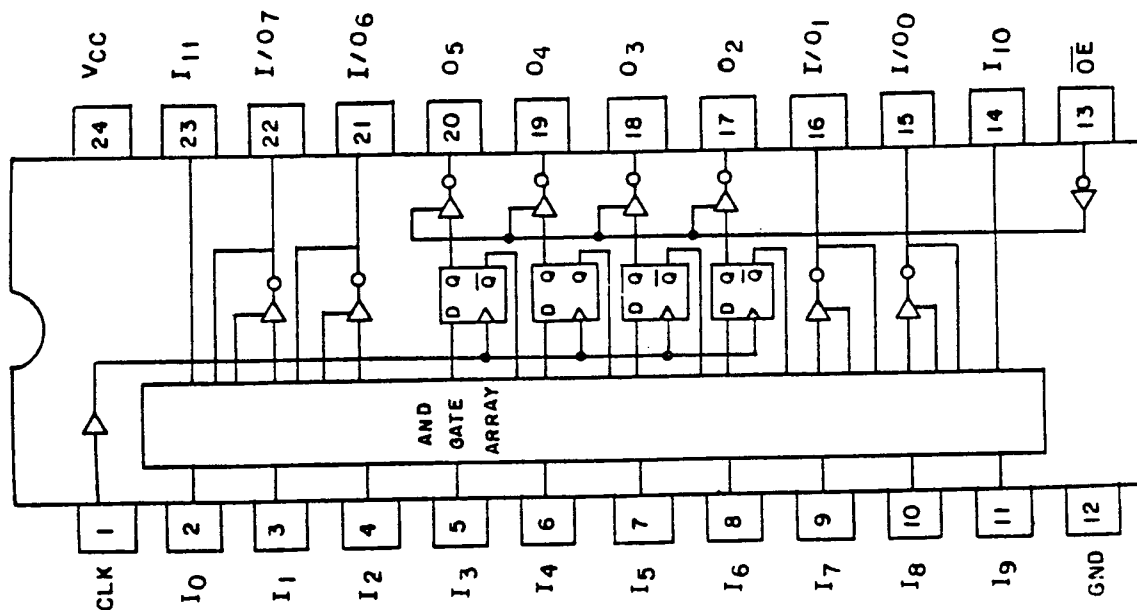


FIGURE 1. Terminal connections - Continued.

Device types 04 and 12
Cases J, K, and L



Device types 04 and 12
Case 3

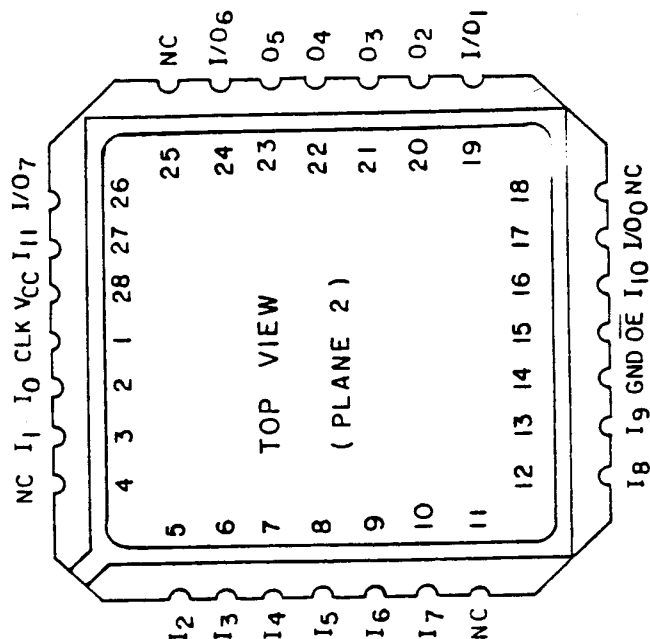


FIGURE 1. Terminal connections - Continued.

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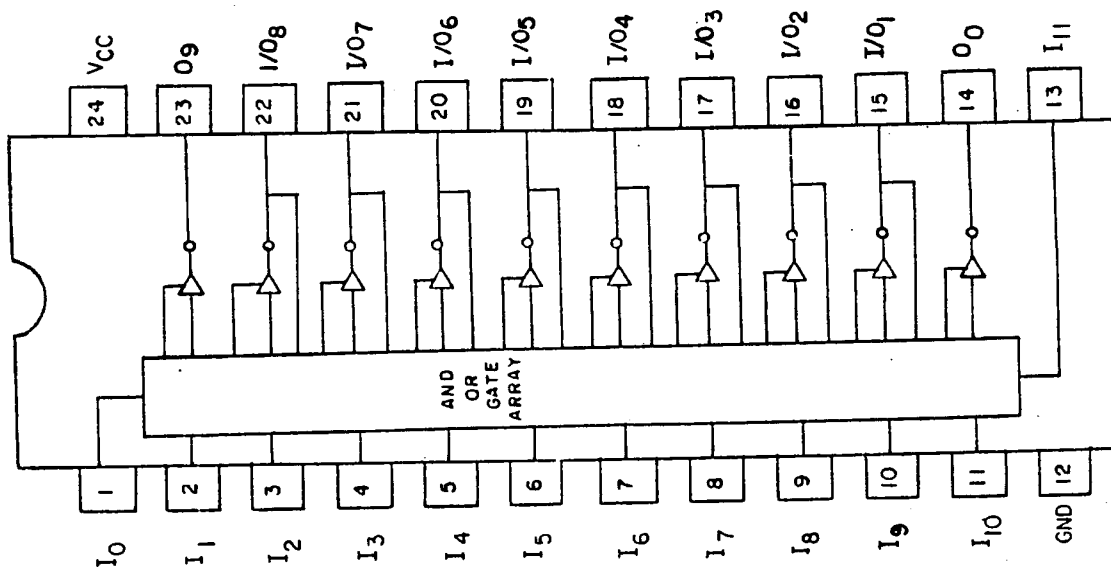
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Device type 05
Cases K and L



Device type 05
Case 3

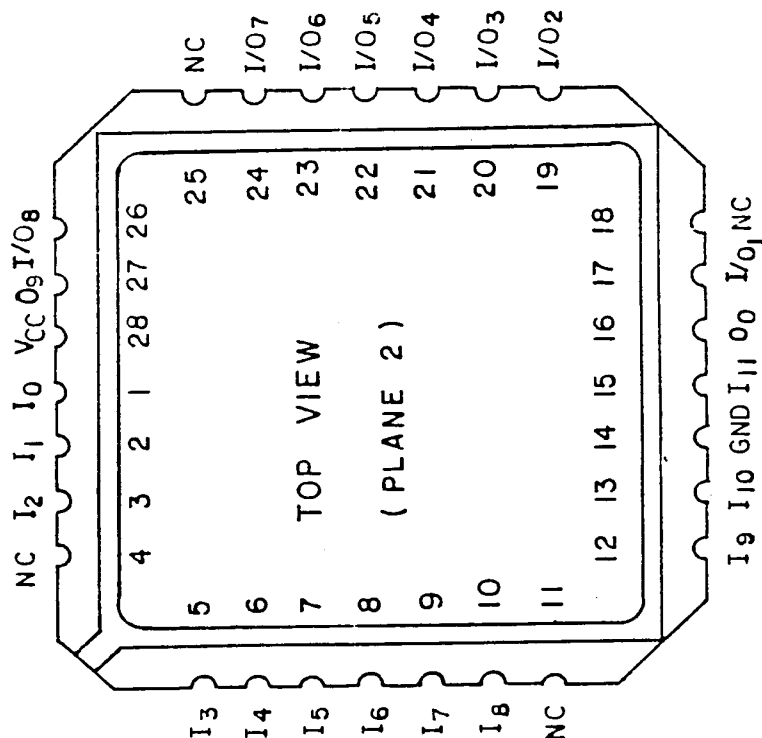


FIGURE 1. Terminal connections - Continued.

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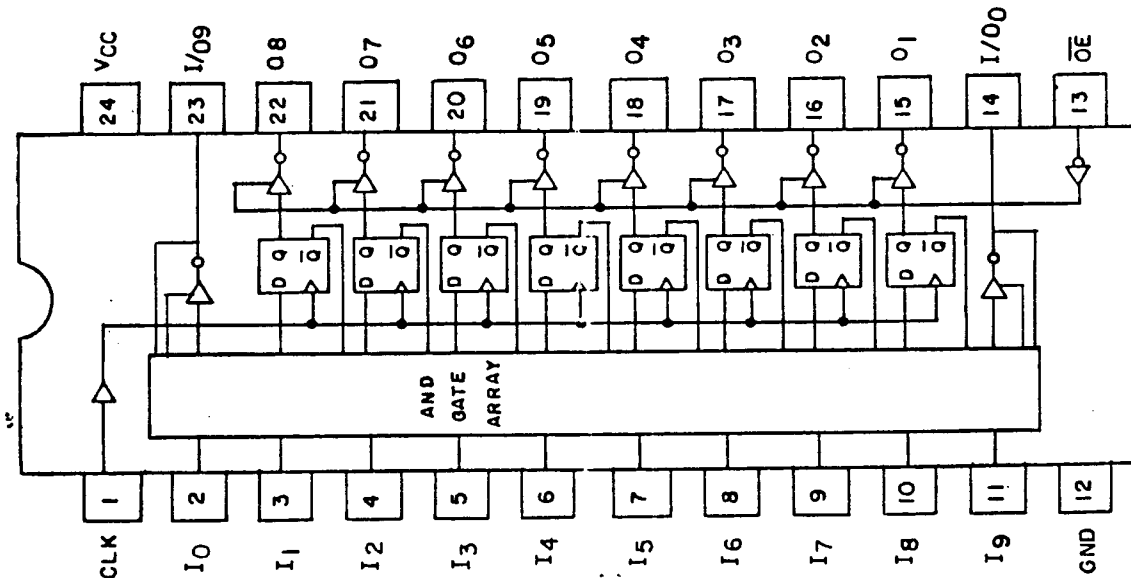
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Device type 06

Cases K and L



Device type 06

Case 3

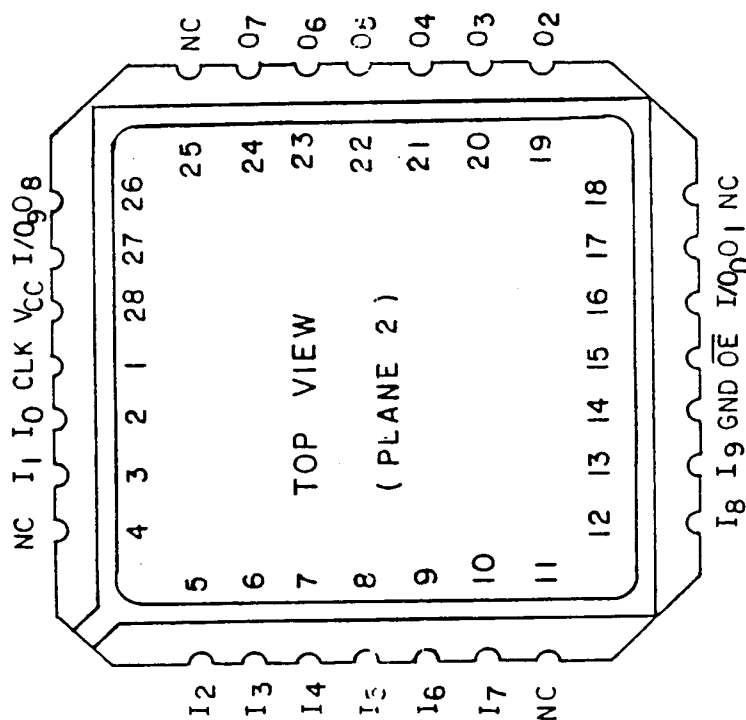


FIGURE 1. Terminal connections - Continued.

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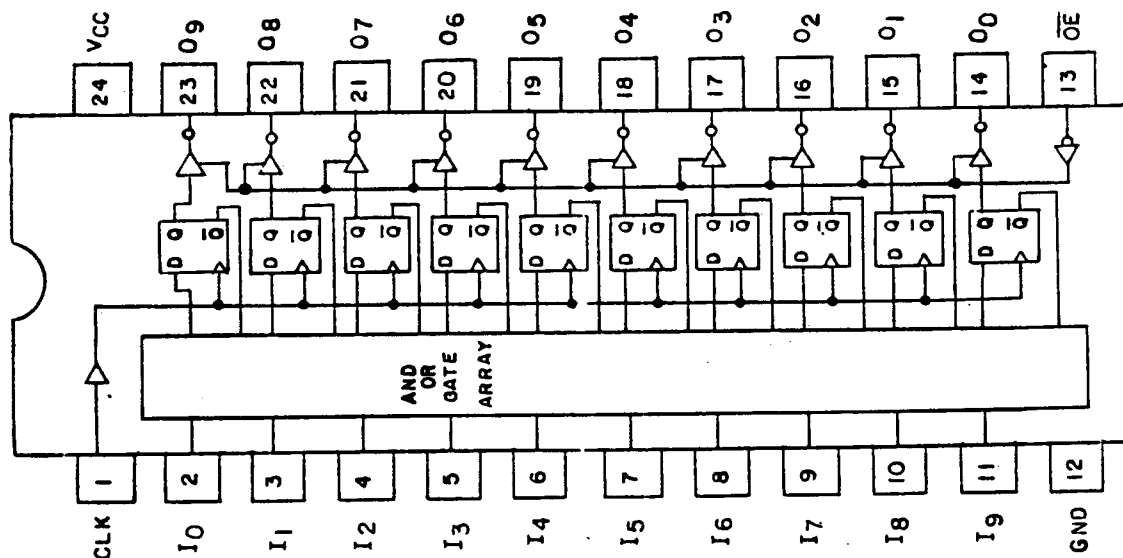
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Device type 07
Cases K and L



Device type 07

Case 3

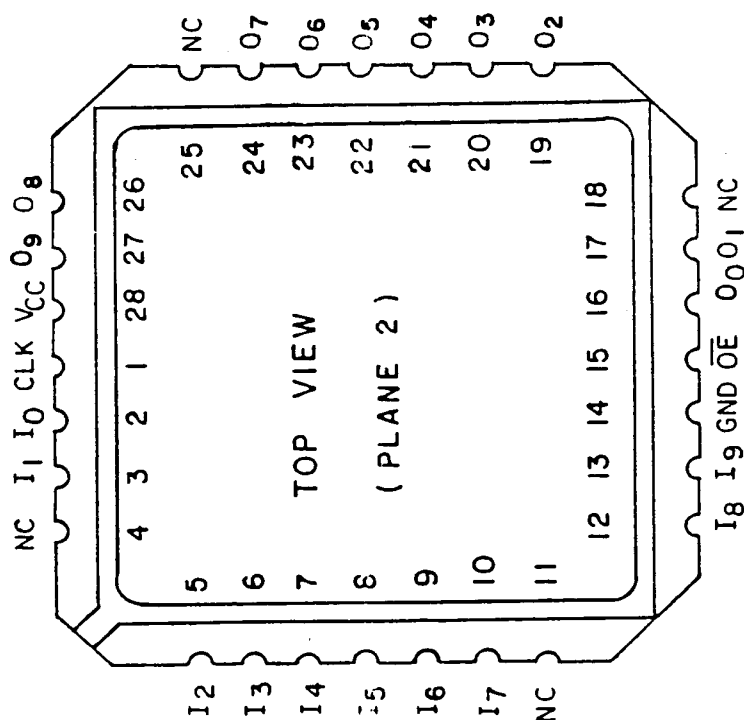


FIGURE 1. Terminal connections - Continued.

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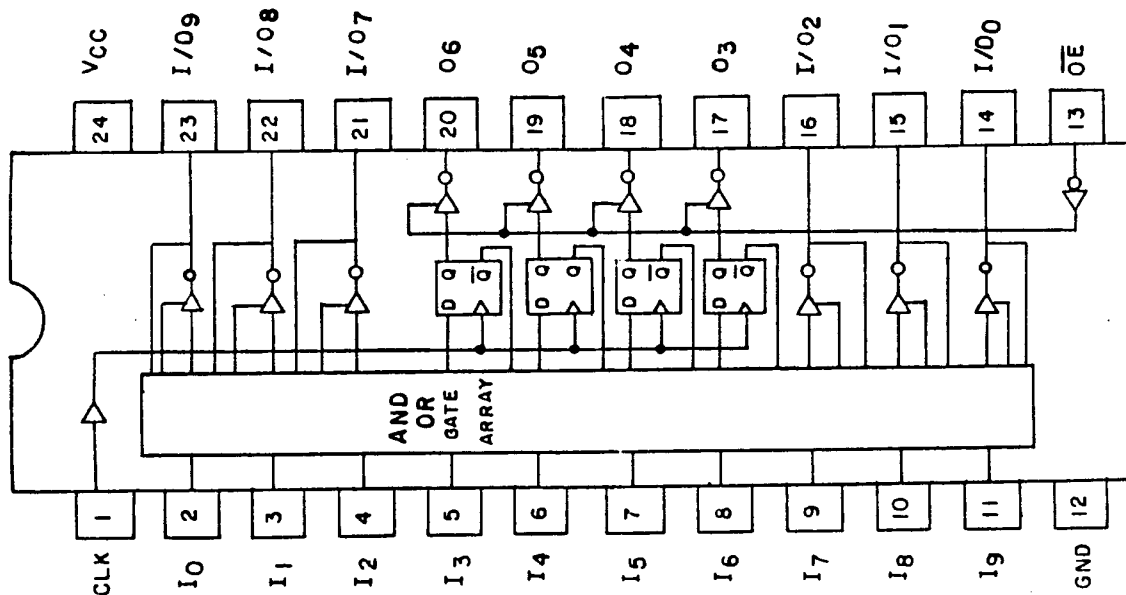
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Device type 08

Cases K and L



Device type 08

Case 3

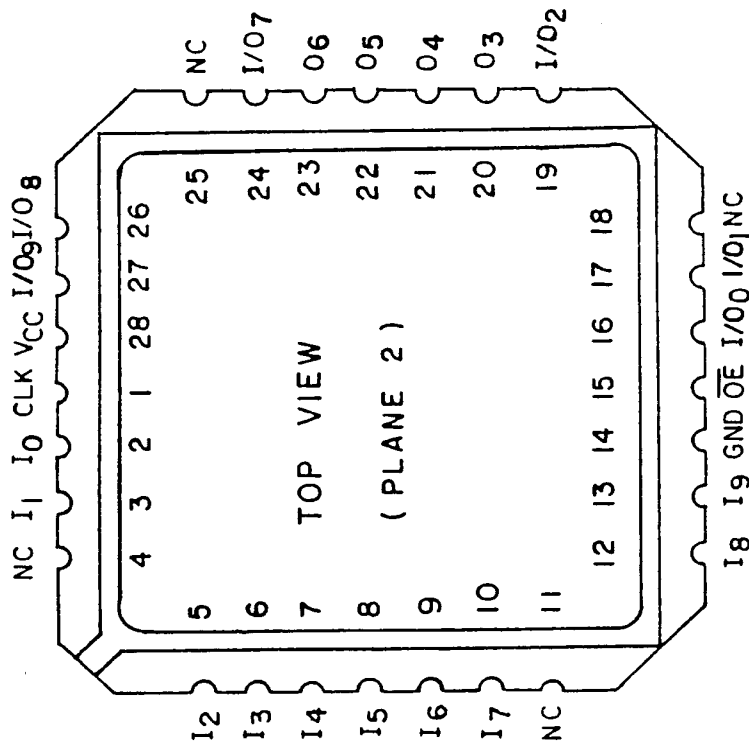


FIGURE 1. Terminal connections - Continued.

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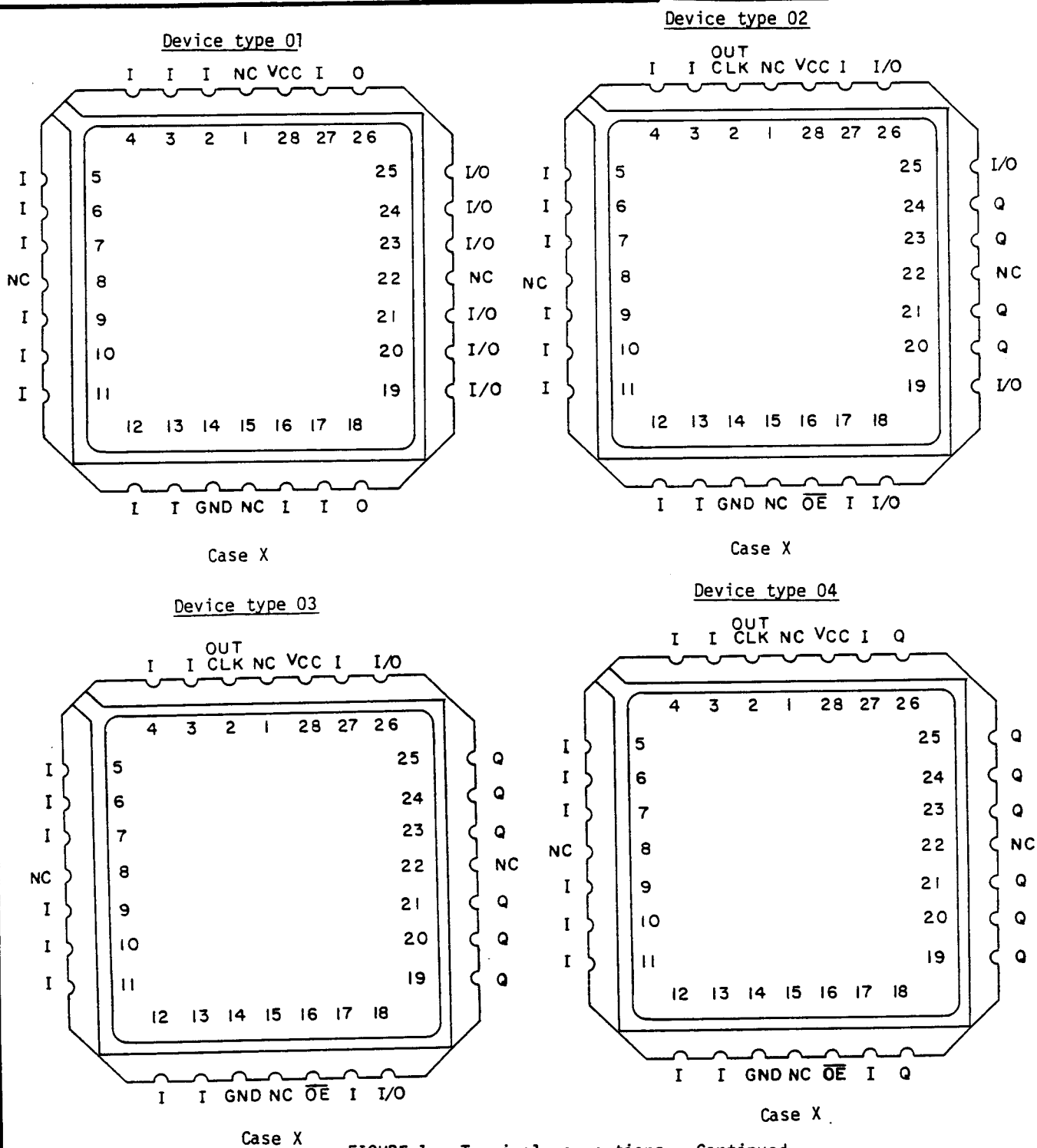
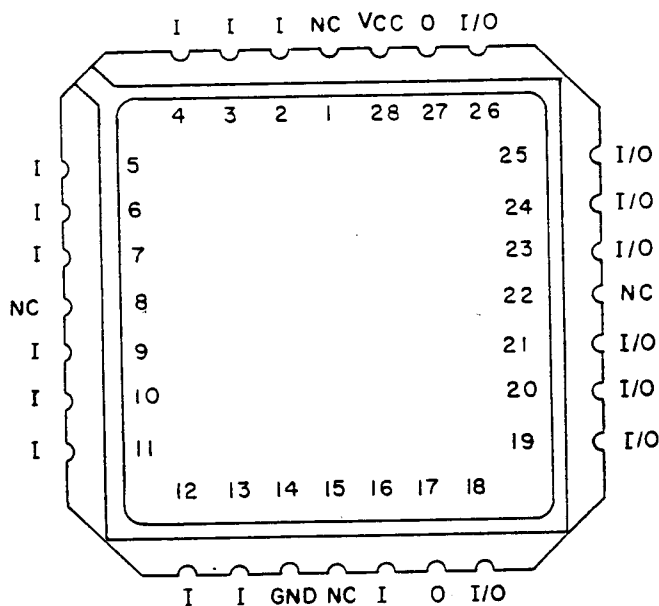


FIGURE 1. Terminal connections - Continued.

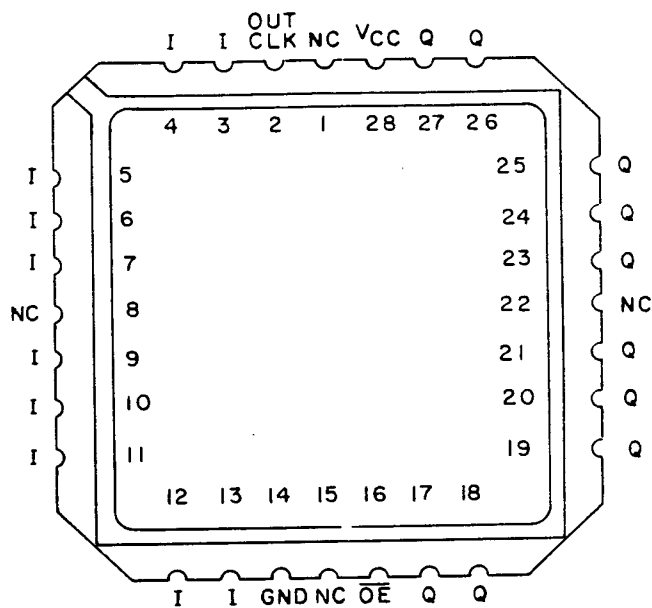
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Device type 05



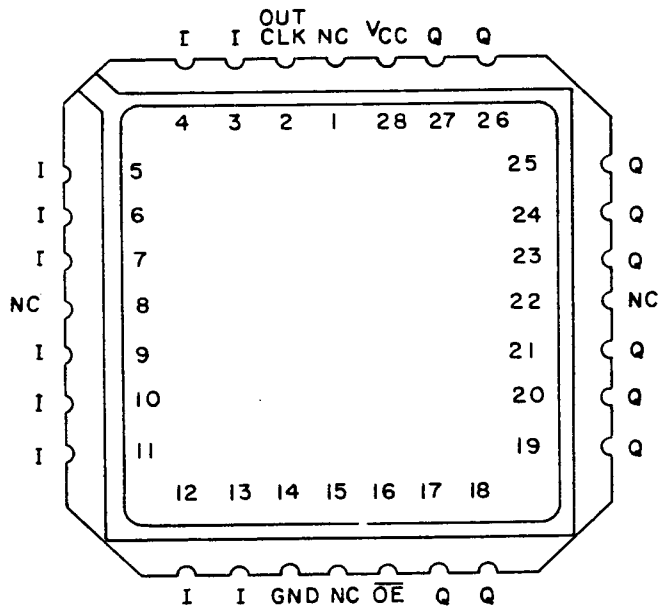
Case X

Device type 06



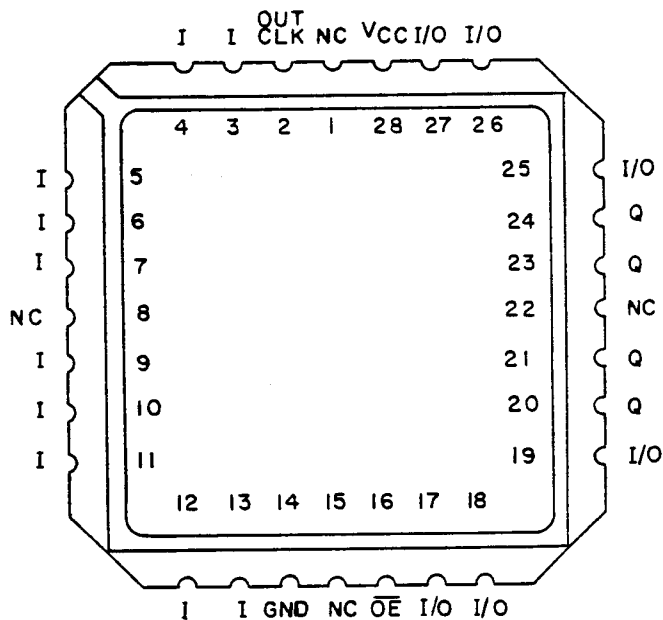
Case X

DEVICE TYPE 07



Case X

Device type 08



Case X

FIGURE 1. Terminal connections - Continued.

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Device types 01 and 09

INPUTS														OUTPUTS							
I ₁₃	I ₁₂	I ₁₁	I ₁₀	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	O ₇	I/O ₆	I/O ₅	I/O ₄	I/O ₃	I/O ₂	I/O ₁	O ₀
X	X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z

Device types 02 and 10

INPUTS														OUTPUTS							
$\overline{OE}$	I ₁₁	I ₁₀	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	CLK	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₀
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	H	H	H	H	H	H	H	H

Device types 03 and 11

INPUTS														OUTPUTS							
$\overline{OE}$	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	CLK	I/O_7	O_6	O_5	O_4	O_3	O_2	O_1	I/O_0
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK.	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	H	H	H	H	H	H	Z

Device types 04 and 12

INPUTS														OUTPUTS							
$\overline{OE}$	I ₁₁	I ₁₀	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	CLK	I/O ₇	I/O ₆	O ₅	O ₄	O ₃	O ₂	I/O ₁	I/O ₀
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	H	H	H	H	Z	Z

FIGURE 2. Truth tables (unprogrammed).

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Device type 05

Inputs												Outputs									
I ₁₁	I ₁₀	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	O ₉	I/O ₈	I/O ₇	I/O ₆	I/O ₅	I/O ₄	I/O ₃	I/O ₂	I/O ₁	O ₀
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Device type 06

Inputs												Outputs									
$\overline{OE}$	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	CLK	I/O ₉	O ₈	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	I/O ₀
H	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	CLK	Z	H	H	H	H	H	H	H	H	Z

Device type 07

Inputs												Outputs									
$\overline{OE}$	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	CLK	O ₉	O ₈	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₀
H	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	CLK	H	H	H	H	H	H	H	H	H	H

Device type 08

Inputs												Outputs									
$\overline{OE}$	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	CLK	I/O ₉	I/O ₈	I/O ₇	O ₆	O ₅	O ₄	O ₃	I/O ₂	I/O ₁	I/O ₀
H	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	H	H	H	H	Z	Z	Z

FIGURE 2. Truth tables (unprogrammed) - Continued.

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Device types 01 and 09

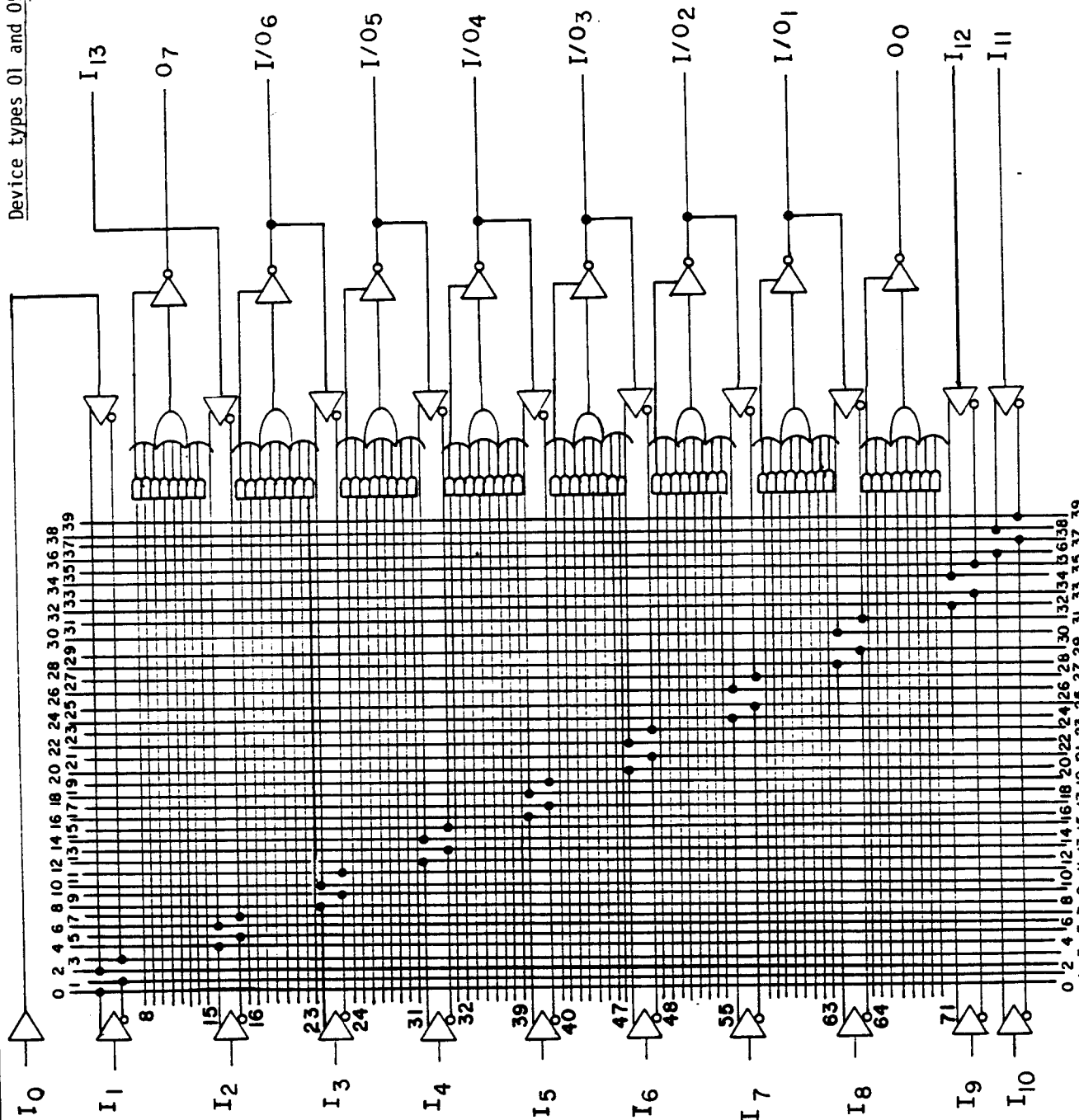


FIGURE 3. (Unprogrammed) Logic diagrams.

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Device types 02 and 10

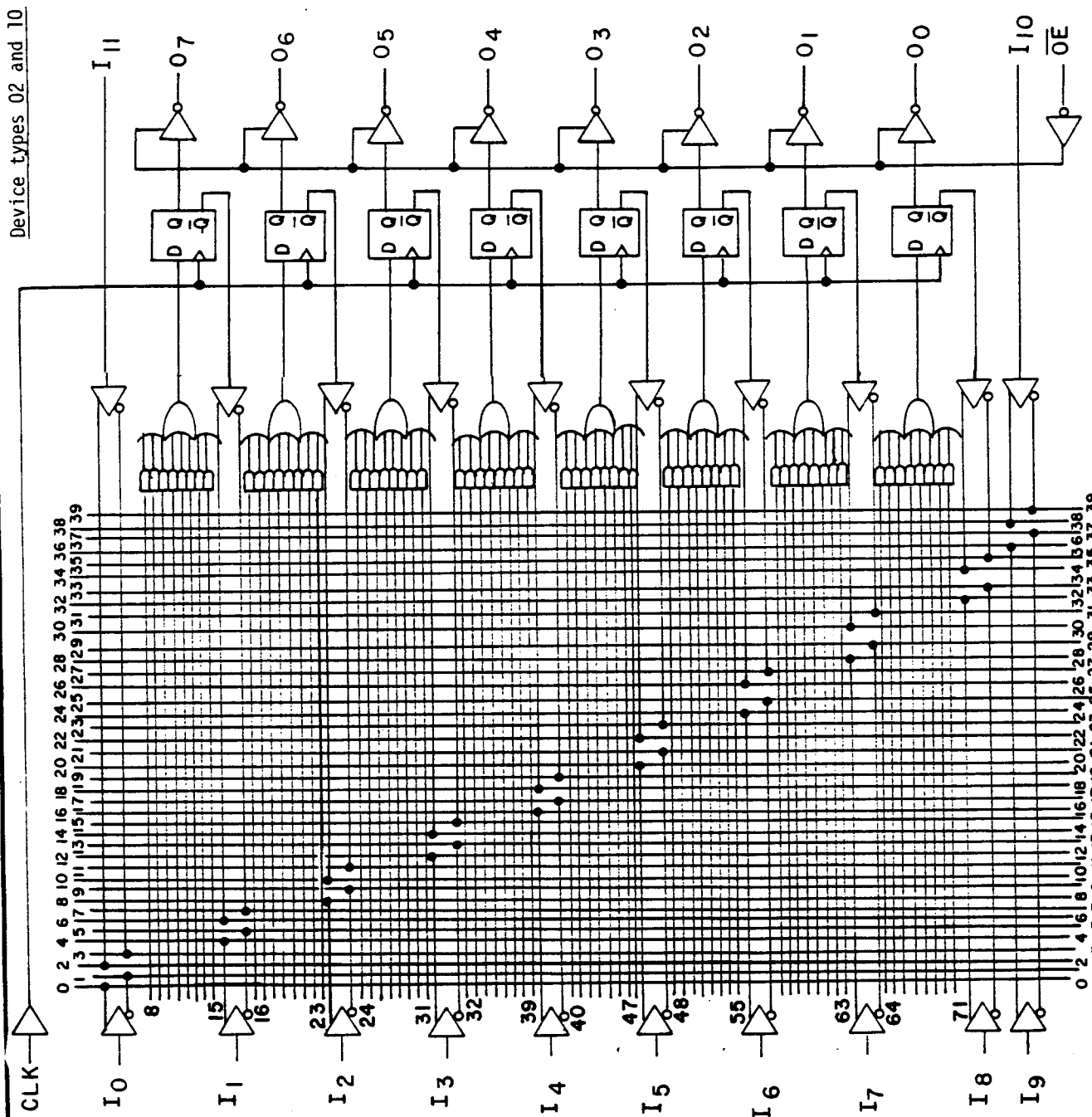


FIGURE 3. (Unprogrammed) Logic diagrams - Continued.

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Device types 03 and 11

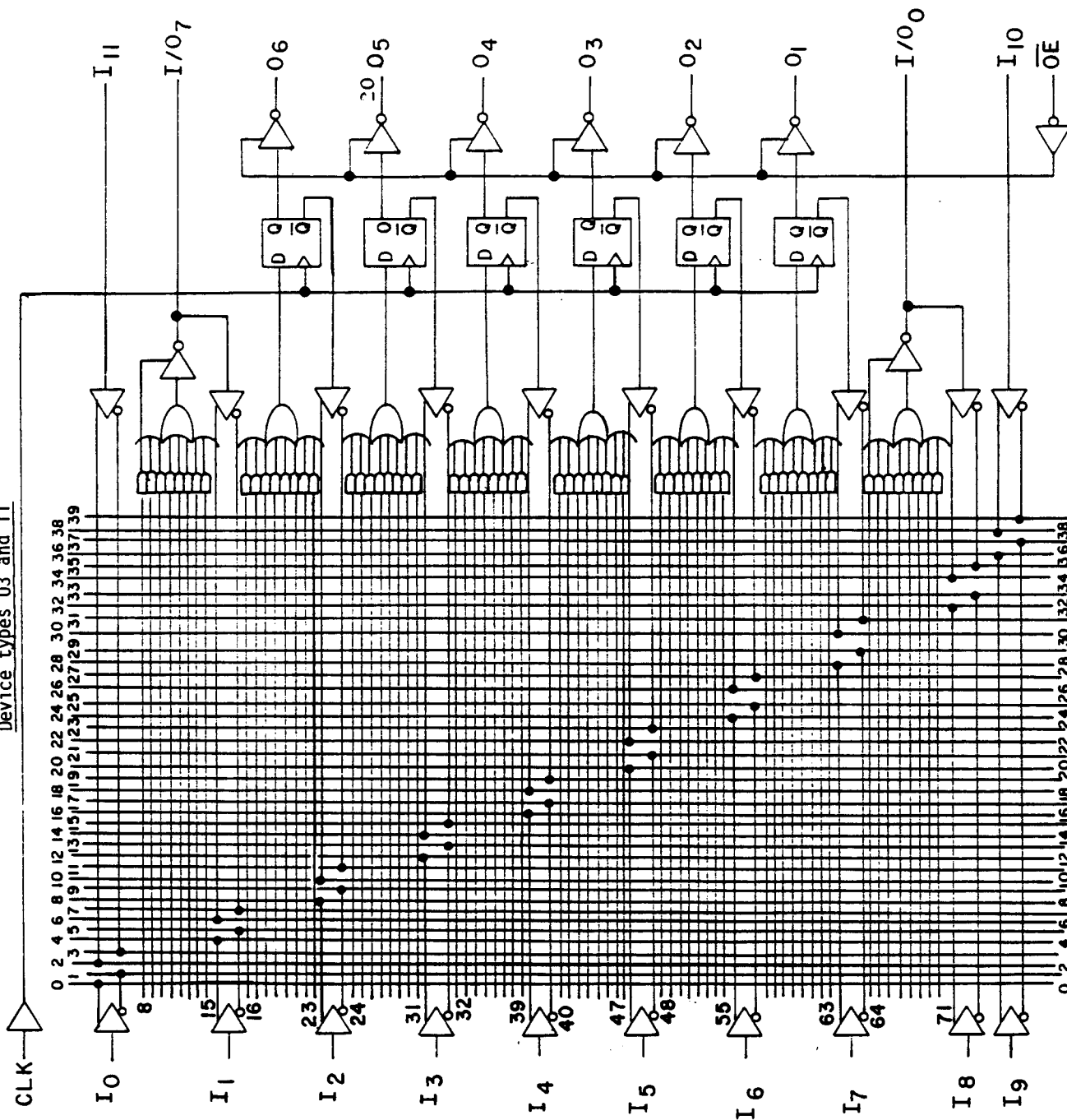


FIGURE 3. (Unprogrammed) Logic diagrams - Continued.

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Device types 04 and 12

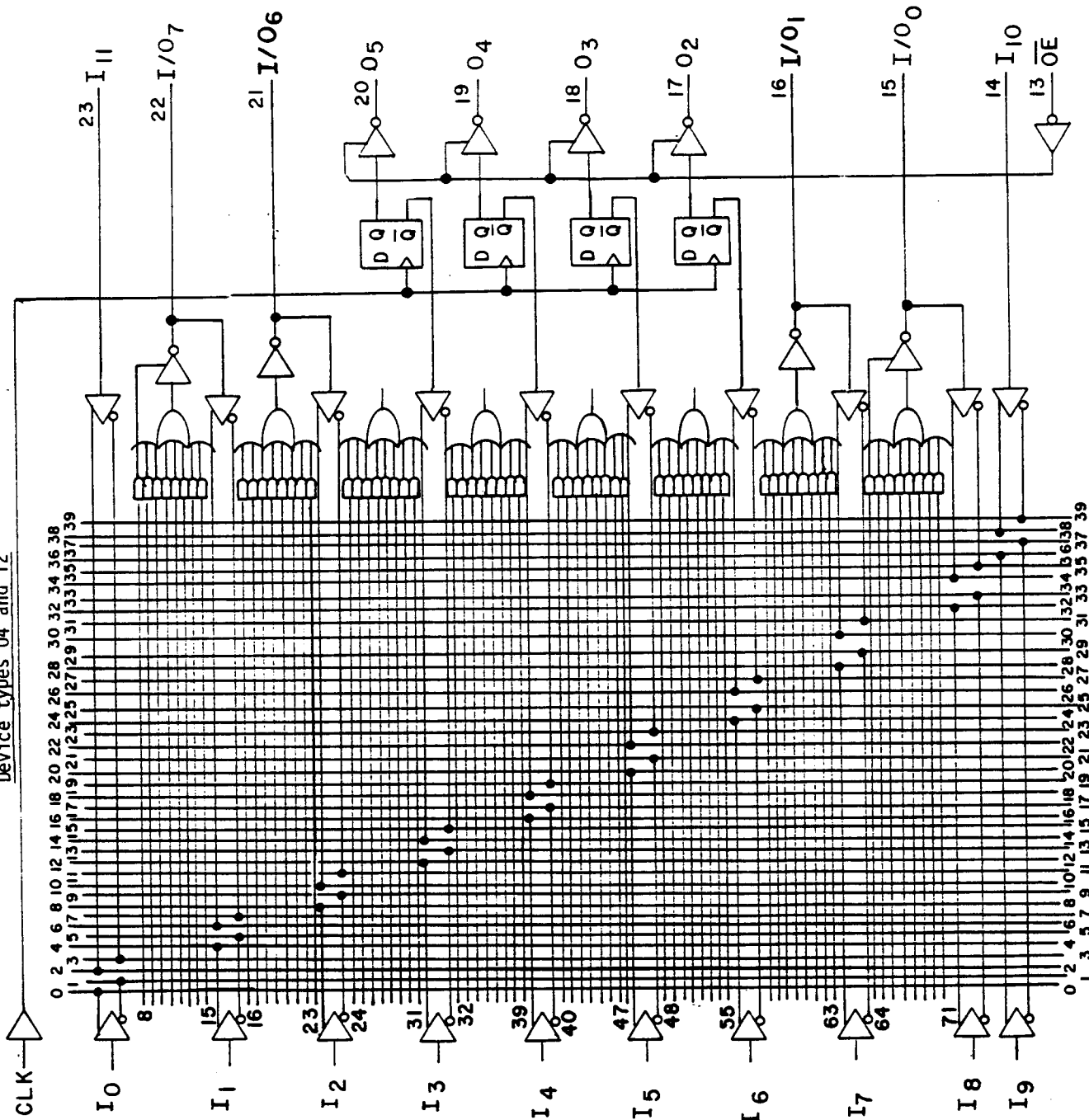


FIGURE 3. (Unprogrammed) Logic diagrams - Continued.

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Device type 05

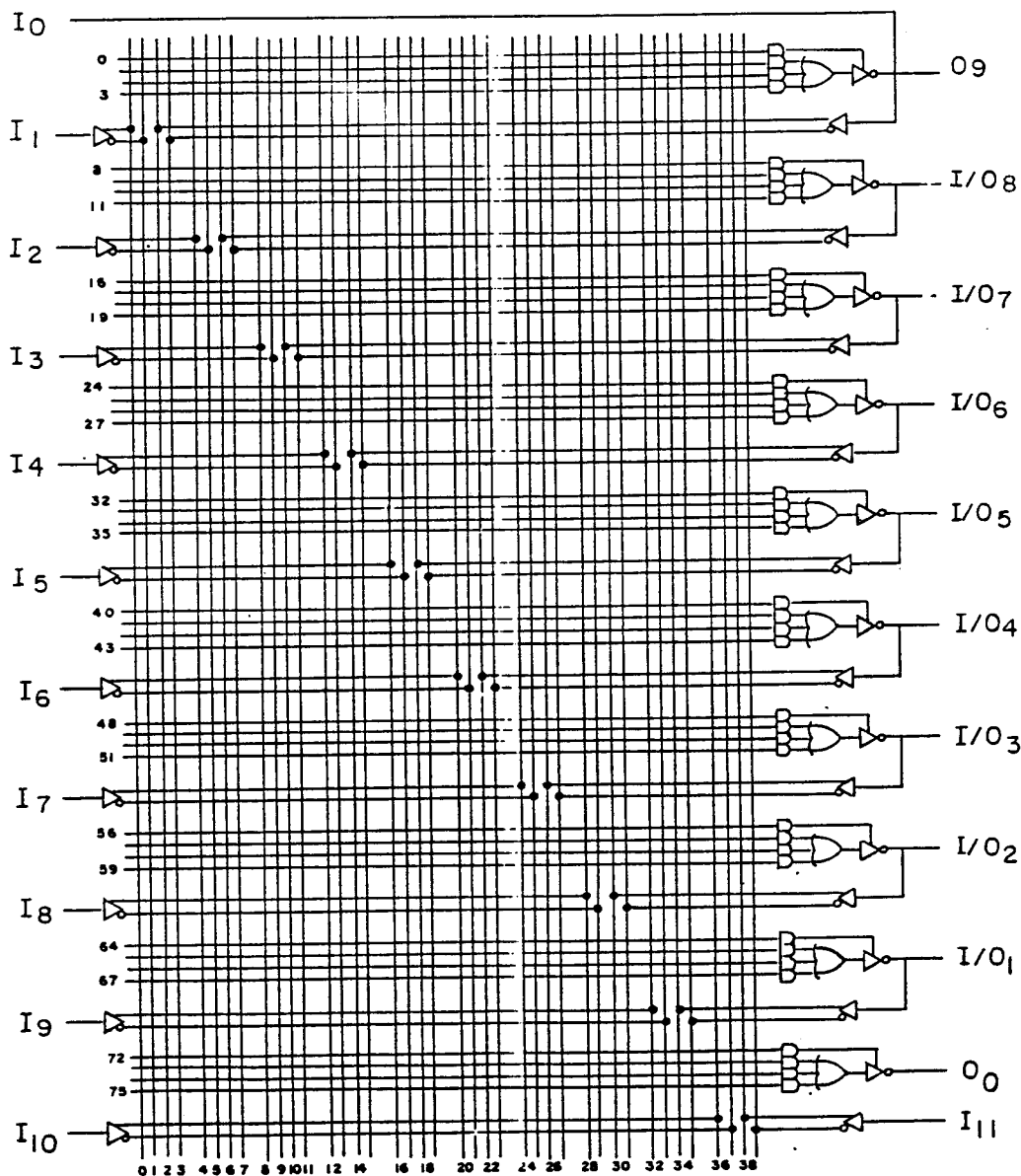


FIGURE 3. (Unprogrammed) Logic diagrams - Continued.

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Device type 06

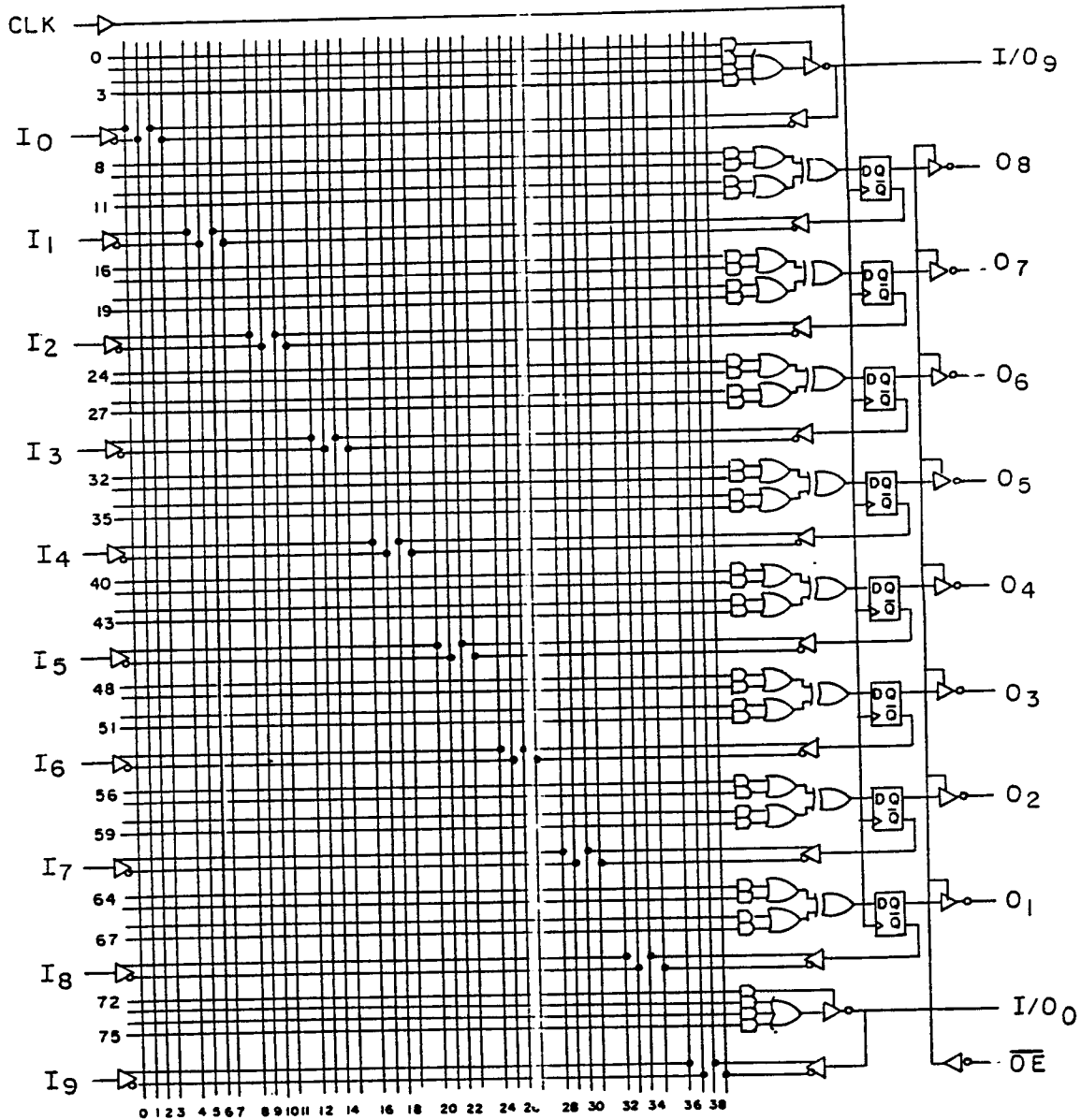


FIGURE 3. (Unprogrammed) Logic diagrams - Continued.

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Device type 07

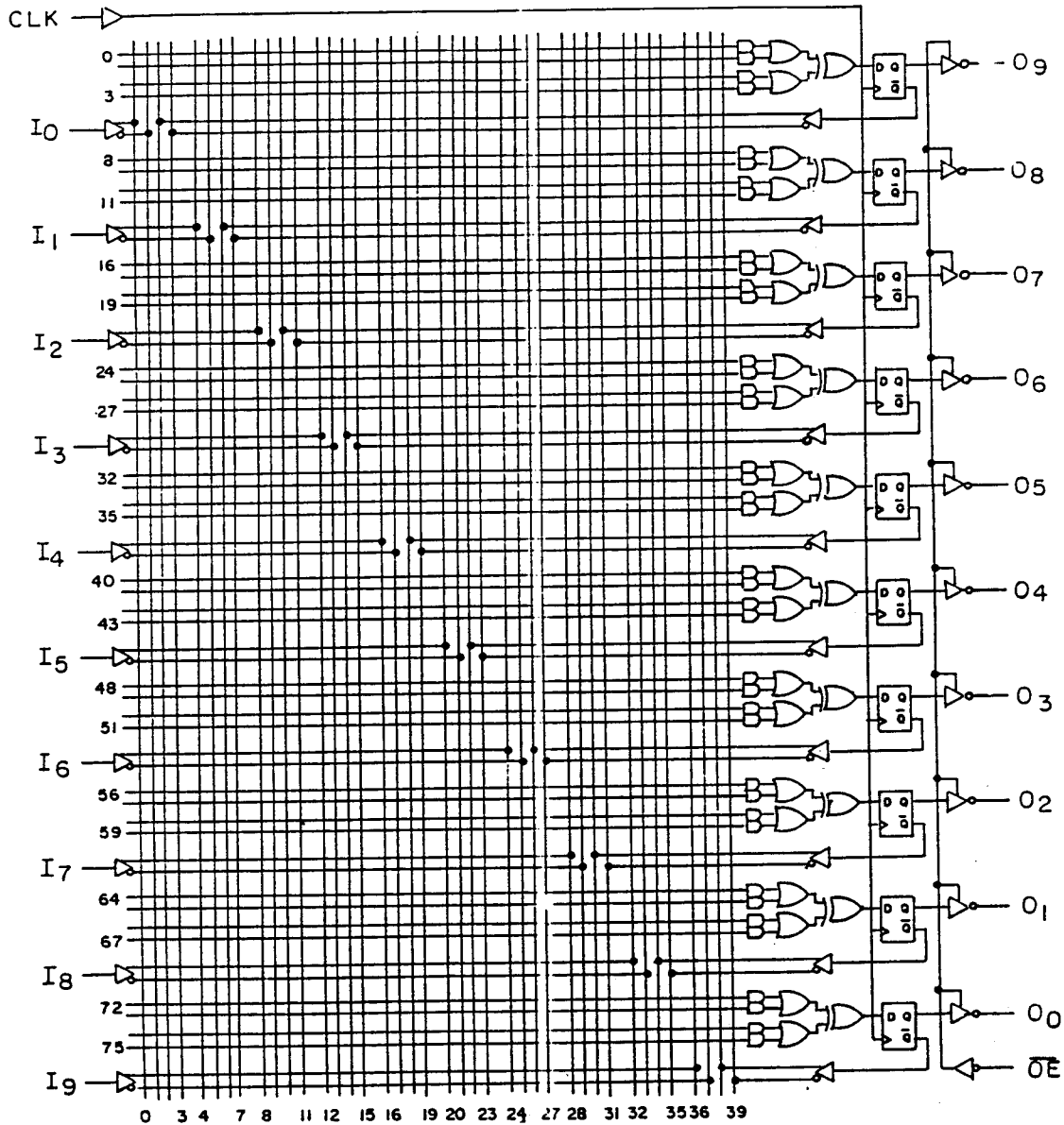


FIGURE 3. (Unprogrammed) Logic diagrams - Continued.

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Device type 08

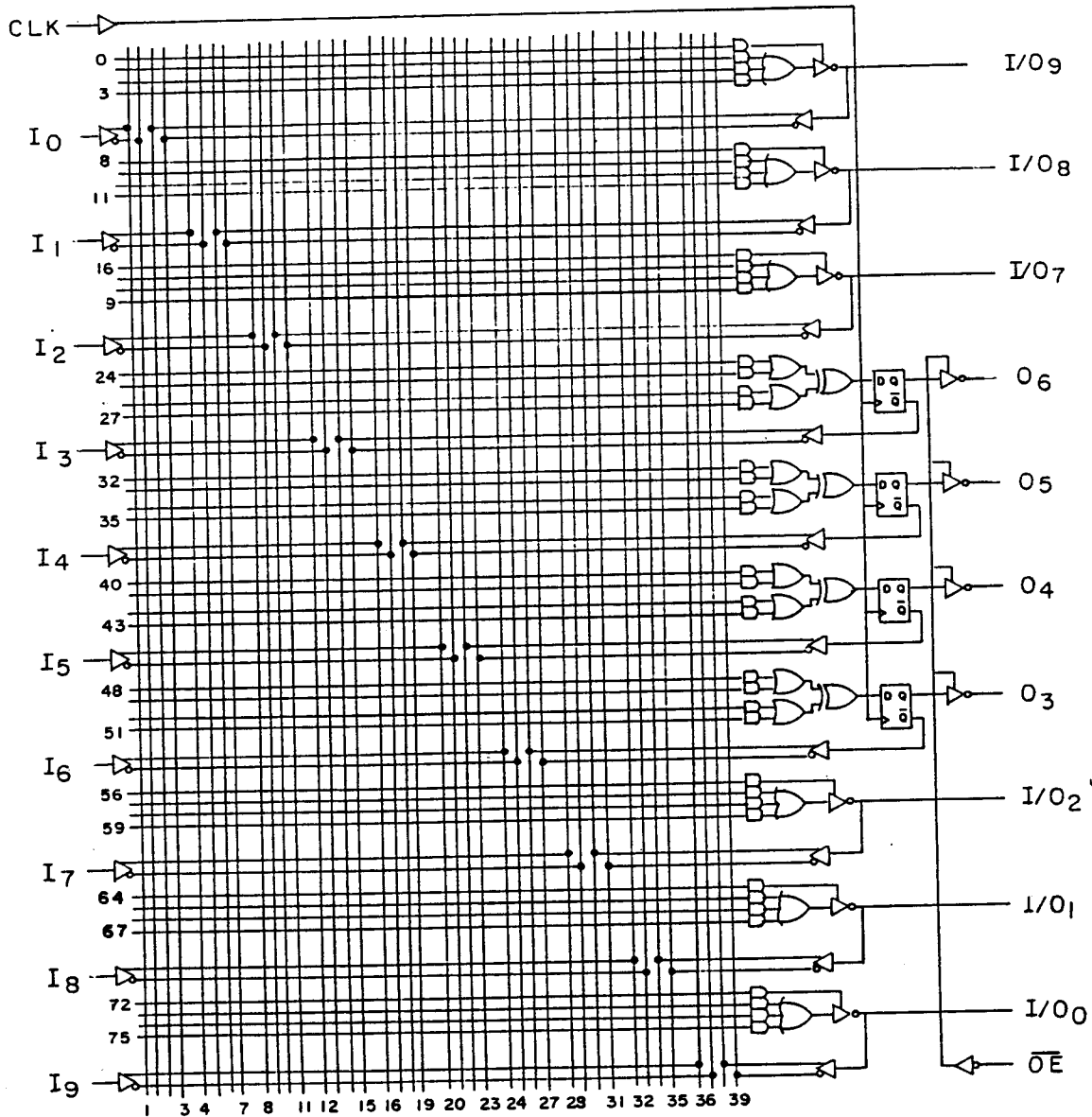


FIGURE 3. (Unprogrammed) Logic diagrams - Continued.

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TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8,9
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7*,8
Group A test requirements (method 5005)	1,2,3,7,8,9 10, 11 <u>4/</u>
Groups C and D end-point electrical parameters (method 5005)	1,2,3

- 1/ * PDA applies to subgroups 1 and 7.
 2/ Any or all subgroups may be combined when using high-speed testers.
 3/ Subgroups 7 and 8 functional tests shall also verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II).
 4/ Subgroups 10 and 11, if not tested, shall be guaranteed to specified limits in table I.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

- Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
- When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/505XXBXX.

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6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>	Replacement military specification part number
8412901JX	<u>2/</u>	PAL20L8AMJTB	
012508 8412901LX <u>3/</u>	01295 50364	TIBPAL20L8-20MJTB PAL20L8AMJS/883B	M38510/50501BLX
8412901KX	50364 01295	PAL20L8AMW/883B TIBPAL20L8-20MWB	
84129013X <u>3/</u>	50364	PAL20L8AML/883B	M38510/50501B3X
8412901XX	01295	TIBPAL20L8-20MFKB	
8412902JX	<u>2/</u>	PAL20R8AMJTB	
8412902LX <u>3/</u>	01295 50364	TIBPAL20R8-20MJTB PAL20R8AMJS/883B	M38510/50502BLX
012509 8412902KX	50364 01295	PAL20R8AMW/883B TIBPAL20R8-20MWB	
84129023X <u>3/</u>	50364	PAL20R8AML/883B	M38510/50502B3X
8412902XX	01295	TIBPAL20R8-20MFKB	
8412903JX	<u>2/</u>	PAL20R6AMTJB	
8412903LX <u>3/</u>	01295 50364	TIBPAL20R6-20MJTB PAL20R6AMJS/883B	M38510/50503BLX
012510 8412903KX	50364 01295	PAL20R6AMW/883B TIBPAL20R6-20MWB	
84129033X <u>3/</u>	50364	PAL20R6AML/883B	M38510/50503B3X
8412903XX	01295	TIBPAL20R6-20MFKB	
012511 8412904JX	<u>2/</u>	PAL20R4AMJTB	

See footnotes at end of table.

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Military drawing part number	Vendor CAGE number	Vendor similar part 1/ number	Replacement military specification part number
8412904LX 3/	01295 50364	TIBPAL20R4-20MJTB PAL20R4AMJS/883B	M38510/50504BLX
8412904KX	50364 01295	PAL20R4AMW/883B TIBPAL20R4-20MWB	
84129043X 3/	50364	PAL20R4AML/883B	M38510/5050483X
8412904XX	01295	TIBPAL20R4-20MKFB	
8412905LX	01295 50364	TIBPAL20L10-25MJTB PAL20L10AMJS/883B	
8412905KX	50364 01295	PAL20L10AMW/883B TIBPAL20L10-25MWB	
84129053X	50364	PAL20L10AML/883B	
8412905XX	01295	TIBPAL20L10-25MFKB	
8412906LX	01295 50364	TIBPAL20X8-25MJTB PAL20X8AMJS/883B	
8412906KX	50364 01295	PAL20X8AMW/883B TIBPAL20X8-25MWB	
84129063X	50364	PAL20X8AML/883B	
8412906XX	01295	TIBPAL20X8-25MFKB	
8412907LX	01295 50364	TIBPAL20X10-25MJTB PAL20X10AMJS/883B	
8412907KX	50364 01295	PAL20X10AMW/883B TIBPAL20X10-25MWB	
84129073X	50364	PAL20X10AML/883B	
8412907XX	01295	TIBPAL20X10-25MFKB	
8412908LX	01295 50364	TIBPAL20X4-25MJTB PAL20X4AMJS/883B	
8412908KX	50364 01295	PAL20X4AMW/883B TIBPAL20X4-25MWB	
84129083X	50364	PAL20X4AML/883B	
8412908XX	01295	TIBPAL20X4-25MFKB	
8412909LX	50364	PAL20L8A-2MJS/883B	

See footnotes at end of table.

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Military drawing part number	Vendor CAGE number	Vendor similar part number	Replacement military specification part number
012508 8412909KX	50364	PAL20L8A-2MW/883B	
84129093X	50364	PAL20L8A-2ML/883B	
8412910LX	50364	PAL20R8A-2MJS/883B	
012509 8412910KX	50364	PAL20R8A-2MW/883B	
84129103X	50364	PAL20R8A-2ML/883B	
8412911LX	50364	PAL20R6A-2MJS/883B	
012510 8412911KX	50364	PAL20R6A-2MW/883B	
84129113X	50364	PAL20L6A-2ML/883B	
8412912LX	50364	PAL20R4A-2MJS/883B	
012511 8412912KX	50364	PAL20R4A-2MW/883B	
84129123X	50364	PAL20R4A-2ML/883B	

- 1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
 2/ Not available from an approved source.
 3/ Inactive for new design. Use M38510/5050XBXX.

Vendor CAGE
number

50364

01295

Vendor name
and address

Monolithic Memories, Inc.
2175 Mission College Blvd.
Santa Clara, CA 95051

Texas Instruments
P.O. Box 6448
Midland, TX 79711

Fusible
link

Titanium-Tungsten

Titanium-Tungsten

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