| REVISIONS | | | | |
|---|---|---|---|---|
| LTR | DESCRIPTION | | DATE | APPROVED |

Prepared in accordance with DOD-STD-100

Selected item drawing

| REV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Original date of drawing | PREPARED BY *Greg A. Pitz* | DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO |
|---|---|---|
| 14 May 1986 | CHECKED BY | TITLE MICROCIRCUITS, MONOLITHIC, N-CHANNEL, SILICON GATE, COUNTER/TIMER AND PARALLEL I/O UNIT |
| | APPROVED BY | |

| SIZE A | CODE IDENT. NO. 14933 | DWG NO. 85517 |
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5962-E080

## 1. SCOPE

1.1 **Scope.** This drawing describes the requirements for N-channel, counter/timer and parallel I/O unit microcircuits. This drawing provides a level of microcircuit quality and reliability assurance for acquisition of microcircuits in accordance with MIL-M-38510.

1.2 **Part number.** The complete part number shall be as shown in the following example:

```
        85517                    01                     Q                      X
          |                       |                     |                      |
          |                       |                     |                      |
   ───────────────        ─────────────────     ────────────────       ────────────────
   Drawing number           Device type           Case outline           Lead finish
                             (1.2.1)                (1.2.2)                 (3.3)
```

1.2.1 **Device types.** The device types shall identify the circuit function as follows:

| Device type | Generic number | Frequency | Circuit |
|---|---|---|---|
| 01 | Z8036A | 6.0 MHz | Counter/timer and parallel I/O unit |
| 02 | Z8036 | 4.0 MHz | Counter/timer and parallel I/O unit |

1.2.2 **Case outlines.** The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

| Outline letter | Case outline |
|---|---|
| Q | D-5 (40-lead, 9/16" x 2"), dual-in-line package |
| Y | C-5 (44-terminal, .650" x .650"), square chip carrier package |

1.3 **Absolute maximum ratings.**

| | |
|---|---|
| $V_{CC}$ supply voltage range (referenced to ground)- - - - | -0.3 V dc to +7.0 V dc |
| Voltage on any pin (referenced to ground)- - - - - - - - | -0.3 V dc to +7.0 V dc |
| Storage temperature range- - - - - - - - - - - - - - - | -65°C to +150°C |
| Maximum power dissipation: | |
| -55°C- - - - - - - - - - - - - - - - - - - - - - - - - | 1.2 W |
| Lead temperature (soldering, 10 seconds) - - - - - - - | +270°C |
| Maximum junction temperature ($T_J$) | |
| at $T_C$ = 125°C- - - - - - - - - - - - - - - - - - - - - | +148°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$) - - - - - - | See MIL-M-38510, appendix C |

1.4 **Recommended operating conditions.**

| | |
|---|---|
| Supply voltage - - - - - - - - - - - - - - - - - - - - - | 4.5 V dc minimum to 5.5 V dc maximum |
| Minimum high level input voltage ($V_{IH}$) - - - - - - - - - | 2.2 V dc |
| Maximum low level input voltage ($V_{IL}$)- - - - - - - - - | 0.8 V dc |
| Frequency of operation: | |
| Device type 01 - - - - - - - - - - - - - - - - - - - | 0.5 MHz to 6.0 MHz |
| Device type 02 - - - - - - - - - - - - - - - - - - - | 0.5 MHz to 4.0 MHz |
| Case operating temperature range ($T_C$)- - - - - - - - - | -55°C to +125°C |
| Clock rise and fall times | |
| Device type 01 - - - - - - - - - - - - - - - - - - - | 10 ns maximum fall; 15 ns maximum rise |
| Device type 02 - - - - - - - - - - - - - - - - - - - | 20 ns maximum |

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510    -    Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883    -    Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. The country of manufacture requirement of MIL-M-38510 does not apply.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Design documentation. The design documentation shall be in accordance with MIL-M-38510 and, unless otherwise specified in the contract or purchase order, shall be retained by the manufacturer but be available for review by the acquiring activity or contractor upon request.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510.

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.5 Marking. Marking shall be in accordance with MIL-M-38510, except the part number shall be in accordance with 1.2 herein. The Vendor Similar Part Number may also be marked in accordance with 6.10 herein. Both part numbers, when used, shall be printed on the same surface. The "M38510/XXX" part number and the "JAN" or "J" mark shall not be used. Lead finish letter "X" is used only as specified in MIL-M-38510 and shall not be marked on the microcircuit or its packaging. The country of origin shall be marked on the microcircuit.

3.6 Quality assurance requirements. Microcircuits furnished under this drawing shall have been subjected to, and passed all the requirements, tests, and inspections detailed herein including screening and quality conformance inspections.

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TABLE I.  Electrical performance characteristics.

| Test | Symbol | Conditions -55°C $\leq$ T$_C$ $\leq$ +125°C V$_{CC}$ = 5.0 V ±10% unless otherwise specified | Group A subgroups | Device type | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| Input high voltage | V$_{IH}$ | | 1, 2, 3 | ALL | 2.2 | V$_{CC}$+0.3 1/ | V |
| Input low voltage | V$_{IL}$ | | 1, 2, 3 | ALL | -0.3 1/ | 0.8 | V |
| Low output voltage | V$_{OL}$ | I$_{OL}$ = 2.0 mA | 1, 2, 3 | ALL | | 0.4 | V |
| High output voltage | V$_{OH}$ | I$_{OH}$ = -250 μA | 1, 2, 3 | ALL | 2.4 | | V |
| Power supply current | I$_{CC}$ | T$_C$ = -55°C V$_{CC}$ = 5.5 V | 1, 2, 3 | ALL | | 200 | mA |
| Output leakage current low | I$_{LOL}$ | V$_{IN}$ = 0.4 V | 1, 2, 3 | ALL | -10 | +10 | μA |
| Output leakage current high | I$_{LOH}$ | V$_{IN}$ = 2.4 V | 1, 2, 3 | ALL | -10 | +10 | μA |
| Input low current | I$_{IL}$ | V$_{IN}$ = 0.4 V | 1, 2, 3 | ALL | -10 | +10 | μA |
| Input high current | I$_{IH}$ | V$_{IN}$ = 2.4 V | 1, 2, 3 | ALL | -10 | +10 | μA |
| Maximum frequency 1/ low-output current | f$_{MAX}$ | | 9, 10, 11 | 01 02 | 6.0 4.0 | | MHz MHz |
| Input capacitance 2/ | C$_{IN}$ | | 4 | ALL | | 10 | pF |
| Output capacitance 2/ | C$_{OUT}$ | | 4 | ALL | | 15 | pF |
| Bidirectional capacitance 2/ | C$_{I/O}$ | | 4 | ALL | | 20 | pF |

See footnotes at end of table.

| Test | Symbol | Conditions −55°C ≤ $T_C$ ≤ +125°C $V_{CC}$ = 5.0 V ±10% unless otherwise specified | Group A subgroups | Refer-ence | Limits 01 Min | 01 Max | 02 Min | 02 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| AS low width | TwAS | $C_L$ = 50 pF ±10% unless otherwise specified See figure 3 | 9, 10, 11 | 1 | 50 | 2000 | 70 | 2000 | ns |
| Address to AS ↑ 3/ setup time | TsA(AS) | | 9, 10, 11 | 2 | 10 | | 30 | | ns |
| Address to AS ↑ 3/ hold time | ThA(AS) | | 9, 10, 11 | 3 | 30 | | 50 | | ns |
| Address to DS ↓ 2/, 3/ setup time | TsA(DS) | | 9, 10, 11 | 4 | 100 | | 130 | | ns |
| CS0 to AS ↑ 2/, 3/ setup time | TsCS0(AS) | | 9, 10, 11 | 5 | 0 | | 0 | | ns |
| CS0 to AS ↑ hold time 3/ | ThCS0(AS) | | 9, 10, 11 | 6 | 40 2/ | | 60 | | ns |
| AS ↑ to DS ↓ delay 2/3/ | TdAS(DS) | | 9, 10, 11 | 7 | 55 | | 85 | | ns |
| CS1 to DS ↓ setup time | TsCS1(DS) | | 9, 10, 11 | 8 | 80 2/ | | 100 | | ns |
| R/W (Read) to DS ↓ set up time | TsRWR(DS) | | 9, 10, 11 | 9 | 80 | | 100 | | ns |
| R/W (Write) to DS ↓ 2/ setup time | TsRWW(DS) | | 9, 10, 11 | 10 | 0 | | 0 | | ns |
| DS low width 2/ | TwDS | | 9, 10, 11 | 11 | 250 | | 390 | | ns |
| Write data to DS ↓ 2/ setup time | TsDW(DSf) | | 9, 10, 11 | 12 | 20 | | 30 | | ns |
| DS (Read) ↓ to address data bus driven 2/ | TdDS(DRV) | | 9, 10, 11 | 13 | 0 | | 0 | | ns |
| DS ↓ to read data valid delay 2/ | TdDSf(DR) | | 9, 10, 11 | 14 | | 180 | | 250 | ns |
| Write data to DS ↑ 2/ hold time | ThDW(DS) | | 9, 10, 11 | 15 | 20 | | 30 | | ns |
| DS ↑ to read data not valid delay 2/ | TdDSr(DR) | | 9, 10, 11 | 16 | 0 | | 0 | | ns |

TABLE I. Electrical performance characteristics - Continued.

See footnotes at end of table.

| Test | Symbol | Conditions -55°C ≤ $T_C$ ≤ +125°C $V_{CC}$ = 5.0 V ±10% unless otherwise specified | Group A subgroups | Reference | Limits 01 Min | 01 Max | 02 Min | 02 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| DS ↑ to read data float delay 2/ 4/ | TdDS(DRz) | $C_L$ = 50 pF ±10% unless otherwise specified See figure 3 | 9, 10, 11 | 17 | | 45 | | 70 | ns |
| R/W to DS ↑ hold time 2/ | ThRW(DS) | | 9, 10, 11 | 18 | 40 | | 55 | | ns |
| CS₁ to DS ↑ hold time 2/ | ThCS₁(DS) | | 9, 10, 11 | 19 | 40 | | 55 | | ns |
| DS ↑ to AS ↓ delay 2/ | TdDS(AS) | | 9, 10, 11 | 20 | 25 | | 50 | | ns |
| Valid access recovery time 2/ 5/ | TrC | | 9, 10, 11 | 21 | 650 | | 1000 | | ns |
| Pattern match to INT delay (bit port) 2/ 6/ | TdPM(INT) | | 9, 10, 11 | 22 | | 1+800 | | 1+800 | ns |
| ACKIN to INT delay (Port with handshake) 2/ 6/ 7/ | TdACK(INT) | | 9, 10, 11 | 23 | | 4+600 | | 4+600 | ns |
| Counter input to INT delay (counter mode) 2/ 6/ | TdCI(INT) | | 9, 10, 11 | 24 | | 1+700 | | 1+700 | ns |
| PCLK to INT delay (timer mode) 2/ 6/ | TdPC(INT) | | 9, 10, 11 | 25 | | 1+700 | | 1+700 | ns |
| AS to INT delay 2/ | TdAS(INT) | | 9, 10, 11 | 26 | | | | 300 | ns |
| INTACK to AS ↑ setup time | Ts1A(AS) | | 9, 10, 11 | 27 | 0 2/ | | 0 | | ns |
| INTACK to AS ↑ hold time | Th1A(AS) | | 9, 10, 11 | 28 | 250 | | 250 | | ns |
| AS ↑ to DS (acknowledge) ↓ setup time 2/ 8/ | TsAS(DSA) | | 9, 10, 11 | 29 | 250 | | 350 | | ns |
| DS (acknowledge) ↓ to read data valid delay 2/ | TdDSA(DR) | | 9, 10, 11 | 30 | | 180 | | 250 | ns |

See footnotes at end of table.

| | | | | | |
|---|---|---|---|---|---|
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TABLE I.  Electrical performance characteristics - Continued.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0$ V ±10% unless otherwise specified | Group A subgroups | Refer- ence | Limits 01 Min | Limits 01 Max | Limits 02 Min | Limits 02 Max | Unit |
|------|--------|------------|-----------|-------|-----|-----|-----|-----|------|
| $\overline{DS}$ (acknowledge) 2/ low width | TwDSA | $C_L = 50$ pF ±10% unless otherwise specified See figure 3 | 9, 10, 11 | 31 | 250 | | 390 | | ns |
| $\overline{AS}$ ↑ to IEO ↓ delay 2/ 8/ $\overline{INTACK}$ cycle | TdAS(IEO) | | 9, 10, 11 | 32 | | 250 | | 350 | ns |
| IEI to IEO delay 2/, 8/ | TdIEI(IEO) | | 9, 10, 11 | 33 | | 100 | | 150 | ns |
| IEO to $\overline{DS}$ (acknowledge) ↓ setup time 2/8/ | TsIEI(DSA) | | 9, 10, 11 | 34 | 70 | | 100 | | ns |
| IEI to $\overline{DS}$ (acknowledge) ↑ hold time 2/ | ThIEI(DSA) | | 9, 10, 11 | 35 | 70 | | 100 | | ns |
| DS (acknowledge) to INT ↑ delay 2/ | TdDSA(INT) | | 9, 10, 11 | 36 | | 600 | | 600 | ns |
| Data input to $\overline{ACKIN}$ ↓ 2/ setup time | TsDI(ACK) | | 9, 10, 11 | 1 | 0 | | 0 | | ns |
| Data input to $\overline{ACKIN}$ ↓ 2/ hold time - strobed handshake | ThDI(ACK) | | 9, 10, 11 | 2 | | | 500 | | ns |
| $\overline{ACKIN}$ ↓ to RFD ↓ 2/ delay | TdACKf(RFD) | | 9, 10, 11 | 3 | 0 | | 0 | | ns |
| $\overline{ACKIN}$ low width - 2/ strobed handshake | TwACKI | | 9, 10, 11 | 4 | | | 250 | | ns |
| $\overline{ACKIN}$ high width - 2/ strobed handshake | TwACKI | | 9, 10, 11 | 5 | | | 250 | | ns |
| RFD ↑ to $\overline{ACKIN}$ ↓ 2/ delay | TdRFDr(ACK) | | 9, 10, 11 | 6 | 0 | | 0 | | ns |
| Data out to $\overline{DAV}$ ↓ 2/, 9/ setup time | TsDO(DAV) | | 9, 10, 11 | 7 | 20 | | 25 | | ns |
| $\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ 2/ delay | TdDAVf(ACK) | | 9, 10, 11 | 8 | 0 | | 0 | | ns |
| Data out to $\overline{ACKIN}$ ↓ 2/, 10/ hold time | ThDO(ACK) | | 9, 10, 11 | 9 | 1 | | 1 | | ns |

See footnotes at end of table.

| | SIZE | CODE IDENT. NO. | DWG NO. |
|---|---|---|---|
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TABLE I. <u>Electrical performance characteristics</u> - Continued.

| Test | Symbol | Conditions -55°C $\leq T_C \leq$ +125°C $V_{CC}$ = 5.0 V ±10% unless otherwise specified | Group A subgroups | Reference | Limits | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | 01 Min | 01 Max | 02 Min | 02 Max | |
| $\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ delay 2/, 10/ | TdACK(DAV) | $C_L$ = 50 pF ±10% unless otherwise specified See figure 3 | 9, 10, 11 | 10 | 1 | | 1 | | ns |
| Data input to RFD ↓ hold time - inter-locked handshake 2/ | ThDI(RFD) | | 9, 10, 11 | 11 | 0 | | 0 | | ns |
| RFD ↓ to $\overline{ACKIN}$ ↑ delay - inter-locked handshake 2/ | TdRFDf(ACK) | | 9, 10, 11 | 12 | 0 | | 0 | | ns |
| $\overline{ACKIN}$ ↑ ($\overline{DAV}$ ↑) to RFD ↑ delay-interlocked and 3-wire handshake 2/ | TdACKr(RFD) | | 9, 10, 11 | 13 | 0 | | 0 | | ns |
| $\overline{DAV}$ ↑ to $\overline{ACKIN}$ ↑ (RFD ↓) inter-locked and 3-wire handshake 2/ | TdDAVr(ACK) | | 9, 10, 11 | 14 | 0 | | 0 | | ns |
| $\overline{ACKIN}$ ↑ (RFD ↓) to $\overline{DAV}$ ↓ delay - interlocked and 3-wire handshake 2/ | TdACK(DAV) | | 9, 10, 11 | 15 | 0 | | 0 | | ns |
| $\overline{DAV}$ ↓ to DAC ↑ delay input 3-wire handshake 2/ | TdDAVIf(DAC) | | 9, 10, 11 | 16 | 0 | | 0 | | ns |
| Data input to $\overline{DAC}$ ↑ hold time - 3-wire handshake 2/ | ThDI(DAC) | | 9, 10, 11 | 17 | 0 | | 0 | | ns |
| DAC ↑ to $\overline{DAV}$ ↓ delay input 3-wire handshake 2/ | TdDACOr(DAV) | | 9, 10, 11 | 18 | 0 | | 0 | | ns |
| $\overline{DAV}$ ↑ to DAC ↓ delay input 3-wire handshake 2/ | TdDAVIr(DAC) | | 9, 10, 11 | 19 | 0 | | 0 | | ns |
| $\overline{DAV}$ ↓ to DAC ↑ delay output 3-wire handshake 2/ | TdDAVOf(DAC) | | 9, 10, 11 | 20 | 0 | | 0 | | ns |
| Data output to DAC ↑ hold time - 3-wire handshake 2/, 10/ | ThDO(DAC) | | 9, 10, 11 | 21 | 1 | | 1 | | ns |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions -55°C ≤ $T_C$ ≤ +125°C $V_{CC}$ = 5.0 V ±10% unless otherwise specified | Group A subgroups | Refer- ence | Limits 01 Min | Limits 01 Max | Limits 02 Min | Limits 02 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| DAC ↑ to DAV ↑ delay 2/ output 3-wire handshake | TdDACIr(DAV) | $C_L$ = 50 pF ±10% unless otherwise specified See figure 3 | 9, 10, 11 | 22 | 1 | | 1 | | ns |
| DAV ↑ to DAC ↓ delay 2/ output 3-wire handshake | TdDAVOr(DAC) | | 9, 10, 11 | 23 | 0 | | 0 | | ns |
| PCLK cycle time 11/ | TcPC | | 9, 10, 11 | 1 | 165 | 4000 | 250 | 4000 | ns |
| PCLK high width 2/ | TwPCh | | 9, 10, 11 | 2 | 70 | 2000 | 105 | 2000 | ns |
| PCLK low width | TwPCI | | 9, 10, 11 | 3 | 70 | 2000 | 105 | 2000 | ns |
| PCLK fall time | TfPC | | 9, 10, 11 | 4 | | 10 | | 20 2/ | ns |
| PCLK rise time 2/ | TrPC | | 9, 10, 11 | 5 | | 15 | | 20 | ns |
| Counter input cycle time 2/ | TcCI | | 9, 10, 11 | 6 | 330 | | 500 | | ns |
| Counter input high width 2/ | TCIh | | 9, 10, 11 | 7 | 150 | | 230 | | ns |
| Counter input low width 2/ | TwCII | | 9, 10, 11 | 8 | 150 | | 230 | | ns |
| Counter input fall time 2/ | TfCI | | 9, 10, 11 | 9 | | 15 | | 20 | ns |
| Counter input rise time 2/ | TrCI | | 9, 10, 11 | 10 | | 15 | | 20 | ns |
| Trigger input to 2/, 12/ PCLK ↓ setup time (timer mode) | TsTI(PC) | | 9, 10, 11 | 11 | | | 150 | | ns |

See footnotes at end of table.

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| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified | Group A subgroups | Refer-ence | Limits 01 Min | Limits 01 Max | Limits 02 Min | Limits 02 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Trigger input to counter input ↓ setup time (counter mode) 2/, 12/ | TsTI(CI) | $C_L = 50\ pF \pm 10\%$ unless otherwise specified See figure 3 | 9, 10, 11 | 12 | | | 150 | | ns |
| Trigger input pulse width (high or low) 2/ | TwTI | | 9, 10, 11 | 13 | | | 200 | | ns |
| Gate input to PCLK ↓ setup time (timer mode) 2/, 12/ | TsGI(PC) | | 9, 10, 11 | 14 | | | 100 | | ns |
| Gate input to counter input ↓ setup time (counter mode) 2/, 12/ | TsGI(CI) | | 9, 10, 11 | 15 | | | 100 | | ns |
| Gate input to PCLK ↓ hold time (timer mode) 2/, 12/ | ThGI(PC) | | 9, 10, 11 | 16 | | | 100 | | ns |
| Gate input to counter input ↓ hold time (counter mode) 2/, 12/ | ThGI(CI) | | 9, 10, 11 | 17 | | | 100 | | ns |
| PCLK to counter output delay (timer mode) 2/ | TdPC(CO) | | 9, 10, 11 | 18 | | | | 475 | ns |
| Counter input to counter output delay (counter mode) 2/ | TdCI(CO) | | 9, 10, 11 | 19 | | | | 475 | ns |
| DS ↓ to REQ ↓ delay 2/ | TdDS(REQ) | | 9, 10, 11 | 1 | | | | 500 | ns |
| DS ↓ to WAIT ↓ delay 2/ | TdDS(WAIT) | | 9, 10, 11 | 2 | | | | 500 | ns |
| PCLK ↓ to REQ ↑ delay 2/ | TdPC(REQ) | | 9, 10, 11 | 3 | | | | 300 | ns |

See footnotes at end of table.

| Test | Symbol | Conditions -55°C ≤ $T_C$ ≤ +125°C $V_{CC}$ = 5.0 V ±10% unless otherwise specified | Group A subgroups | Refer-ence | 01 Min | 01 Max | 02 Min | 02 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| TABLE I. Electrical performance characteristics - Continued. |||||||||||

| Test | Symbol | Conditions | Group A subgroups | Refer-ence | 01 Min | 01 Max | 02 Min | 02 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| PCLK ↓ to WAIT ↑ delay 2/ | TdPC(WAIT) | $C_L$ = 50 pF ±10% unless otherwise specified See figure 3 | 9, 10, 11 | 4 | | | | 300 | ns |
| ACKIN ↓ to REQ ↑ delay 2/, 13/, 14/ | TdACK(REQ) | | 9, 10, 11 | 5 | | | | 3+2 +1000 | ns |
| ACKIN ↓ to WAIT ↑ delay 2/, 15/ | TdACK(WAIT) | | 9, 10, 11 | 6 | | | | 10+ 600 | ns |
| Delay from DS ↑ to AS ↓ for no reset 2/ | TdDSQ(AS) | | 9, 10, 11 | 1 | 15 | | 40 | | ns |
| Delay from AS ↑ to DS ↓ for no reset 2/ | TdASQ(DS) | | 9, 10, 11 | 2 | 30 | | 50 | | ns |
| Minimum width of AS and DS both low for reset 16/ | TwRES | | 9, 10, 11 | 3 | 170 | | 250 | | ns |
| Any input rise time 2/ | TrI | | 9, 10, 11 | 1 | | 100 | | 100 | ns |
| Any input fall time 2/ | TfI | | 9, 10, 11 | 2 | | 100 | | 100 | ns |
| 1's catcher high width 2/, 17/ | Tw1's | | 9, 10, 11 | 3 | 170 | | 250 | | ns |
| Pattern match input valid (bit port) 2/ | TwPM | | 9, 10, 11 | 4 | 500 | | 750 | | ns |
| Data latched on pattern match setup time (bit port) 2/ | TsPMD | | 9, 10, 11 | 5 | 0 | | 0 | | ns |
| Data latched on pattern match hold time (bit port) 2/ | ThPMD | | 9, 10, 11 | 6 | 650 | | 1000 | | ns |

See footnotes on next page.

TABLE I.  Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \leq T_C \leq +125°C$ $V_{CC} = 5.0$ V $\pm10\%$ unless otherwise specified | Group A subgroups | Refer-ence | Limits 01 Min | 01 Max | 02 Min | 02 Max | Unit |
|------|--------|------------|-----------|------|-----|-----|-----|-----|------|
| I/O ↑ to RFD/DAV high delay  2/ | TdIOr(DAV) | $C_L = 50$ pF $\pm10\%$ unless otherwise specified See figure 3 | 9, 10, 11 | 1 | | 500 | | 500 | ns |
| I/O ↑ to data float delay  2/ | TdIOr(DRZ) | | 9, 10, 11 | 2 | | 500 | | 500 | ns |
| I/O ↑ to ACKIN ↓ delay  18/ | TdIOr(ACK) | | 9, 10, 11 | 3 | | | | | ns |
| I/O ↓ to RFD/DAV high delay  2/ | TdIOf(RFD) | | 9, 10, 11 | 4 | | 500 | | 500 | ns |
| I/O ↓ tc RFD/DAV ↓ delay  2/, 19/ | TdIOf(DAV) | | 9, 10, 11 | 5 | 3 | | 3 | | ns |
| I/O ↓ to data bus driven  2/, 19/ | TdDO(IO) | | 9, 10, 11 | 6 | 2 | | 2 | | ns |

1/  Guaranteed by characterization/design.
2/  Guaranteed, if not tested.
3/  Parameter does not apply to interrupt acknowledge transactions.
4/  Float delay is measured to the time when the output has changed 0.5 V from steady state with minimum AC load and maximum DC load.
5/  This is the delay from DS ↑ of one CIO access to DS ↓ of another CIO access.
6/  Units equal to AS cycle + ns.
7/  The delay is from DAV ↓ for 3-wire input handshake.  The delay is from DAC ↑ for 3-wire output handshake.  One additional AS cycle is required for ports in the single buffered mode.
8/  The parameters for the devices in any particular daisy chain must meet the following constraint:  the delay from AS ↑ to DS ↓ must be greater than the sum of TdAS(IEO) for the highest priority peripheral.  TsIEI(DSA) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.
9/  This time can be extended through the use of the deskew timers.
10/ Units equal to AS cycle.
11/ PCLK is only used with the counter/timers (in timer mode), the deskew timers, and the REQUEST/WAIT logic.  If these functions are not used, the PCLK input can be held low.
12/ These parameters must be met to guarantee the trigger or gate is valid for the next counter/timer cycle.
13/ The delay is from DAV ↓ for the 3-wire input handshake.  The delay is from DAC ↑ for the 3-wire output handshake.
14/ Units equal to AS cycles + PCLK cycles + ns.
15/ Units equal to PCLK cycles + ns.
16/ Internal circuitry allows for the reset provided by the Z8 (DS held low while AS pulses) to be sufficient.
17/ If the input is programmed inverting, a low-going pulse of the same width will be detected.
18/ Minimum delay is four AS cycles or one AS cycle after the corresponding IP is cleared, whichever is longer.
19/ Units equal to AS cycles.

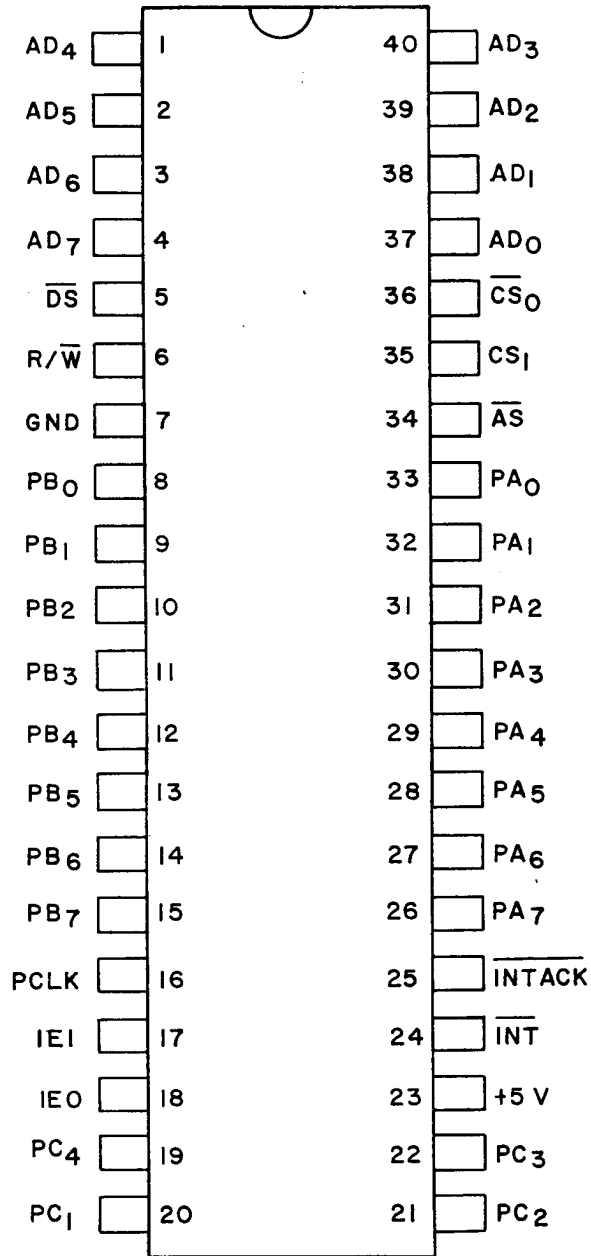| DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO | SIZE A | CODE IDENT. NO. 14933 | DWG NO. 85517 |
|---|---|---|---|
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Case Q



| | | |
|---|---|---|
| $AD_4$ | 1 | 40 | $AD_3$ |
| $AD_5$ | 2 | 39 | $AD_2$ |
| $AD_6$ | 3 | 38 | $AD_1$ |
| $AD_7$ | 4 | 37 | $AD_0$ |
| $\overline{DS}$ | 5 | 36 | $\overline{CS}_0$ |
| $R/\overline{W}$ | 6 | 35 | $CS_1$ |
| GND | 7 | 34 | $\overline{AS}$ |
| $PB_0$ | 8 | 33 | $PA_0$ |
| $PB_1$ | 9 | 32 | $PA_1$ |
| $PB_2$ | 10 | 31 | $PA_2$ |
| $PB_3$ | 11 | 30 | $PA_3$ |
| $PB_4$ | 12 | 29 | $PA_4$ |
| $PB_5$ | 13 | 28 | $PA_5$ |
| $PB_6$ | 14 | 27 | $PA_6$ |
| $PB_7$ | 15 | 26 | $PA_7$ |
| PCLK | 16 | 25 | $\overline{INTACK}$ |
| IEI | 17 | 24 | $\overline{INT}$ |
| IEO | 18 | 23 | +5 V |
| $PC_4$ | 19 | 22 | $PC_3$ |
| $PC_1$ | 20 | 21 | $PC_2$ |

FIGURE 1.  Terminal connections.

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Case Y
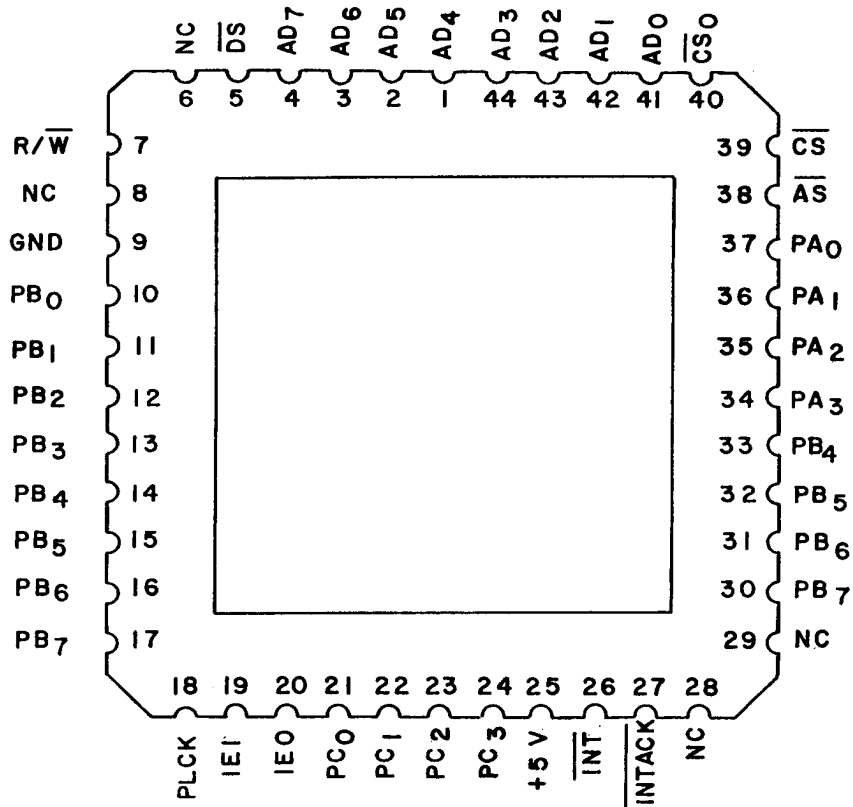


FIGURE 1.  Terminal connections - Continued.

| | SIZE | CODE IDENT. NO. | DWG NO. | |
|---|---|---|---|---|
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INTERRUPT CONTROL LOGIC

4 INTERRUPT CONTROL

INTERNAL BUS

PORT A

8 PORT A I/O

ADDRESS/ DATA BUS

8

Z-BUS INTERFACE

6 CONTROL INPUTS

COUNTER/ TIMER 3

PORT C

4 PORT C I/O

INTERRUPT CONTROL LOGIC

COUNTER/ TIMER 2

PORT B

8 PORT B I/O

COUNTER/ TIMER 1
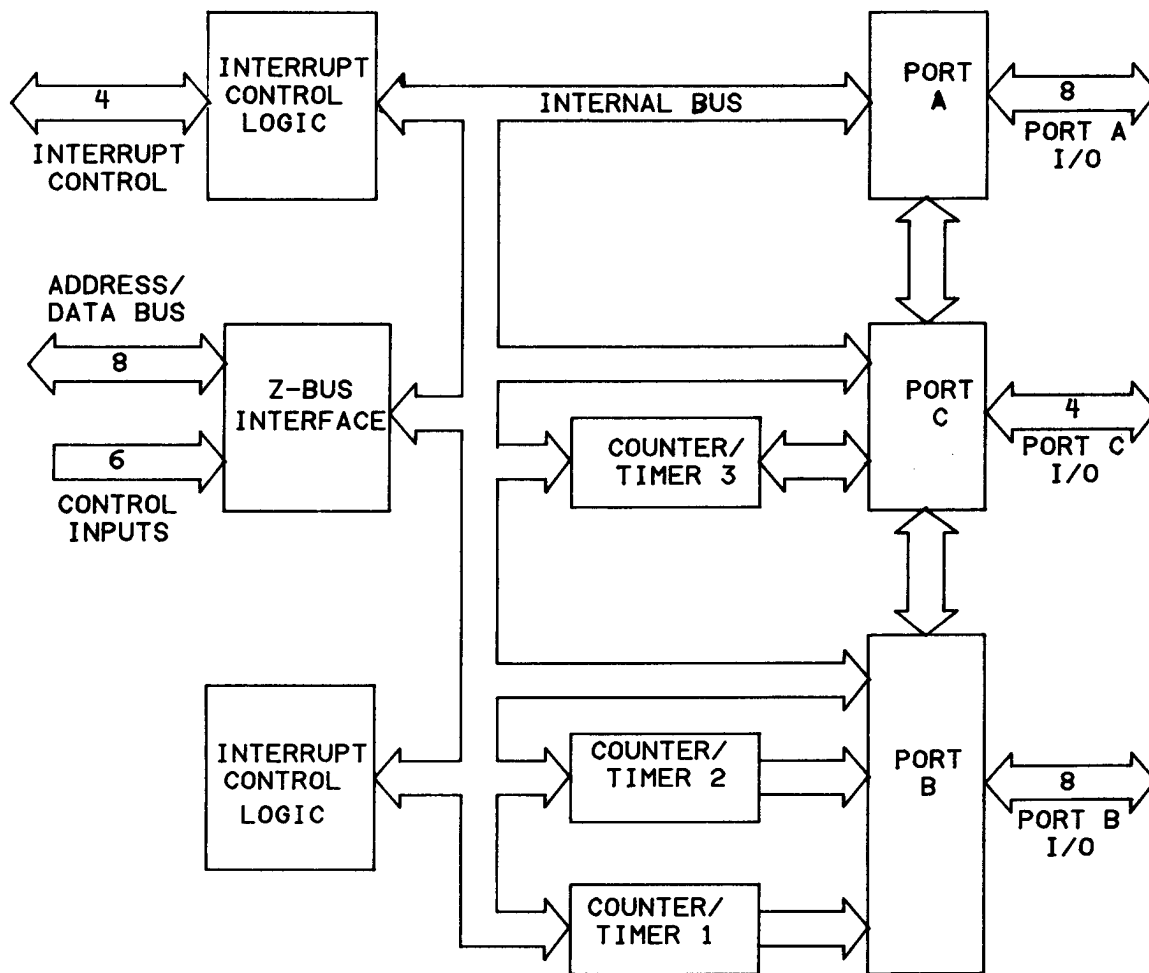
FIGURE 2.  Functional block diagram.

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|---|---|---|---|
| | | REV | PAGE 15 |
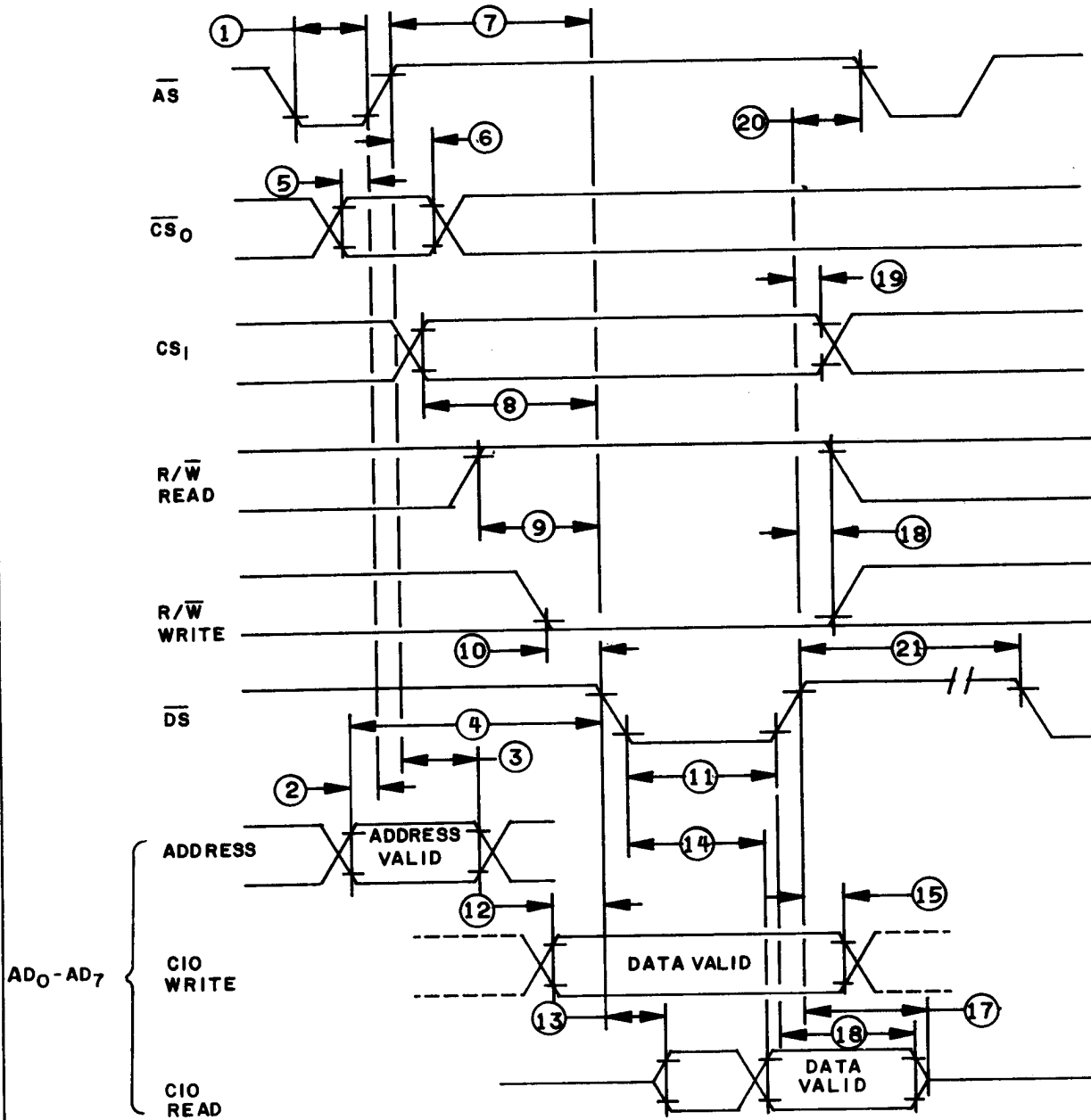
FIGURE 3. Timing diagram for device types 01 and 02.

| | SIZE | CODE IDENT. NO. | DWG NO. | |
|---|---|---|---|---|
| **DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO** | A | **14933** | 85517 | |
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INTERRUPT TIMING
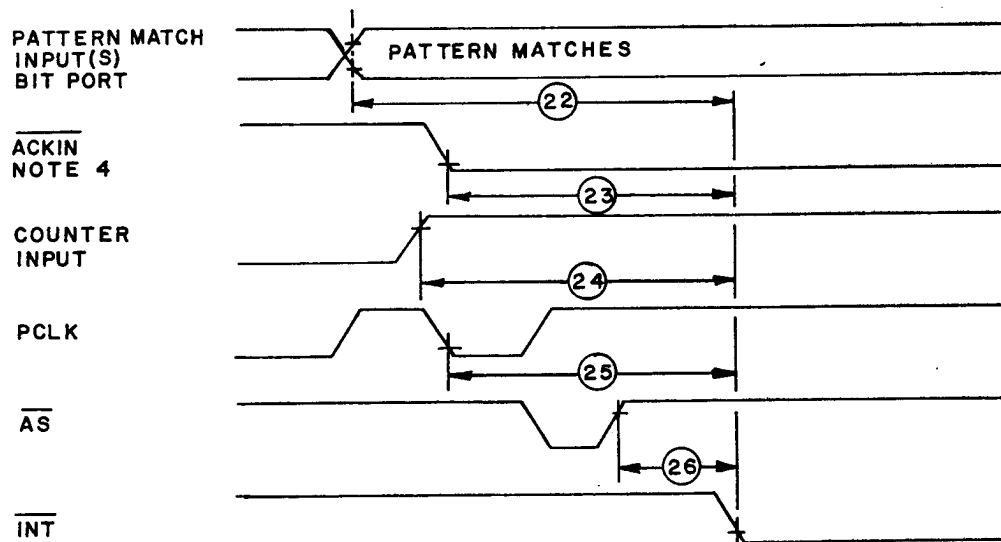
PATTERN MATCH
INPUT(S)
BIT PORT

ACKIN
NOTE 4

COUNTER
INPUT

PCLK

AS

INT

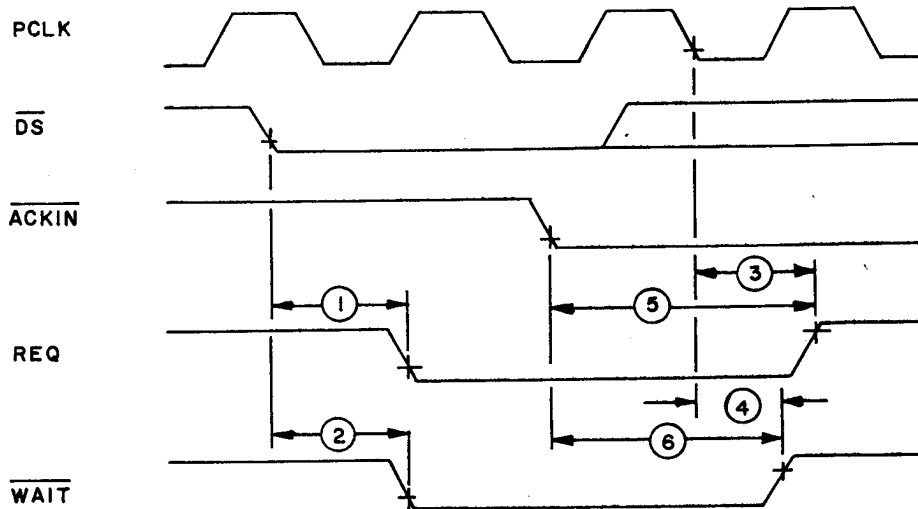PATTERN MATCHES

(22)

(23)

(24)

(25)

(26)
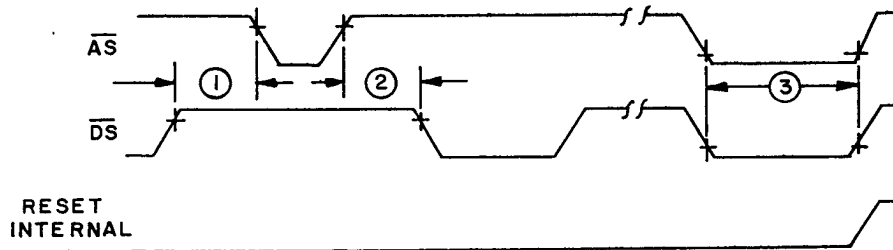
FIGURE 3.   Timing diagram for device types 01 and 02 - Continued.

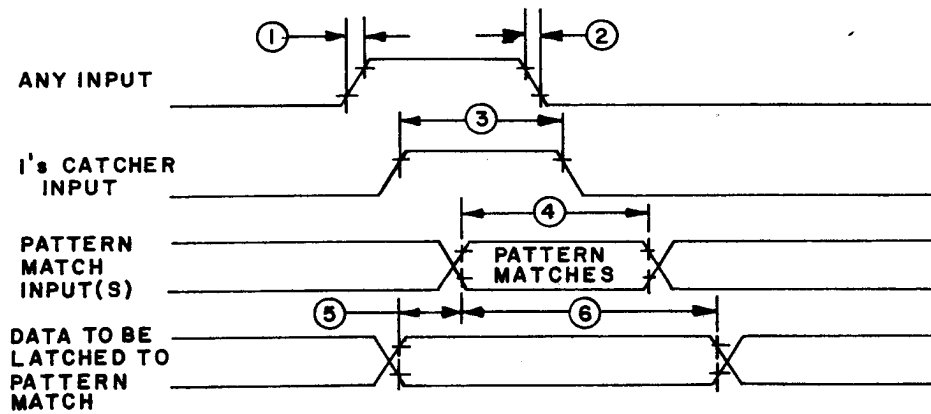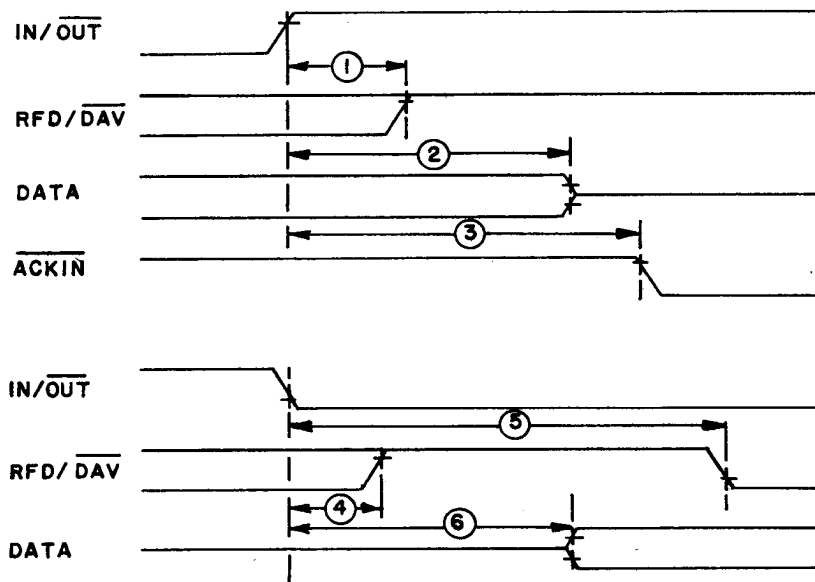| DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO | SIZE A | CODE IDENT. NO. 14933 | DWG NO. 85517 | |
|---|---|---|---|---|
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INTERRUPT
ACKNOWLEDGE TIMING

FIGURE 3. Timing diagram for device types 01 and 02 - Continued.

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STROBED
HANDSHAKE
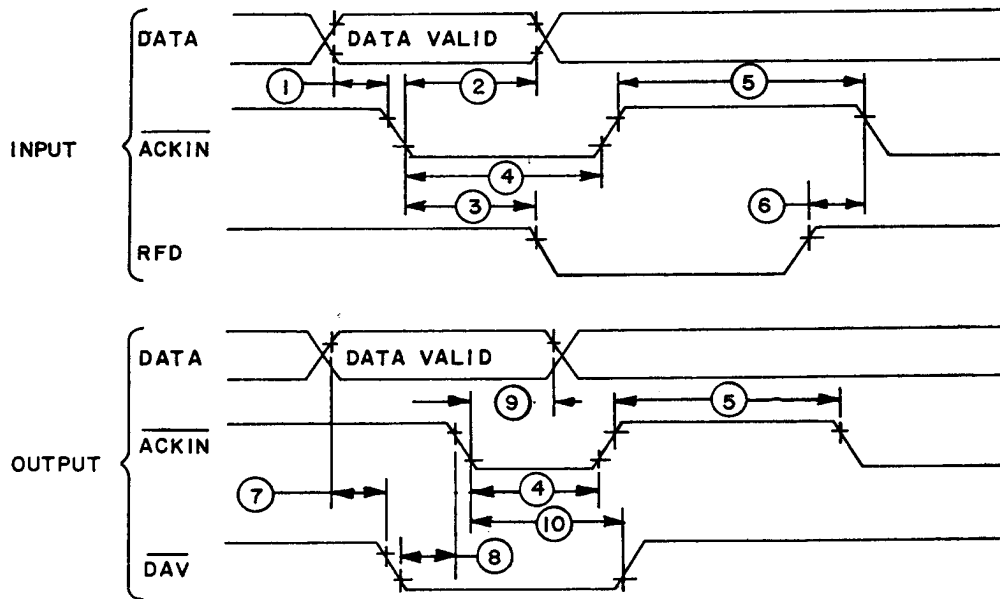


FIGURE 3.   Timing diagram for device types 01 and 02 - Continued.

| | SIZE | CODE IDENT. NO. | DWG NO. | |
|---|---|---|---|---|
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INTERLOCKED
HANDSHAKE
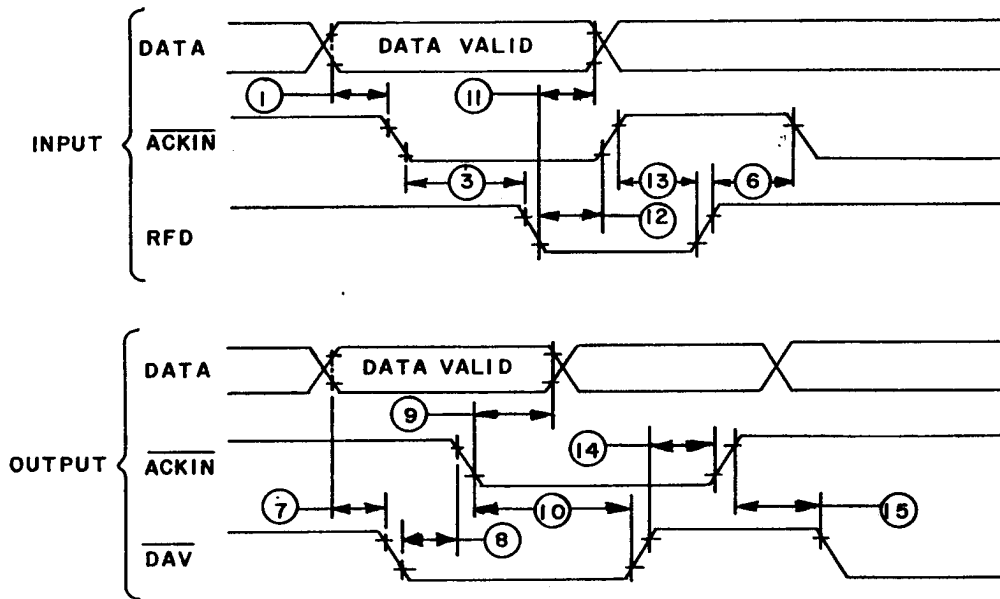


FIGURE 3. Timing diagram for device types 01 and 02 - Continued.

| | SIZE | CODE IDENT. NO. | DWG NO. | |
|---|---|---|---|---|
| DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO | A | 14933 | 85517 | |
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3-WIRE HANDSHAKE
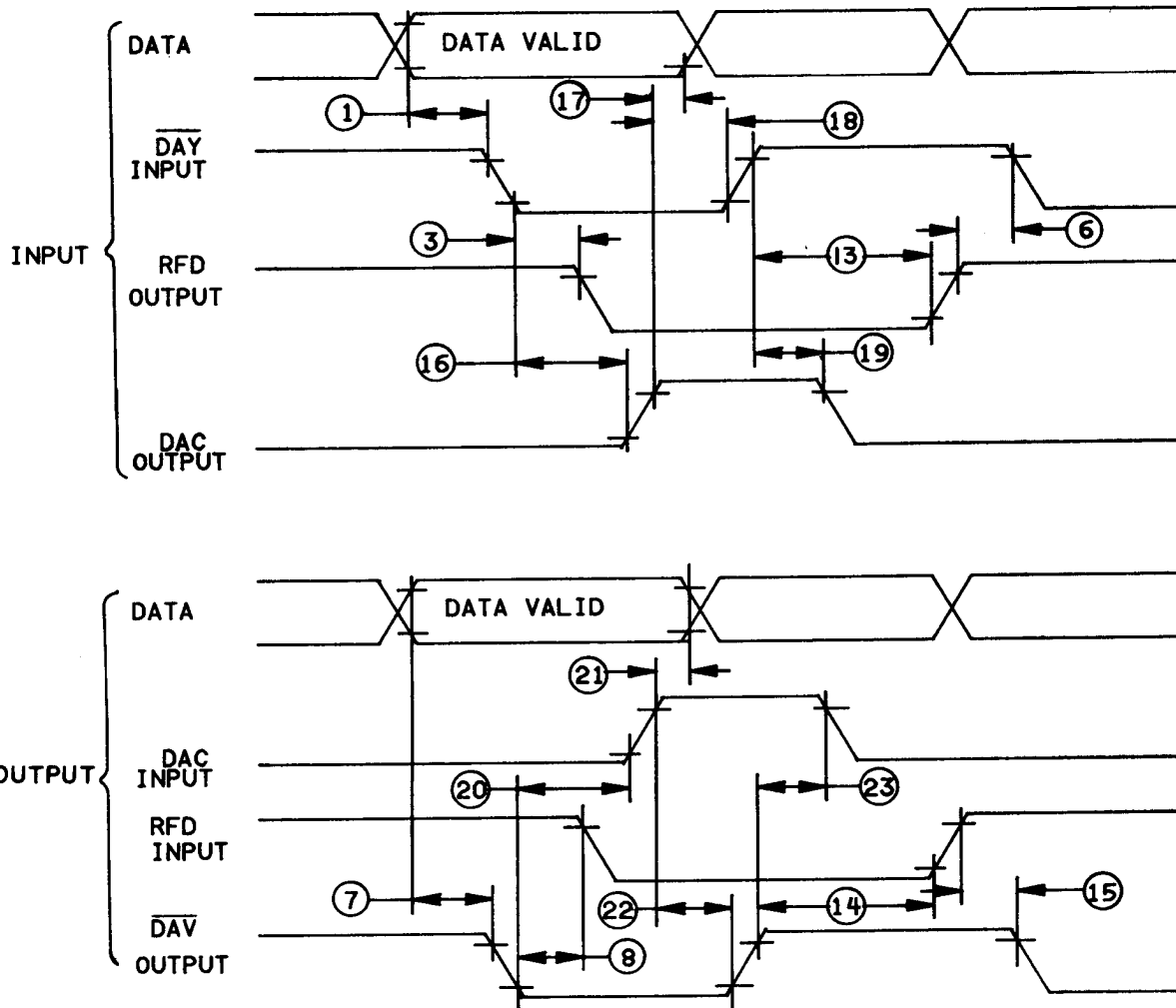


FIGURE 3.  Timing diagram for device types 01 and 02 - Continued.

COUNTER/TIMER
TIMING
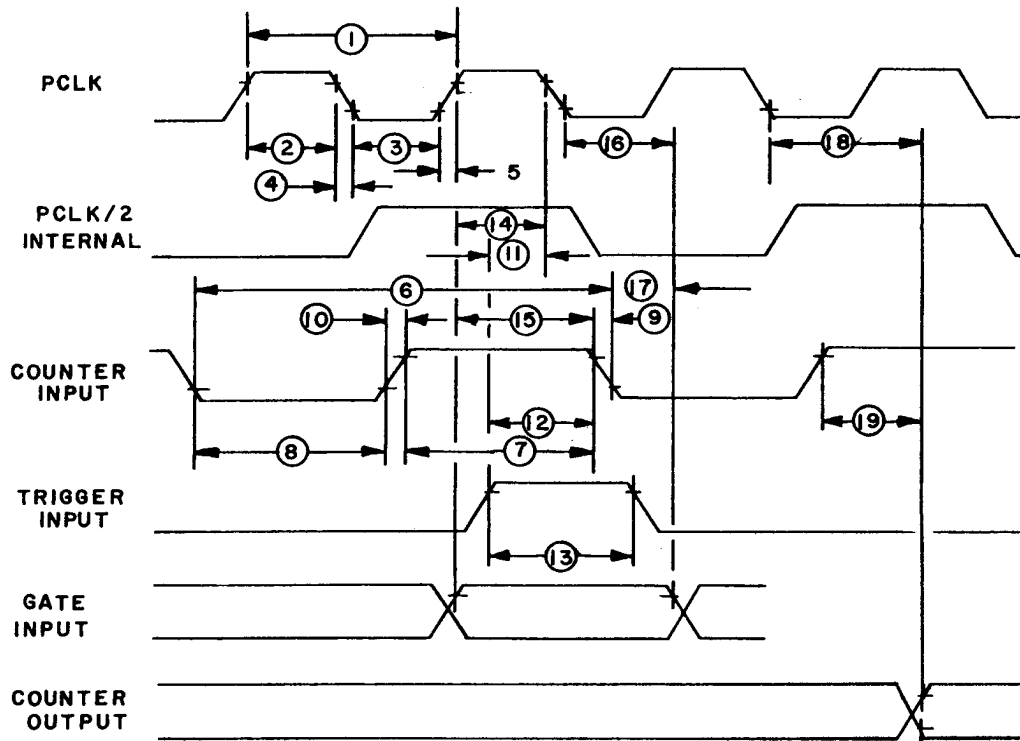


FIGURE 3.  Timing diagram for device types 01 and 02 - Continued.

| | SIZE | CODE IDENT. NO. | DWG NO. | |
|---|---|---|---|---|
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REQUEST/$\overline{\text{WAIT}}$ TIMING



RESET TIMING



FIGURE 3.   Timing diagram for device types 01 and 02 - Continued.

MISCELLANEOUS
PORT TIMING

ANY INPUT

I's CATCHER
INPUT

PATTERN
MATCH
INPUT(S)

PATTERN
MATCHES

DATA TO BE
LATCHED TO
PATTERN
MATCH

BIDIRECTIONAL
PORT TIMING

IN/OUT

RFD/DAV

DATA

ACKIN

IN/OUT

RFD/DAV

DATA

FIGURE 3.   Timing diagram for device types 01 and 02 - Continued.

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3.6.1  Screening.  Screening shall be in accordance with method 5004, class B of MIL-STD-883 and 4.2 herein.

3.6.2  Qualification.  Qualification inspection for the device types specified herein shall not be required.

3.6.3  Quality conformance inspection.  Quality conformance inspection shall be in accordance with MIL-M-38510 and 4.4 herein.

3.6.4  Burn-in test circuit documentation.  The burn-in test circuit documentation shall be made available to the acquiring activity on request.

3.7  Manufacturer eligibility.  To be eligible to supply microcircuits to this drawing, a manufacturer shall have manufacturer certification in accordance with MIL-M-38510 for at least one line and have part I listing on Qualified Products List QPL-38510 for at least one device type (not necessarily the one for which the acquisition of this drawing is to apply).

3.8  Certificate of compliance.  A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply (see 6.9 and 6.10).

4.  QUALITY ASSURANCE PROVISIONS

4.1  Sampling and inspection.  Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2  Screening.  Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.  The following additional criteria shall apply:

    a.  Burn-in test (method 1015 of MIL-STD-883).

       (1)  Test condition A, B, C, or D.

       (2)  $T_A$ = +125°C, minimum.

    b.  Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

    c.  The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.3  Qualification inspection.  Qualification inspection for the device types specified herein shall not be required.

4.4  Quality conformance inspection.  Quality conformance inspection shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883.  Groups A and B inspections shall be performed on each inspection lot or as specified in method 5005 of MIL-STD-883.  Groups C and D shall be performed on a periodic basis in accordance with MIL-M-38510.  Generic test data (see 6.5) may be used to satisfy the requirements for groups C and D inspections.  Manufacturers shall keep lot records for 5 years (minimum), monitor for compliance to the prescribed procedures, and observe that satisfactory manufacturing conditions and records on lots are maintained for these devices.  The records, including an attributes summary of all screening and quality conformance inspections conducted on each lot shall be available for review by customers at all times.

TABLE II.  Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (per method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | --- |
| Final electrical test parameters (method 5004) | 1, 2, 3, 9 |
| Group A test requirements (method 5005) | 1, 2, 3, 7, 8, 9, 10, 11** |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3 |

*  PDA applies to subgroup 1 (see 4.2c).
** Subgroups 10 and 11, if not tested, shall be
   guaranteed to the specified limits in table I.

4.4.1  Group A inspection.  Group A inspection shall consist of the test subgroups and LTPD values shown in table I of method 5005 of MIL-STD-883, class B, and as follows:

a.  Tests shall be as specified in table II herein.

b.  Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c.  Subgroup 7, functional testing shall include verification of instruction set.

4.4.2  Group B inspection.  Group B inspection shall consist of the test subgroups and LTPD values shown in table IIb of method 5005 of MIL-STD-883, class B.

4.4.3  Groups C and D inspections.  Groups C and D inspections shall consist of the test subgroups and LTPD values shown in tables III and IV, method 5005 of MIL-STD-883, class B, and as follows:

a.  End-point electrical parameters shall be as specified in table II herein.

b.  Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1)  Test condition A, B, C, or D.

(2)  $T_A = +125°C$, minimum.

(3)  Test duration:  1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

5.  PACKAGING

5.1  Packaging requirements.  The requirements for packaging shall be in accordance with MIL-M-38510.

6.  NOTES

6.1  Notes.  Only the note "Reevaluation of lot quality" of the notes specified in MIL-M-38510 shall apply to this drawing.

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6.2 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. This drawing is intended exclusively to prevent the proliferation of unnecessary duplicate specifications, drawings, and stock catalog listings. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, this drawing will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity, if applicable.

e. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct shipment to the Government.

6.4 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.5 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than 1 year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design, and process and from the same plant as the die represented. Group D generic data shall be on date codes no more than 1 year old and on the same package type (terms, definitions, and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain the generic data for a period of not less than 5 years from the date of shipment.

6.6 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, OH 45444, or telephone 513-296-5375.

6.7 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surfaces.

b. Ground test equipment, tools, and operator.

c. Do not handle devices by the leads.

d Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent, if practical.

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6.8 Terms and definitions. The abbreviations, terms, symbols, and definitions used herein (including terms and symbols for device terminals) are defined in MIL-M-38510, MIL-STD-1331, and as follows:

$AD_0$-$AD_7$. Z-BUS address/data lines (bidirectional/3-state). These multiplexed address/data lines are used for transfers between the CPU and the device specified herein.

$\overline{AS}$*. Address strobe (input, active low). Addresses, $\overline{INTACK}$, and $\overline{CS_0}$ are sampled while $\overline{AS}$ is low.

$\overline{CS_0}$ and $CS_1$. Chip select 0 (input, active low) and chip select 1 (input, active high). $\overline{CS_0}$ and $CS_1$ must be low and high, respectively, in order to select a device. $\overline{CS_0}$ is latched by $\overline{AS}$.

$\overline{DS}$*. Data strobe (input, active low). $\overline{DS}$ provides timing for the transfer of data into or out of the device specified herein.

IEI. Interrupt enable in (input, active high). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A high IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO. Interrupt enable out (output, active high). IEO is high only if IEI is high and the CPU is not servicing an interrupt from the requesting device or is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{INT}$. Interrupt request (output, open-drain, active low). This signal is pulled low when the device requests an interrupt.

$\overline{INTACK}$. Interrupt acknowledge (input, active low). This signal indicates to the device that an interrupt acknowledge cycle is in progress. $\overline{INTACK}$ is sampled while $\overline{AS}$ is low.

$PA_0$ - $PA_7$. Port A I/O lines (bidirectional, 3-state, or open-drain). These eight I/O lines transfer information between the device's port A and external devices.

$PB_0$ - $PB_7$. Port B I/O lines (bidirectional, 3-state, or open-drain). These eight I/O lines transfer information between the device's port B and external devices. May also be used to provide external access to counter/timers 1 and 2.

$PC_0$ - $PC_3$. Port C I/O lines (bidirectional, 3-state, or open-drain). These four I/O lines are used to provide handshake, $\overline{WAIT}$, and REQUEST lines for Ports A and B or to provide external access to counter/timer 3 or access to the device's Port C.

PCLK. (Input, TTL-compatible). This is a peripheral clock that may be, but is not necessarily, the CPU clock. It is used with timers and REQUEST/$\overline{WAIT}$ logic.

R/$\overline{W}$. Read/write (input). R/$\overline{W}$ indicates that the CPU is reading from (high) and writing to (low) the device.

*When $\overline{AS}$ and $\overline{DS}$ are detected low at the same time (normally an illegal condition), the device is reset.

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6.9 Submission of certificate of compliance. The certificate of compliance submitted to DESC-ECS, prior to listing as an approved source of supply in 6.10, shall state that the manufacturer's product meets the provisions for MIL-STD-883 compliant devices and the requirements herein.

6.10 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.8) has been submitted to DESC-ECS.

| DESC drawing part number | Vendor FSCM number | Vendor similar part number 1/ |
|---|---|---|
| 8551701QX | 56708 | Z8036ACMB |
| 8551702QX | 56708 | Z8036CMB |
| 8551701YX | 56708 | Z8036ALMB |
| 8551702YX | 56708 | Z8036LMB |

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor FSCM
number

56708

Vendor name
and address

Zilog, Incorporated
1315 Dell Avenue
Campbell, CA  95008

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