REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete t_{pd18}, t_{pd22}, and t_{pd27} from table I. Add footnote 2/. Convert to military drawing format. Editorial changes throughout.	1986 OCT 27	
B	Change code identification number to 67268. Add vendor CAGE number 50088 as second source. Editorial changes throughout.	1987 NOV 12	
C	Changes to table I. Editorial change throughout.	1988 OCT 7	

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19				

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Greg A. Pitz

CHECKED BY: Ray Monnin

APPROVED BY:

DRAWING APPROVAL DATE: 24 FEBRUARY 1986

REVISION LEVEL: C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, VECTORED PRIORITY INTERRUPT CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	86029

SHEET 1 OF 19

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1002

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

86029	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2914	Bipolar vectored priority interrupt controller

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225") dual-in-line package
U	C-5 (44-terminal, .662" x .662" x .120") square chip carrier package
Y	See figure 1 (42-lead, 1.090" x .660" x .115") flat package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.705 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q and U	(See MIL-M-38510, appendix C)
Case Y	40°C/W
Junction temperature (T_J)	+175°C
DC output current, into inputs	30 mA
DC input current	-30 mA to +5.0 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Block diagram. The block diagram shall be as specified on figure 2.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.3 Instruction set. The instruction set shall be as specified on figure 4.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

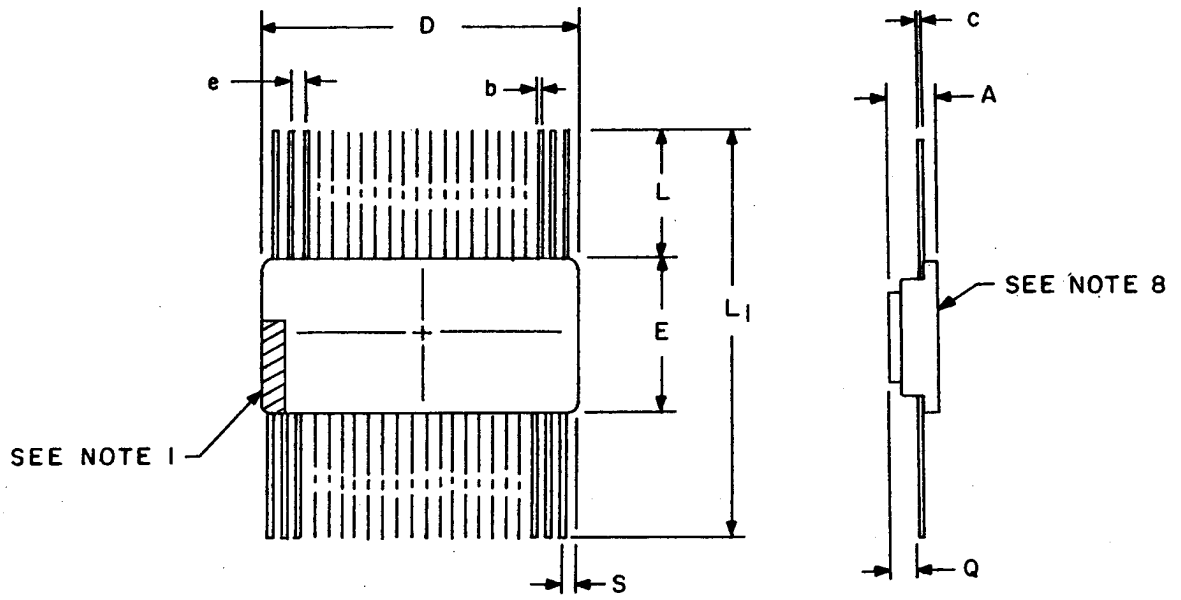

FIGURE 1. Case outline Y (42-lead, 1.090" x .660").

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		86029
		REVISION LEVEL C	SHEET 4

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☆ U.S. GOVERNMENT PRINTING OFFICE: 1987—549-096

Ltr	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.070	.115	1.78	2.92	
b	.017	.023	0.43	0.58	5
c	.006	.012	0.15	0.30	5
D	1.030	1.090	26.16	27.69	
E	.600	.660	15.24	16.76	
E1	---	.720	---	18.29	3
e	.045	.055	1.14	1.40	4,6
L	.250	.370	6.35	9.40	
L1	1.300	1.370	33.02	34.80	
Q	.020	.060	0.51	1.52	2
S	.005	---	0.13	---	7

NOTES:
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is .050 (1.25 mm) between centerlines. Each pin centerline shall be located within ±.005 (0.13 mm) of its exact longitudinal position relative to pins 1 and 42.
5. All leads: Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A is applied.
6. Forty spaces.
7. Applies to all four corners (lead numbers 1, 21, 22, and 42).
8. Configuration 2 is optional. If this configuration is used, no organic or polymeric materials shall be molded to the top of the package to cover the leads.

FIGURE 1. Case outline Y (42-lead, 1.090" x .660") - Continued.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = Minimum, I_{OH} = -1.0 mA V_{IN} = V_{IH} or V_{IL}		1, 2, 3	2.4		V
Output low voltage	V_{OL}	V_{CC} = Minimum V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA	1, 2, 3		0.4	V
			I_{OL} = 8.0 mA			0.45	
			I_{OL} = 12 mA			0.5	
Input high level	V_{IH}			1, 2, 3	2.0		V
Input low level	V_{IL}			1, 2, 3		0.8	V
Input clamp voltage	V_{IC}	V_{CC} = Minimum, I_{IN} = -18 mA		1, 2, 3		-1.5	V
Output leakage current for $\overline{IR}$ output	I_{CEX}	V_{CC} = Minimum, V_O = 5.5 V		1, 2, 3		250	µA
Input low current	I_{IL}	V_{CC} = Maximum V_{IN} = 0.4 V	M_{0-7}	1, 2, 3		-0.15	mA
			S_{0-2}			-0.1	
			LB			-0.4	
			$\overline{ID}$			-2.0	
			$\overline{IE}$			-1.2	
			All others			-0.8	
Input high current	I_{IH1}	V_{CC} = Maximum V_{IN} = 2.7 V	M_{0-7}	1, 2, 3		150	µA
			S_{0-2}			100	
			$\overline{GE}$, $\overline{GAR}$			40	
			$\overline{IE}$			60	
			$\overline{ID}$			60	
			All others			20	
Input high current	I_{IH2}	V_{CC} = Maximum, V_{IN} = 5.5 V		1, 2, 3		1.0	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Off-state output current	I_{OZL}	V_{CC} = Maximum	V_{OUT} = 0.5 V, M_{o-7}	1, 2, 3		-150	µA
			S_{o-2}			-100	
			V_{o-2}			-50	
	I_{OZH}		V_{OUT} = 2.4 V, M_{o-7}			150	
			S_{o-2}			100	
			V_{o-2} others			50	
Power supply current	I_{CC}	V_{CC} = Maximum	-55°C, +25°C	1, 3		310	mA
			+125°C	2		260	
Functional tests		See 4.3.1c		7, 8			
Output short circuit current 1/	I_{OS}	V_{CC} = 6.0 V, V_O = 0.5 V		1, 2, 3	-30	-85	mA
Propagation delay from input $\overline{IE}$ to output:		See figure 5 2/		9, 10, 11			
SM Bus	t_{pd1}					60	ns
S Bus	t_{pd2}					68	ns
V_0, V_1, V_2	t_{pd3}					70	ns
$\overline{GAS}$	t_{pd4}					62	ns
Propagation delay from input I_0, I_1, I_2, I_3 to output: SM Bus	t_{pd5}					60	ns
S Bus	t_{pd6}					68	ns
V_0, V_1, V_2	t_{pd7}					70	ns
$\overline{GAS}$	t_{pd8}					62	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay from input IRPT disable to output: V_0, V_1, V_2	t_{pd9}	See figure 5 2/	9, 10, 11		48	ns
$\overline{IR}$	t_{pd10}				60	ns
$\overline{RD}$	t_{pd11}				22	ns
$\overline{GAS}$	t_{pd12}				33	ns
Propagation delay from IRPT latches and register to: V_0, V_1, V_2	t_{pd13}				82	ns
$\overline{IR}$	t_{pd14}				105	ns
PD	t_{pd15}				75	ns
$\overline{RD}$	t_{pd16}				75	ns
$\overline{GAS}$	t_{pd17}				85	ns
Propagation delay from mask register to: $\overline{IR}$	t_{pd19}				105	ns
PD	t_{pd20}				75	ns
$\overline{RD}$	t_{pd21}				75	ns
Propagation delay from status register to: V_0, V_1, V_2	t_{pd23}				73	ns
$\overline{IR}$	t_{pd24}				96	ns
PD	t_{pd25}				66	ns
$\overline{RD}$	t_{pd26}				66	ns

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay from lowest group enabled flip-flop to:		See figure 5 2/	9, 10, 11			
PD	t_{pd28}				54	ns
$\overline{RD}$	t_{pd29}				58	ns
$\overline{GS}$	t_{pd30}				45	ns
Propagation delay from IRPT request enable flip-flop to $\overline{IR}$	t_{pd31}				66	ns
Propagation delay from status overflow flip-flop to status overflow	t_{pd32}				40	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Setup time 1	from: S Bus	t_{s1}	See figure 5 2/	9, 10, 11	15		ns
Hold time 1		t_{h1}			19		ns
Setup time 2	from: M Bus	t_{s2}			15		ns
Hold time 2		t_{h2}			16		ns
Setup time 3	from: $\overline{P}_0$-$\overline{P}_7$	t_{s3}			15		ns
Hold time 3		t_{h3}			9		ns
Setup time 4	from: Latch bypass	t_{s4}			20		ns
Hold time 4		t_{h4}			0		ns
Setup time 5	from: $\overline{IE}$, I_0, I_1, I_2, I_3	t_{s5}			55 t_{PWL} +40		ns
Hold time 5	3/	t_{h5}			0		ns
Setup time 6	from: $\overline{GE}$	t_{s6}			15		ns
Hold time 6		t_{h6}			13		ns
Setup time 7	from: $\overline{GAR}$	t_{s7}			15		ns
Hold time 7		t_{h7}			17		ns
Setup time 8	from: $\overline{ID}$	t_{s8}			42		ns
Hold time 8		t_{h8}			14		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Hold time 9 from: $\overline{P_0}$-$\overline{P_7}$ Hold time relative to LB	t_{h9}	See figure 5 2/	9, 10, 11	25		ns
Minimum clock low time	t_{pw1}			30		ns
Minimum clock high time	t_{pw2}			30		ns
Minimum interrupt input ($\overline{P_0}$-$\overline{P_7}$) low time for guaranteed acceptance (pulse mode)	t_{pw3}			40		ns
Maximum interrupt input ($\overline{P_0}$-$\overline{P_7}$) low time for guaranteed rejection (pulse mode)	t_{pw4}				8	ns
Minimum clock period, $\overline{TE}$ = H on current cycle and previous cycle	t_{pw5}			55		ns
Minimum clock period, $\overline{TE}$ = L on current cycle or previous cycle	t_{pw6}			110		ns

1/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed 1 second.

2/ All outputs fully loaded, C_L = 50 pF. Measurements made at 1.5 V with input levels of 0 and 3.0 V.

3/ t_{PWL} is the clock low time. Both setup times must be met.

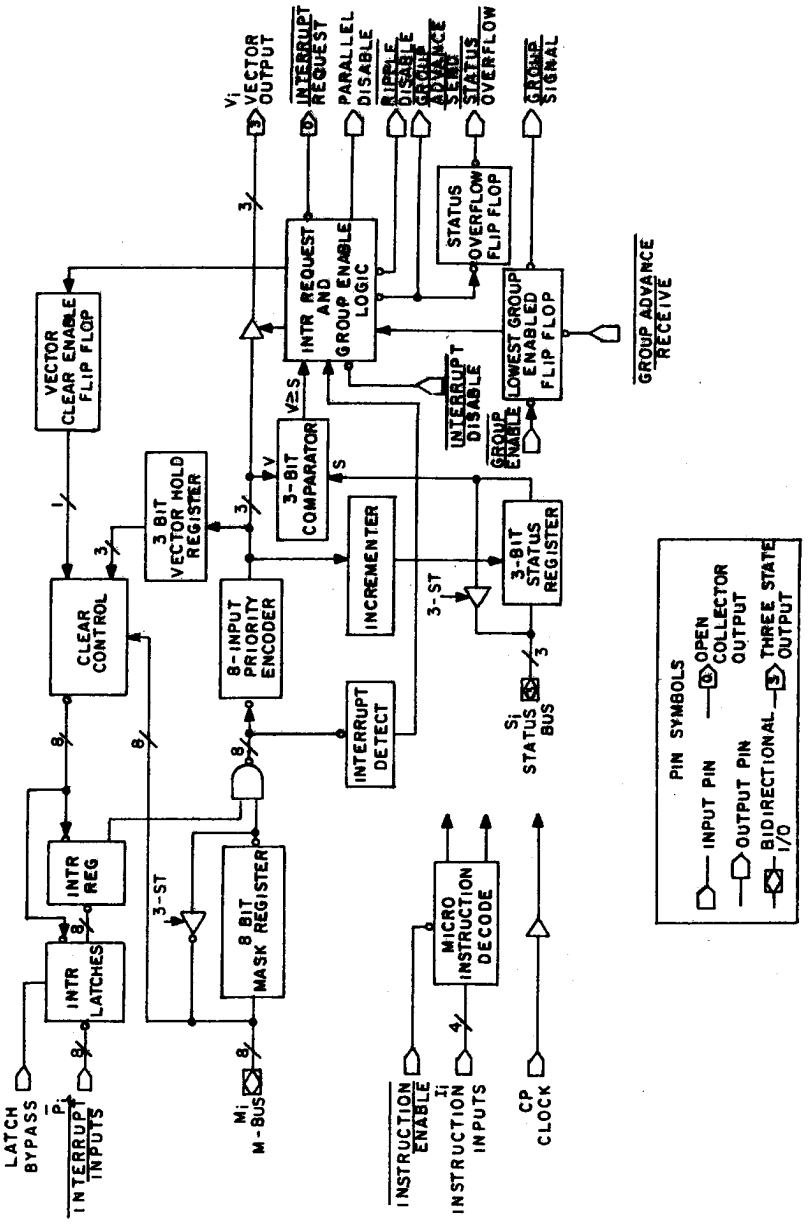

FIGURE 2. Block diagram.

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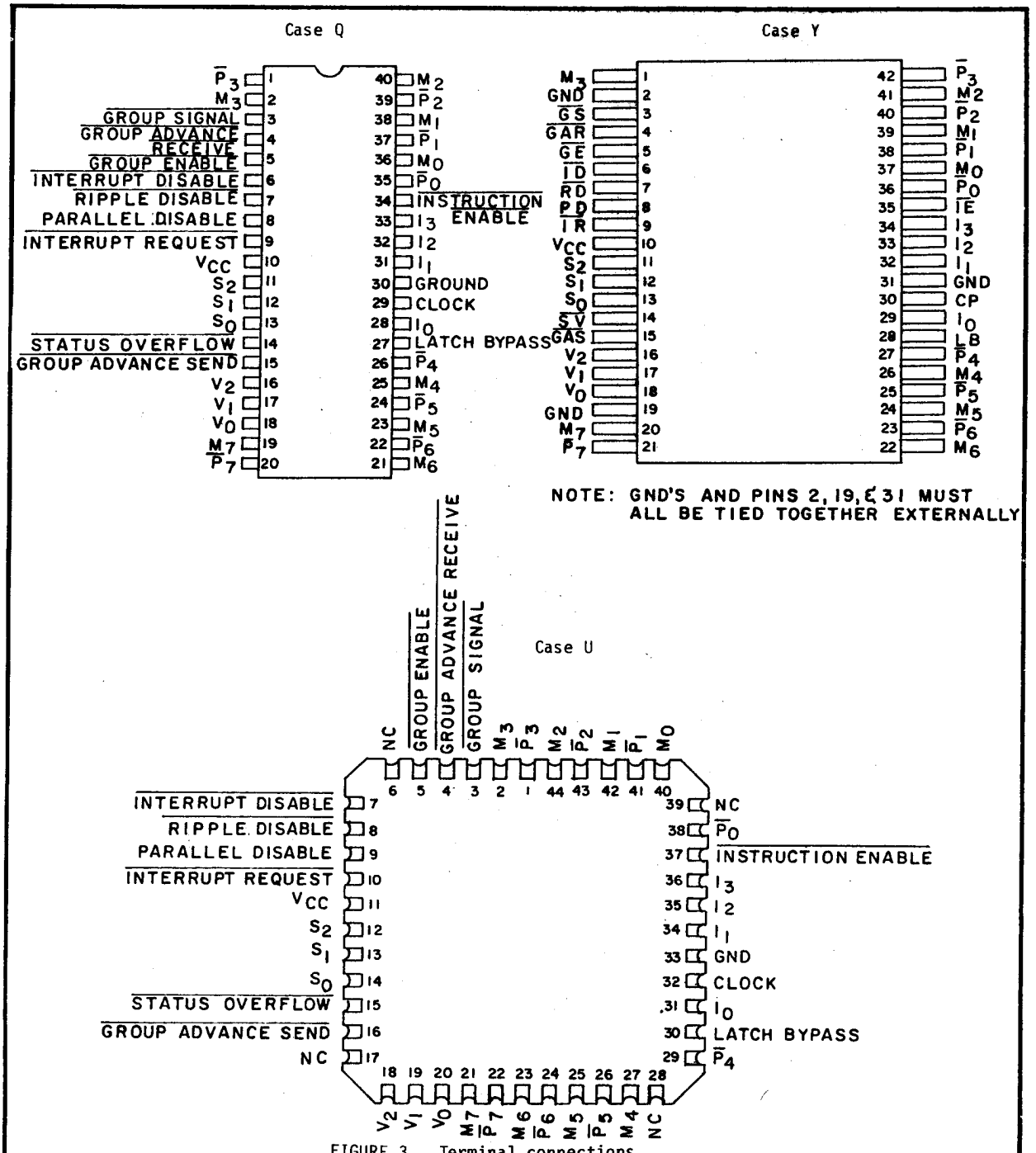

FIGURE 3. Terminal connections.

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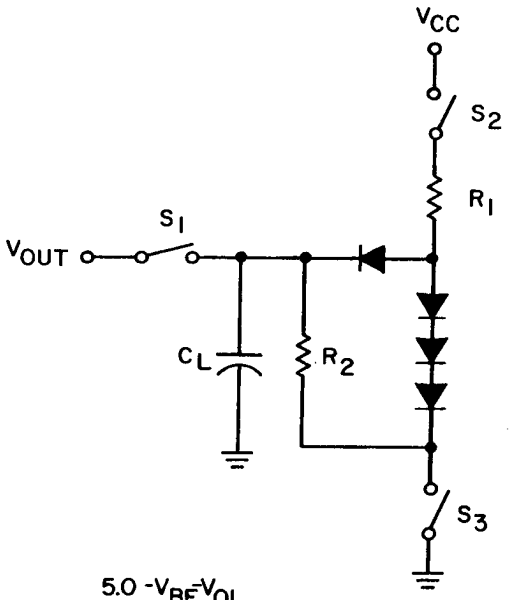
☆ U.S. GOVERNMENT PRINTING OFFICE: 1987—549-096

$I_3I_2I_1I_0$	Mnemonic	Instruction
		Mask register functions
1110	LDM	Load mask register from M bus
0111	RDM	Read mask register to M bus
1100	CLRM	Clear mask register (enables all priorities)
1000	SETM	Set mask register (inhibits all interrupts)
1010	BCLRM	Bit clear mask register from M bus
1011	BSETM	Bit set mask register from M bus
		Status register functions
1001	LDSTA	Load status register from S bus and LGE flip-flop from $\overline{GE}$ input
0110	RDSTA	Read status register to S bus
		Interrupt request control
1111	ENIN	Enable interrupt request
1101	DISIN	Disable interrupt request
		Vectored output
0101	RDVC	Read vector output to V outputs, load V + 1 into status register, load V into vector hold register and set vector clear enable flip-flop
		Priority interrupt register clear
0001	CLRIN	Clear all interrupts
0011	CLRMR	Clear interrupts from mask register data (uses the M bus)
0010	CLRMB	Clear interrupts from M bus data
0100	CLRVC	Clear the individual interrupt associated with the last vector read
		Master clear
0000	MCLR	Clear all interrupts, clear mask register, clear status register, clear LGE flip-flop, enable interrupt request

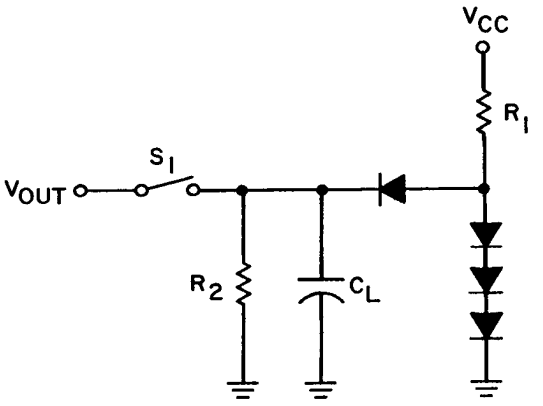
FIGURE 4. Instruction set.

A. Three-state outputs



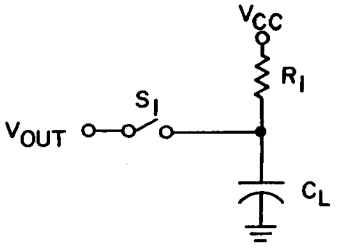
$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1\ K}}$$

B. Normal outputs



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}} \qquad R2 = \frac{2.4\ V}{I_{OH}}$$

C. Open-collector outputs



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

FIGURE 5. Switching test circuit.

Test output load

Pin label	Test circuit	R1	R2
$\overline{\text{Group signal}}$	B	300Ω	2.4 kΩ
$\overline{\text{Group advance receive}}$	B	300Ω	2.4 kΩ
$\overline{\text{Ripple disable}}$	B	300Ω	2.4 kΩ
Parallel disable	B	300Ω	2.4 kΩ
$\overline{\text{Interrupt request}}$	C	390Ω	---
S_{0-2}	A	300Ω	1 kΩ
$\overline{\text{Status overflow}}$	B	300Ω	2.4 kΩ
V_{0-2}	A	300Ω	1 kΩ
M_{0-7}	A	300Ω	1 kΩ

NOTES:
1. C_L = 50 pF includes scope probe, stray wiring, and capacitances without device in test fixture.
2. S_1, S_2, and S_3 are closed during function tests and all ac tests except output enable tests.
3. S1 and S3 are closed while S2 is open for enable high test. S1 and S2 are closed while S3 is open for enable low test.
4. C_L = 5.0 pF for output disable tests.
5. Disable times measured from .5 V change on the output.

FIGURE 5. Switching test circuit - Continued.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall consist of verifying the instruction set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
8602901QX	34335 50088 50088	AM2914/BQA TS2914MCB/C TS2914MJB/C
8602901YX	34335	AM2914/BYC
8602901UX	34335 50088	AM2914/BUA TS2914MEB/C

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Inc. 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088
50088	Thomson Components-Mostek Corporation 1310 Electronics Drive Carrollton, TX 75006