

P54/74FCT257T/AT/CT P54/74FCT258T/AT/CT DATA SELECTOR/MULTIPLEXER

FEATURES

- Function, Pinout and Drive Compatible with the FCT and F Logic
- FCT-C speed at 4.3ns max. (Com'I)
FCT-A speed at 5.0ns max. (Com'I)
- Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 64 mA Sink Current (Com'I), 32 mA (MII)
15 mA Source Current (Com'I), 12 mA (MII)
- 3-State Outputs
- Manufactured in 0.7 micron PACE Technology™

DESCRIPTION

The 'FCT257T and 'FCT258T have four identical 2-input multiplexers with 3-state outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the select input is HIGH. Data appears at the output in true noninverted form for the 'FCT257T and in the inverted form for the 'FCT258T from the selected outputs.

The 'FCT257T and 'FCT258T are logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the select input.

Outputs are forced to a high-impedance "OFF" state when the Output Enable input ($\overline{OE}$) is HIGH.

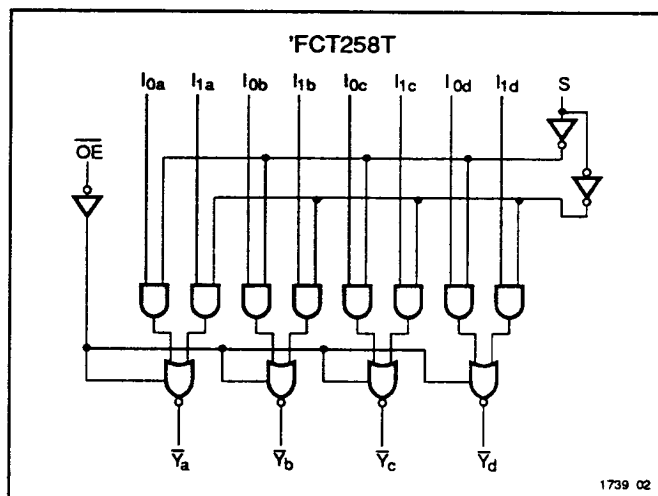
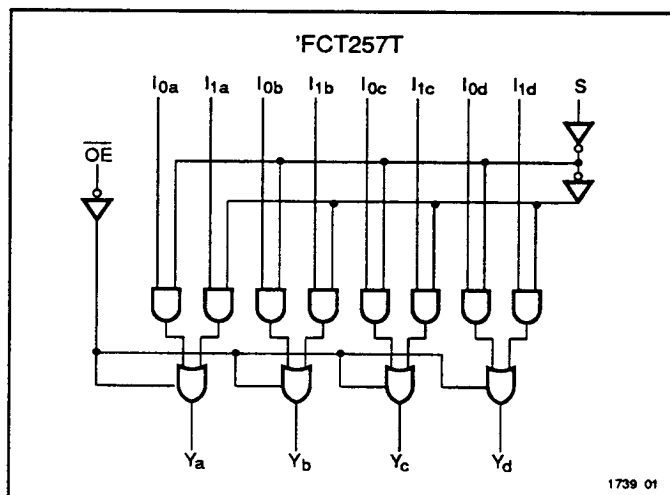
All but one device must be in the High-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

The 'FCT257T/258T is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picoseconds loaded *internal gate delays.

Pace Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

FUNCTIONAL BLOCK DIAGRAM



PERFORMANCE
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2/13/92 - 3

'FCT257T

DIP (P10, D10)
SOIC (S10)

LCC (L10)

1739 03

'FCT258T

DIP (P10, D10)
SOIC (S10)

LCC (L10)

1739 04

ABSOLUTE MAXIMUM RATINGS^{1,2}

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1739 Tbl 01

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1739 Tbl 02

2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1739 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1739 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ ¹	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	$I_{IN} = -18mA$
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	$I_{OH} = -12mA$
		Commercial	2.4	3.3		V	MIN	$I_{OH} = -15mA$
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	$I_{OL} = 32mA$
		Commercial		0.3	0.5	V	MIN	$I_{OL} = 48mA$
		Commercial		0.3	0.5	V	MIN	$I_{OL} = 64mA$
I_I	Input HIGH Current				20	μA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	μA	MAX	$V_{IN} = 2.7V$
I_{IL}	Input LOW Current				–5	μA	MAX	$V_{IN} = 0.5V$
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	μA	MAX	$V_{OUT} = 2.7V$
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	μA	MAX	$V_{OUT} = 0.5V$
I_{OS}	Output Short Circuit Current ²		–60	–120	–225	mA	MAX	$V_{OUT} = 0.0V$
I_{OFF}	Power-off Disable				100	μA	0V	$V_{OUT} = 4.5V$
C_{IN}	Input Capacitance ³			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance ³			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$

1739 Tbl 05

Notes:

- Typical limits are at $V_{CC} = 5.0V$, $T_A = +25^\circ C$ ambient.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

- This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ ¹	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f_1 = 0$, Outputs Open
I_{CCD}	Dynamic Power Supply Current ³	0.15	0.25	mA/ mHz	$V_{CC} = \text{MAX}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current ⁵	1.7	4.0	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, One Input Toggling at $f_1 = 10\text{MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, One Input Toggling at $f_1 = 10\text{MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
		1.7	4.0 ⁴	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, Four Bits Toggling at $f_1 = 2.5\text{MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.7	8.0 ⁴	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, Four Bits Toggling at $f_1 = 2.5\text{MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

1739 Tbl 06

Notes:

- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_1/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_1 = Input Frequency

N_1 = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLE

Inputs				Output	
$\overline{OE}$	S	I_0	I_1	Y	$\overline{Y}$
H	X	X	X	Z	Z
L	H	X	L	L	H
L	H	X	H	H	L
L	L	L	X	L	H
L	L	H	X	H	L

1739 Tbl 07

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High impedance (OFF) state

DEFINITION OF FUNCTIONAL TERMS

Pins	Description
$I_{0n} - I_{1n}$	Data inputs
S	Common select input
$\overline{OE}$	Enable input (Active-Low)
$Y_a - Y_d$	Data outputs 'FCT257T
$\overline{Y}_a - \overline{Y}_d$	Data outputs 'FCT258T

1739 Tbl 08

AC CHARACTERISTICS ('FCT257T)

Sym.	Parameter	'FCT257T				'FCT257AT				'FCT257CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.		
t_{PLH} t_{PHL}	Prop Delay I_{na}, I_{nb} to Y_n	1.5	7.0	1.5	6.0	1.5	5.8	1.5	5.0	1.5	5.0	1.5	4.3	ns	1, 3
t_{PLH} t_{PHL}	Prop Delay S to O_n	1.5	12.0	1.5	10.5	1.5	8.1	1.5	7.0	1.5	6.0	1.5	5.2	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time to High or Low	1.5	10.0	1.5	8.5	1.5	8.0	1.5	7.0	1.5	6.8	1.5	6.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time from High or Low	1.5	8.0	1.5	6.0	1.5	5.8	1.5	5.5	1.5	5.3	1.5	5.0	ns	1, 7, 8

1739 Tbl 09

AC CHARACTERISTICS ('FCT258T)

Sym.	Parameter	'FCT258T				'FCT258AT				'FCT258CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.		
t_{PLH} t_{PHL}	Prop Delay I_{na}, I_{nb} to Y_n	1.5	7.5	1.5	6.5	1.5	6.3	1.5	5.5	1.5	5.5	1.5	4.8	ns	1, 2
t_{PLH} t_{PHL}	Prop Delay S to O_n	1.5	12.5	1.5	11.0	1.5	8.6	1.5	7.5	1.5	6.5	1.5	5.7	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time to High or Low	1.5	10.5	1.5	9.0	1.5	8.5	1.5	7.5	1.5	7.3	1.5	6.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time from High or Low	1.5	8.5	1.5	6.5	1.5	6.3	1.5	6.0	1.5	5.8	1.5	5.5	ns	1, 7, 8

1739 Tbl 10

ORDERING INFORMATION

PxxFCT	xxxx	x	x		
Temp. Class	Device type	Package	Processing		
				Blank	Commercial
				M	Military Temperature
				B	MIL-STD-883, Class B
				P	Plastic DIP
				D	CERDIP
				SO	Small Outline IC
				L	Leadless Chip Carrier
				257 T	Quad 2-line to 1-line Data Selector/Multiplexer (Non-Inverting)
				258 T	Quad 2-line to 1-line Data Selector/Multiplexer (Inverting)
				257 AT	Fast Quad 2-line to 1-line Data Selector/Multiplexer (Non-Inverting)
				258AT	Fast Quad 2-line to 1-line Data Selector/Multiplexer (Inverting)
				257 CT	Ultra Fast Quad 2-line to 1-line Data Selector/Multiplexer (Non-Inverting)
				258 CT	Ultra Fast Quad 2-line to 1-line Data Selector/Multiplexer (Inverting)
				74	Commercial
				54	Military

1739 05