FREQUENCY DEVICES™

# 874 SERIES DIGITALLY PROGRAMMABLE HIGHPASS ACTIVE FILTERS

DS-00874-00

## FEATURES

**4-Pole Highpass Butterworth, and Chebyscheff Models featuring:**

- **Digitally Programmable Corner Frequency via CMOS Interface Logic**
- **Internally Latched Control Lines to Store Frequency Selection Data**
- **Most Widely Used Transfer Characteristics for Broadest Application Scope**
- **Plug-in Ready-to-Use Fully Finished Filter Component**

## APPLICATIONS

- **Programmable Automatic Test Equipment (A.T.E.) Systems**
- **Data Acquisition Systems**
- **Real and Compressed Time Data Analysis**
- **Production Test Systems**
- **Industrial Process Control**

## GENERAL DESCRIPTION

The **874 Series** are digitally-programmable highpass active filters that are tunable over a 256:1 frequency range. These units contain 8-bit CMOS clocked "D" latches which can be digitally configured to operate in any of three modes:

a) Transfer frequency control input data into the latches on the STROBE (or CLOCK) rising edge.

b) As above, but on the STROBE falling edge.

c) Continuously follow the frequency tuning input data, in a non-latching transparent mode.

Fifteen models offer a choice of 4-pole Butterworth, and Chebycheff transfer characteristics. Each is available with any single factory-set tuning range listed below:

– 1 Versions: 0.1Hz to 25.6Hz
– 2 Versions: 1.0hz to 256Hz
– 3 Versions: 10Hz to 2560Hz
– 4 Versions: 100Hz to 25.6kHz
– 5 Versions: 200Hz to 51.2kHz

All **874 Series** models are fully finished filters which require no external components or adjustments, and operate from non-critical ±12 to ±18V power supplies. A 20KΩ input impedance and a 10Ω (max.) output impedance make these compact (2.0"W x 4.0"L footprint, by 0.4"H or 0.6"H) encapsulated plug-in modules convenient and easy to use.

### CONDENSED FREQUENCY SELECTION TABLE

| MSB | --- | --- | --- | --- | --- | --- | LSB | <– Bit Weight |
|---|---|---|---|---|---|---|---|---|
| $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ | Corner Frequency (fc) |
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | fmax/256 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | fmax/64 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | fmax/16 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | fmax/2 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | fmax |

**Five of the possible 256 frequency selection codes.**



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**ANALOG SPECIFICATIONS (Typical @ 25°C & ±15Vdc unless otherwise noted)**

| | |
|---|---|
| **RESPONSE CHARACTERISTICS** | |
| Full Power Response | 100Khz |
| Gain Polarity | Non-inverting |
| Gain Tolerance | |
| @ Passband Gain | See Table A. |
| @ −3dB Corner Freq. $f_C$ | See Table A. |
| @ −70dB Frequency $f_{70dB}$ | See Table A. |
| Tuning Characteristics | |
| Programming Range | Fmax/256 to Fmax |
| *Step Size (Resolution) | Fmax/256 |
| Stability | ±0.01%/°C |
| **ATTENUATION CHARACTERISTICS** | |
| Gain vs. Frequency Plot | See Figures 1, 2, 3, 4 |
| Gain, Phase and Delay Data | See Tables 1, 2, 3, 4 |
| **ANALOG INPUT CHARACTERISTICS** | |
| Impedance | 20KΩ |
| Voltage Range | ±10V |
| Maximum Safe Voltage | ±Vs |
| **ANALOG OUTPUT CHARACTERISTICS** | |
| Resistance | 10Ω max. |
| Linear Operating Range | ±10V |
| Maximum Current | ±2mA |
| Offset Voltage | 2mV typ., 20mV max. |
| Offset vs. Temperature | See discussion, next page. |
| Noise | 50μV RMS |
| **POWER SUPPLY (±Vs)** | |
| Rated Voltage | ±15Vdc |
| Operating Range | ±12 to ±18Vdc |
| Maximum Safe Voltage | ±18Vdc |
| Quiescent Current | 20mA max. |
| **TEMPERATURE** | |
| Operating | 0°C to +70°C |
| Storage | −25°C to +85°C |

**Notes:**
1. Input and output signal voltages are referenced to supply common.
2. Output is short circuit protected to common. DO NOT CONNECT TO ±Vs.
3. Measured in a 5Hz to 50kHz bandwidth.

**Table A. Deviations from theoretical responses**

| Characteristic Response | Pass Band Gain -A- | At fc, the −3dB Corner Frequency -B- | At $f_{70dB}$, Frequency for −70dB Gain -C- |
|---|---|---|---|
| Butterworth | ±0.5dB | ±0.2dB | ±2dB |
| 0.2dB Chebycheff | ±0.5dB | ±0.6dB | ±3dB |
| 0.5dB Chebycheff | ±0.5dB | ±0.8dB | ±3dB |

The above table defines highpass responses having a pass band gain of 0dB ±A (the value in column A), a gain of −3dB ±B at corner frequency $f_C$, and a gain of −70dB ±C at $f_{70dB}$, the frequency for a theoretical gain of −70dB.

In general, filters programmed at frequencies below 20kHz fall well within the above deviation boundaries. These error bounds on the filter transfer characteristics are approached only as the programmed frequencies reach 20kHz and above.





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## DC OFFSET vs. TEMPERATURE

The DC offset voltage of **874 Series** filters originates at two internal sources that cause it to vary with temperature and selected frequency. Slight mismatches between operational amplifier (op amp) semiconductor junctions create the first source of DC offset. Switching element leakage currents flowing through switch-selected tuning resistors predominate as the second source of DC offset. Though small at 25° C, the switch leakage currents increase exponentially with absolute temperature to become significantly large at higher temperatures. This becomes a problem when the filter is tuned to low frequencies, which require high-value tuning resistors.

Figure A illustrates the worst case temperature behavior of the offset voltage; this improves with higher frequency codes. The maximum DC offset voltage will generally occur at the highest temperature and the lowest corner frequency (all "0" input code). This recommends the user to select the model with the LOWEST CORNER FREQUENCY possible.

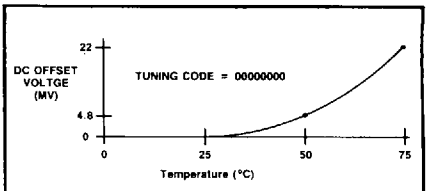


Figure A. The DC offset voltage drift varies with tuning code. Turning on the LSB would halve the maximum DC offset. See discussion.

## USER NOTES

**Grounding:** To achieve specified precision, all analog and digital grounds are connected internal to the filter. Should this cause a problem, all digital inputs (C, P, and $D_0$ - $D_7$) can be optically isolated.

**Settling Time:** When tuned to a different frequency, a filter requires sufficient transient settling time corresponding to several cycles of the new frequency. PLEASE NOTE: DO NOT use these filters in frequency scanning applications without considering settling time.

### DATA CONTROL CHARACTERISTICS

| | | |
|---|---|---|
| **Data Control Lines** | | |
| Functions | Latch Strobe (C)<br>Transition Polarity (P) | |
| **Data Control Modes** | | |
| Mode 1 | P = 0; C = 0 | frequency follows input codes |
| | P = 0; C = 0 −>1 | frequency latched on rising edge |
| Mode 2 | P = 1; C = 1 | frequency follows input codes |
| | P = 1; C = 1 −>0 | frequency latched on falling edge |
| **INPUT DATA LEVELS (CMOS Logic)** | | |
| **Input Voltage (Vs = 15V)** | **Min.** | **Max. Acceptable** |
| Low Level In | 0 Volts | 4 Volts |
| High Level In | 11 Volts | 15 Volts |
| **Input Current** | **Typ.** | **Max.** |
| High Level In | $-10^{-5}$ μA | −1μA |
| Low Level In | $+10^{-5}$μA | +1μA |
| **Input Capacitance** | 5pF | 7.5pf |
| **Latch Response** | | |
| Data Set Up Time[1] | 25 ns | — |
| Data Hold Time[2] | 50 ns | — |
| Strobe | | |
| Min Pulse Width | 80 ns | — |

**Notes:** 1. The time data must be present before occurence of strobe edge.
2. The time data must be present after occurence of strobe edge.



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## DIGITAL TUNING CHARACTERISTICS

The digital tuning interface circuits are two 4042 quad CMOS latches which accept the following CMOS-compatible inputs: eight tuning bits ($D_0$ - $D_7$), a latch strobe bit (C), and a transition polarity bit (P).

Filter tuning follows the tuning equation given below:

$$fc = (fmax/256)\,[1 + D_7*2^7 + D_6*2^6 + D_5*2^5 + D_4*2^4 + D_3*2^3 + D_2*2^2 + D_1*2^1 + D_0*2^0]$$

where $D_0$ – $D_7$ = Logic "0" or "1", and
fmax = maximum tunable frequency
fc = corner frequency
Minimum tunable frequency = fmax/256 ($D_0 -> D_7 = 0$)
Minimum frequency step (Resolution) = fmax/256

## INPUT DATA FORMAT

### Frequency Select Bits

| | | |
|---|---|---|
| Positive Logic | Logic "1" = +Vs<br>Logic "0" = Gnd | Logic threshold typ. = 0.45Vs |
| Bit Weighting (Binary-Coded) | $D_0$ = least significant bit (LSB)<br>$D_7$ = most significant bit (MSB) | |
| Frequency Range | 256:1, Binary Weighted | |

## DIGITAL FREQUENCY SELECTION

**Table 7. Nine of the 256 possible frequency selection codes**

| MSB | --- | --- | --- | --- | --- | --- | LSB | <– Bit Weight |
|---|---|---|---|---|---|---|---|---|
| $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ | Corner Frequency (fc) |
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | fmax/256 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | fmax/128 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | fmax/64 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | fmax/32 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | fmax/16 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | fmax/8 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | fmax/4 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | fmax/2 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | fmax |





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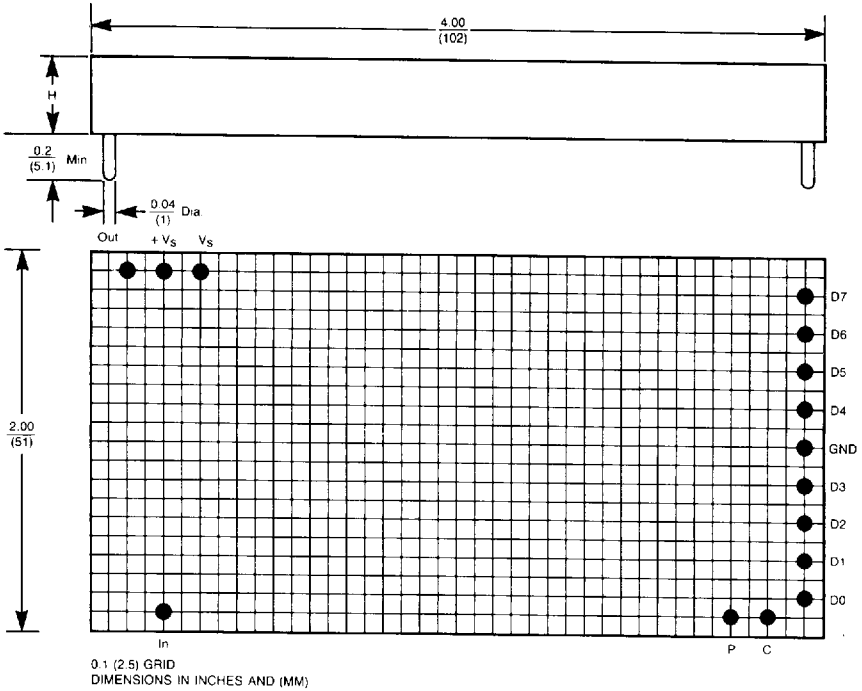


**PACKAGE AND PIN-OUT DATE**
**DIMENSIONS**
**IN INCHES (MM)**

SIDE VIEW
BOTTOM VIEW
0.1 INCH GRID

**CASE DIMENSIONS. ALL 874 SERIES AND (MM)**

| CASE | DIMENSIONS IN INCHES AND (MM) |
|---|---|
| M-1 | 2.0″W x 4.0″L x 0.6″H (51 x 102 x 15 mm) |
| M-2 | 2.0″W x 4.0″L x 0.4″H (51 x 102 x 10 mm) |

**TERMINAL KEY**

| | |
|---|---|
| In | Analog Input Signal |
| Out | Analog Output Signal |
| GND | Power and Signal Return |
| "P" | Transition Polarity Bit |
| "C" | Tuning Strobe Bit |
| + Vs | Supply Voltage, Positive |
| – Vs | Supply Voltage, Negative |

| | |
|---|---|
| $D_0$ | Tuning Bit 0 (LSB) |
| $D_1$ | Tuning Bit 1 |
| $D_2$ | Tuning Bit 2 |
| $D_3$ | Tuning Bit 3 |
| $D_4$ | Tuning Bit 4 |
| $D_5$ | Tuning Bit 5 |
| $D_6$ | Tuning Bit 6 |
| $D_7$ | Tuning Bit 7 (MSB) |



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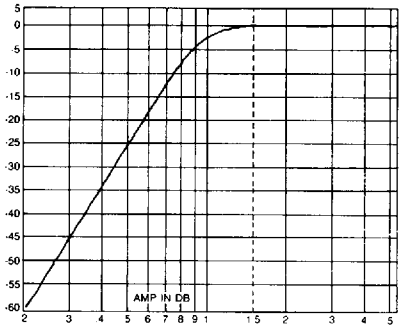
## BUTTERWORTH RESPONSE CURVE..




## NORMALIZED THEORETICAL DATA TABLES

**Table 1. 4-POLE BUTTERWORTH**

| f/fc | AMP (dB) | PHASE (deg) | DELAY (sec) |
|---|---|---|---|
| 0.00 | -∞ | 360.0 | 0.416 |
| 0.10 | -80.0 | 345.0 | 0.418 |
| 0.20 | -55.9 | 330.0 | 0.423 |
| 0.30 | -41.8 | 314.5 | 0.433 |
| 0.40 | -31.8 | 298.6 | 0.449 |
| 0.50 | -24.1 | 282.0 | 0.474 |
| 0.60 | -17.8 | 264.3 | 0.511 |
| 0.70 | -12.6 | 245.1 | 0.558 |
| 0.80 | -8.4 | 224.1 | 0.604 |
| 0.90 | -5.2 | 201.9 | 0.622 |
| 1.00 | -3.0 | 180.0 | 0.588 |
| 1.20 | -0.9 | 143.2 | 0.427 |
| 1.50 | -0.2 | 108.3 | 0.241 |
| 1.70 | -0.1 | 93.5 | 0.175 |
| 2.00 | -0.0 | 78.0 | 0.119 |
| 2.50 | -0.0 | 61.4 | 0.072 |
| 3.00 | -0.0 | 50.7 | 0.049 |
| 4.00 | -0.0 | 37.8 | 0.027 |
| 5.00 | -0.0 | 30.1 | 0.017 |
| 6.00 | -0.0 | 25.1 | 0.012 |
| 7.00 | -0.0 | 21.4 | 0.009 |
| 8.00 | -0.0 | 18.8 | 0.006 |
| 9.00 | -0.0 | 16.7 | 0.005 |
| 10.0 | -0.0 | 15.0 | 0.004 |





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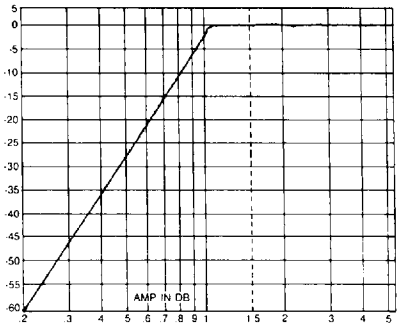
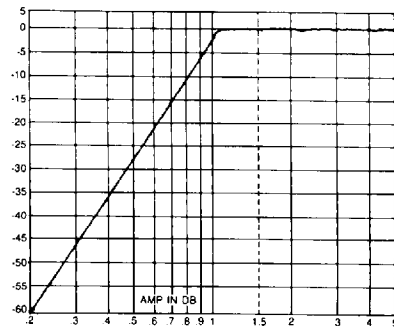
FREQUENCY DEVICES™

# 874 SERIES THEORETICAL HIGHPASS 0.2 & 0.5dB CHEBYCHEFF RESPONSES

**0.2dB RESPONSE CURVE..**




**0.5dB RESPONSE CURVE..**




## NORMALIZED THEORETICAL DATA TABLES

**Table 2. 0.2dB CHEBYCHEFF**

| f/fc | AMP (dB) | PHASE (deg) | DELAY (sec) |
|---|---|---|---|
| 0.00 | -∞ | 000.0 | 0.478 |
| 0.10 | -89.8 | 352.4 | 0.487 |
| 0.20 | -65.5 | 345.7 | 0.509 |
| 0.30 | -51.1 | 336.7 | 0.533 |
| 0.40 | -40.6 | 328.2 | 0.547 |
| 0.50 | -32.2 | 318.9 | 0.533 |
| 0.60 | -25.0 | 308.4 | 0.575 |
| 0.70 | -18.6 | 296.0 | 0.654 |
| 0.80 | -12.7 | 280.3 | 0.833 |
| 0.90 | -7.3 | 259.1 | 1.02 |
| 1.00 | -3.0 | 230.5 | 0.873 |
| 1.20 | 0.1 | 172.3 | 0.385 |
| 1.50 | 0.0 | 127.7 | 0.158 |
| 1.70 | 0.0 | 111.0 | 0.107 |
| 2.00 | 0.1 | 93.3 | 0.067 |
| 2.50 | 0.2 | 73.4 | 0.039 |
| 3.00 | 0.2 | 60.4 | 0.026 |
| 4.00 | 0.2 | 44.5 | 0.014 |
| 5.00 | 0.1 | 35.2 | 0.009 |
| 6.00 | 0.1 | 29.2 | 0.006 |
| 7.00 | 0.1 | 24.9 | 0.004 |
| 8.00 | 0.1 | 21.7 | 0.003 |
| 9.00 | 0.1 | 19.3 | 0.003 |
| 10.0 | 0.0 | 17.3 | 0.002 |

**Table 3. 0.5dB CHEBYCHEFF**

| f/fc | AMP (dB) | PHASE (deg) | DELAY (sec) |
|---|---|---|---|
| 0.00 | -∞ | 000.0 | 0.172 |
| 0.10 | -91.9 | 353.8 | 0.174 |
| 0.20 | -65.6 | 347.4 | 0.179 |
| 0.30 | -53.1 | 340.8 | 0.188 |
| 0.40 | -42.6 | 333.8 | 0.203 |
| 0.50 | -34.1 | 326.1 | 0.226 |
| 0.60 | -26.8 | 317.4 | 0.263 |
| 0.70 | -20.2 | 306.9 | 0.326 |
| 0.80 | -14.0 | 293.3 | 0.440 |
| 0.90 | -8.1 | 274.0 | 0.651 |
| 1.00 | -3.0 | 245.3 | 0.946 |
| 1.20 | 0.5 | 178.9 | 0.693 |
| 1.50 | 0.0 | 133.2 | 0.271 |
| 1.70 | 0.0 | 116.6 | 0.199 |
| 2.00 | 0.3 | 98.2 | 0.146 |
| 2.50 | 0.5 | 72.9 | 0.095 |
| 3.00 | 0.5 | 62.7 | 0.065 |
| 4.00 | 0.4 | 45.5 | 0.035 |
| 5.00 | 0.3 | 35.7 | 0.021 |
| 6.00 | 0.2 | 29.4 | 0.014 |
| 7.00 | 0.2 | 25.0 | 0.010 |
| 8.00 | 0.1 | 21.8 | 0.008 |
| 9.00 | 0.1 | 19.3 | 0.006 |
| 10.0 | 0.1 | 17.3 | 0.005 |



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## AVAILABLE 874 HIGH PASS MODELS

**Butterworth Versions**

| BUTTERWORTH | NO. POLES | TUNING (HZ) RANGE | Min. STEP | CASE |
|---|---|---|---|---|
| 874P8B-1 | 4 | 0.1 to 25.6 | 0.1 | M-1 |
| 874P8B-2 | 4 | 1.0 to 256 | 1.0 | M-2 |
| 874P8B-3 | 4 | 10 to 2560 | 10 | M-2 |
| 874P8B-4 | 4 | 100 to 25.6k | 100 | M-2 |
| 874P8B-5 | 4 | 200 to 51.2k | 200 | M-2 |
| Figure 1 and Table 1 | ← TRANSFER CHARACTERISTICS | | | |

**Chebycheff Versions**

| PASSBAND RIPPLE 0.2dB | 0.5dB | NO. POLES | TUNING (Hz) RANGE | MIN. STEP | CASE |
|---|---|---|---|---|---|
| 874P8YA2W-1 | 874P8YA5W-1 | 4 | 0.1 to 25.6 | 0.1 | M-1 |
| 874P8YA2W-2 | 874P8YA5W-2 | 4 | 1.0 to 256 | 1.0 | M-2 |
| 874P8YA2W-3 | 874P8YA5W-3 | 4 | 10 to 2560 | 10 | M-2 |
| 874P8YA2W-4 | 874P8YA5W-4 | 4 | 100 to 25.6k | 100 | M-2 |
| 874P8YA2W-5 | 874P8YA5W-5 | 4 | 200 to 51.2k | 200 | M-2 |
| Figure 2 and Table 2 | Figure 3 and Table 3 | ← TRANSFER CHARACTERISTICS | | | |

### HOW TO ORDER

The above tables list the fifteen **874 Series** models and the sets of transfer characteristics, frequency range and tuning resolution that distinguish between models. Selection is the simple matter of choosing the filter model with the frequency response, range and resolution required by the application. NOTE: SELECT THE LOWEST FREQUENCY MODEL THAT SPANS THE FREQUENCY RANGE OF INTEREST FOR LOWEST DC OFFSET AND BEST FILTER PERFORMANCE.





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