P54/74PCT377/A
OCTAL D FLIP-FLOP WITH CLOCK ENABLE

PRELIMINARY

T-46-07-11

FEATURES

- Full CMOS Implementation
- Low Power Operation
- Clock Enable for Address and Data Synchronization Application
- Eight Edge-Triggered D Flip-Flops
- Fully TTL Compatible Input and Output Levels
- 3-State Output
- Produced with PACE II Technology™
- Conventional Pinout
  - 20-Pin 300 mil DIP, SOIC
  - 20-Pad 350 mil sq. LCC

DESCRIPTION

The P54/74PCT377/A have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

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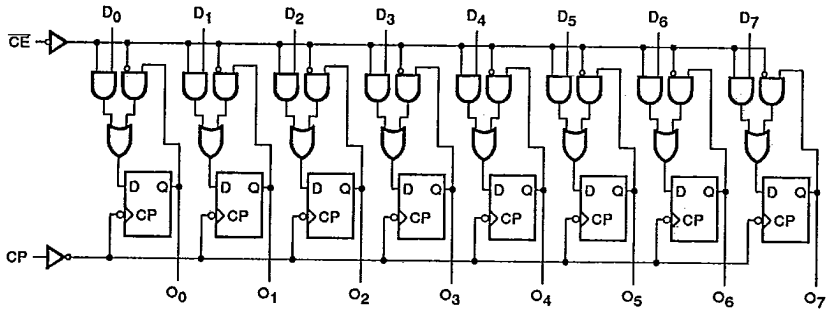
FUNCTIONAL BLOCK DIAGRAM



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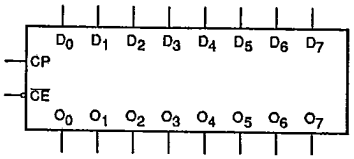
LOGIC SYMBOL



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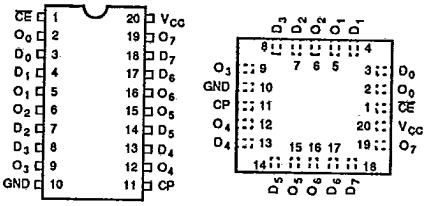
PIN CONFIGURATIONS



DIP (D2, P2), SOIC (S2) LCC (L2)

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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–55 to +125	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	100	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

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Notes:
1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		–0.5		0.8	V		
V_H	Hysteresis			.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage				–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2			V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2			V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.7			V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V			0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)			0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)			0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)			0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied				10	µA	MAX	V_{OUT} = V_{CC}
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied				–10	µA	MAX	V_{OUT} = GND
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied[3]				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied[3]				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60			mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

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Notes:
1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs) Com'l Mil	.003 .003	0.3 0.5	mA mA	V_{CC} = MAX, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, f = 0, Outputs Open
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)		2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ mHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, $\overline{CE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, Outputs Open
I_{CC}	Total Power Supply Current[5]		4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{CE}$ = GND and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{CE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND
			7.8[4]	mA	V_{CC} = MAX, f_0 = 1.0MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{CE}$ = GND and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			16.8[4]	mA	V_{CC} = MAX, f_0 = 1.0MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{CE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQC} + I_{CCQT} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CCQC} = Quiescent Current with CMOS input levels
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	X	H	X	No Change

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H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

AC CHARACTERISTICS

Symbol	Parameter	P54/74PCT377					P54/74PCT377A					Units	Fig. No.
		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L			
		Typ.	Min.[1]	Max.	Min.[1]	Max.	Typ.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH}	Propagation Delay	7.0	2.0	15.0	2.0	13.0	5.0	2.0	8.3	2.0	7.2	ns	1
t_{PHL}	Clock to Output	7.0	2.0	15.0	2.0	13.0	5.0	2.0	8.3	2.0	7.2	ns	5

Note: AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

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AC OPERATING REQUIREMENTS

Symbol	Parameter	P54/74PCT377					P54/74PCT377A					Units	Fig. No.
		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L		T_A=+25°C V_{CC}=+5.0V	MIL		COM'L			
		Typ.	Min.	Max.	Min.	Max.	Typ.	Min.	Max.	Min.	Max.		
t_s(H)	Setup Time, HIGH	1.0	3.0		2.5		1.0	2.0		2.0		ns	4
t_s(L)	or LOW Data to CP	1.0	3.0		2.5		1.0	2.0		2.0			
t_h(H)	Hold Time, HIGH	1.0	2.5		2.0		1.0	1.5		1.5		ns	4
t_h(L)	or LOW Data to CP	1.0	2.5		2.0		1.0	1.5		1.5			
t_w(H)	Setup Time, HIGH	1.5	3.0		3.0		1.0	2.0		2.0		ns	5
t_w(L)	or LOW $\overline{CE}$ to CP	1.5	3.0		3.0		1.0	2.0		2.0			
t_w(H)	Hold Time, HIGH	3.0	5.0		4.0		1.0	2.0		2.0		ns	6
t_w(L)	or LOW $\overline{CE}$ to CP	3.0	5.0		4.0		1.0	2.0		2.0			
t_w(L)	Clock Pulse Width LOW[2]	4.0	7.0		7.0		4.0	7.0		6.0		ns	6

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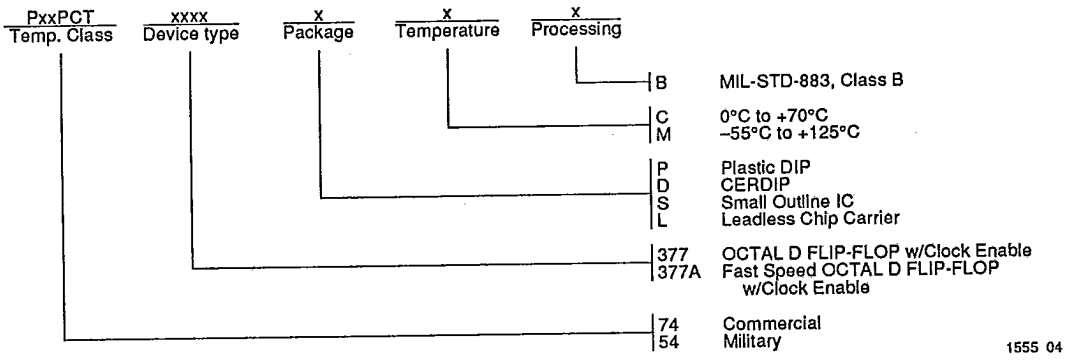
Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. With one data channel toggling, t_w(L) = t_w(H) = 2.0ns and t_r = t_f = 1.0ns.

ORDERING INFORMATION



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