P54/74FCT480/A/B (P54/74PCT480/A/B)
P54/74FCT481/A/B (P54/74PCT481/A/B)
DUAL ODD-PARITY, DUAL EVEN-PARITY GENERATOR/CHECKERS

FEATURES

- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-A speed at 7.5ns max. (Com'l)**
  FCT-B speed at 5.6ns max. (Com'l)
- **CMOS V_{OH} Levels for Low Power Consution**
  —Typically 1/3 of Fast Bipolar Logic
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **ESD protection exceeds 2000V**
- **64 mA Sink Current (Com'l), 32 mA (Mil)**
  15 mA Source Current (Com'l), 12 mA (Mil)
- **Two 8-Bit Parity Generator/Checkers Per Device**
- **Open Drain Low-Active Parity Error Output**
- **Expandable For Larger Word Widths**
- **Manufactured in 0.7 micron PACE Technology™**

DESCRIPTION

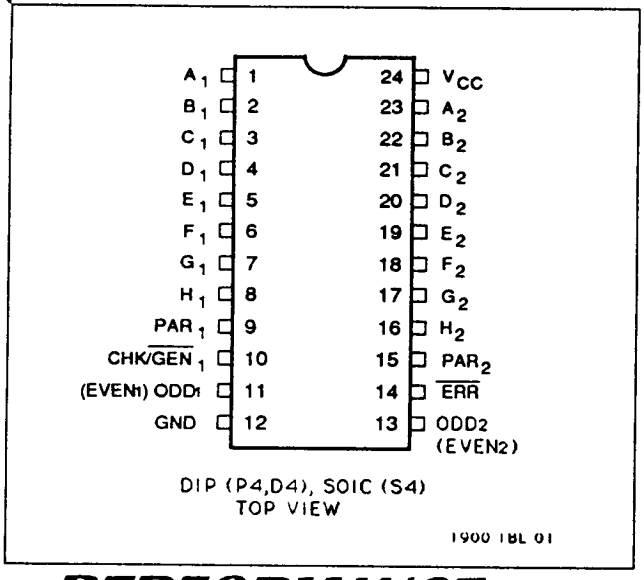
The 'FCT480 and 'FCT481 are high speed dual 8-bit parity generator/checkers. Each parity generator/checker accepts eight data bits and one parity bit as inputs, and generates a parity and a parity error output. The 'FCT480 generates and checks odd parity, while the 'FCT481 generates and checks even parity. In the CHECK mode, the parity output for each generator in the 'FCT480 ('FCT481) is low whenever an odd (even) number of inputs is high; the common parity error output in the 'FCT480 or the 'FCT481 is low, indeicating an error, if either of the generated parity outputs is high. In the GENERATE mode, the two input parity bits are disabled and each device functions as in the CHECK mode.

The parity error output is open-drain, designed for easy expansion of the word width by a simple wired-OR connection of several 'FCT480 and 'FCT481 type devices. Since additional logic is not needed, the parity generation and checking times remain the same as for each 'FCT480 device.

The 'FCT480 and 'FCT481 are manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picoseconds loaded* internal gate delays.

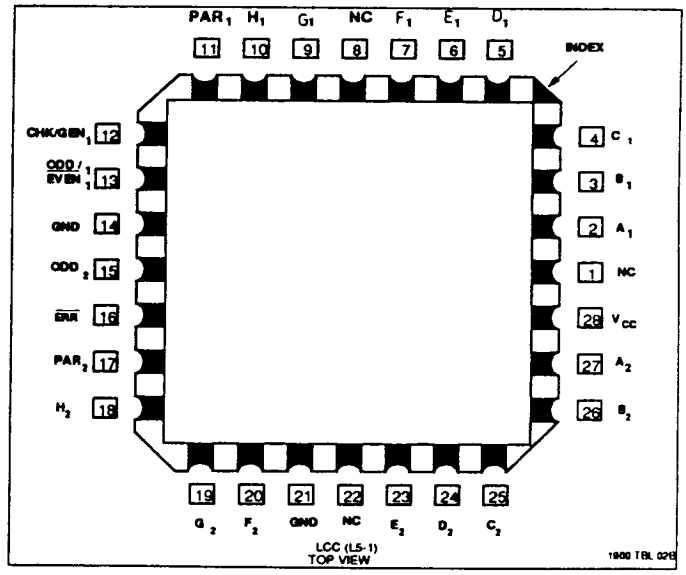
The 'FCT480 and 'FCT481 are available in 24-pin 300 mil DIP and SOIC packages providing excellent board level densities.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.



DIP (P4,D4), SOIC (S4)
TOP VIEW

1900 TBL 01



LCC (L5-1)
TOP VIEW

1900 TBL 02B

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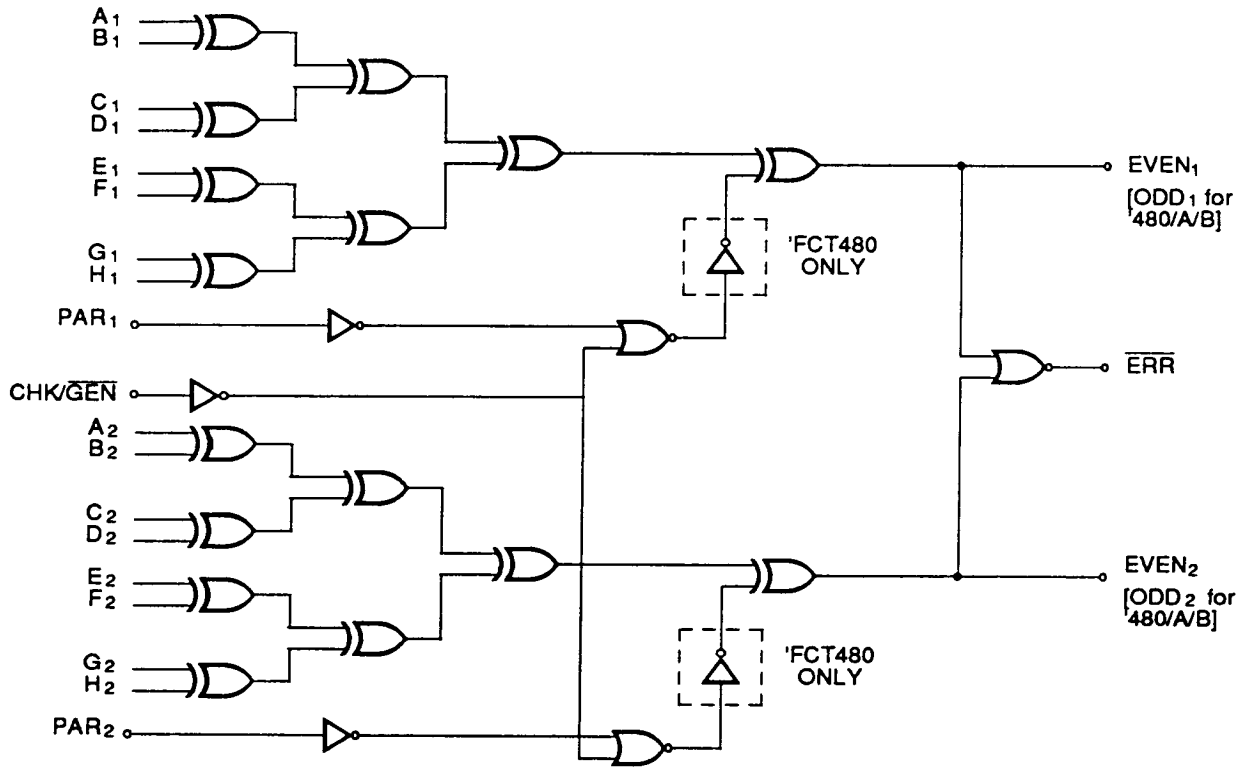
Means Quality, Service and Speed

6/1/92-4

FUNCTIONAL BLOCK DIAGRAM



NOTE: Functional description only.
Not representative of propagation delays.

6/1/92-4

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1900 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1900 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS[3]

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1900 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1900 Tbl 04

Notes:

3. Unless otherwise restricted or extended by detail specifications.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2			V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2	V_{CC}		V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4	4.3		V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.7	4.3		V	MIN	I_{OH} = –15mA
	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V		V_{CC} – 0.2			V		I_{OH} = –300µA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			6	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq$ 0.2V, $V_{IN} \geq V_{CC}$–0.2V

1900 Tbl 05

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.2	0.35	mA/MHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	2.0	5.0	mA	V_{CC} = MAX, Outputs Open, One Bit Toggling at f_1 = 2.5MHz, 50% Duty Cycle, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
		2.5	7.0	mA	V_{CC} = MAX, Outputs Open, One Bit Toggling at f_1 = 2.5MHz, 50% Duty Cycle, V_{IN} = 3.4V or V_{IN} = GND
		7.25	13.75	mA	V_{CC} = MAX, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, 50% Duty Cycle, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
		10.25	22.75	mA	V_{CC} = MAX, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, 50% Duty Cycle, V_{IN} = 3.4V or V_{IN} = GND

1551 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CCQC} + \Delta I_{CC} \cdot D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS (Minimum values for propagation delays are 1.5 ns, guaranteed by design)

Symbol	Parameter	'FCT480 'FCT481		'FCT480A 'FCT481A		'FCT480B 'FCT481B		Unit
		Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
t_{PLH}	Propagation Delay	17.0	13.0	9.5	7.5	7.0	5.6	ns
t_{PHL}	A_n to ODD	16.0	13.0	9.0	7.0	6.6	5.6	ns
t_{PLH}*	Propagation Delay	17.0	13.0	9.0	7.0	7.0	5.6	ns
t_{PHL}	A_n to $\overline{ERR}$	20.0	16.0	10.5	8.5	8.1	6.5	ns
t_{PLH}	Propagation Delay	15.0	12.0	8.5	6.5	6.3	5.9	ns
t_{PHL}	CHK/$\overline{GEN}$ to ODD	18.0	15.0	10.0	7.5	7.4	5.9	ns
t_{PLH}*	Propagation Delay	17.0	14.0	9.5	7.5	7.1	5.7	ns
t_{PHL}	CHK/$\overline{GEN}$ to $\overline{ERR}$	16.0	13.0	9.0	7.0	6.9	5.5	ns

*t_{PLH} is measured up to $V_{OUT} = V_{OL} + 0.3V$

1900 Tbl 07

6/1/92-4

'FCT481T TRUTH TABLE

Inputs					Outputs		
A1 to H1	A2 to H2	CHK/nGEN	OPAR1	OPAR2	ODD1	ODD2	nPER
Number of A1 to H1 Inputs HIGH is EVEN	Number of A2 to H2 Inputs HIGH is EVEN	H	H	H	H	H	L
			L	H	L	H	L
			H	L	H	L	L
			L	L	L	L	H
		L	X	X	L	L	H
	Number of Inputs HIGH A2 to H2 is ODD	H	H	H	H	L	L
			L	H	L	L	H
			H	L	H	H	L
			L	L	L	H	L
		L	X	X	L	H	L
Number of A1 to H1 Inputs HIGH is ODD	Number of A2 to H2 Inputs HIGH is EVEN	H	H	H	L	H	L
			L	H	H	H	L
			H	L	L	L	H
			L	L	H	L	L
		L	X	X	H	L	L
	Number of A2 to H2 Inputs HIGH is ODD	H	H	H	L	L	H
			L	H	H	L	L
			H	L	L	H	L
			L	L	H	H	L
		L	X	X	H	H	L

1900 Tbl 08

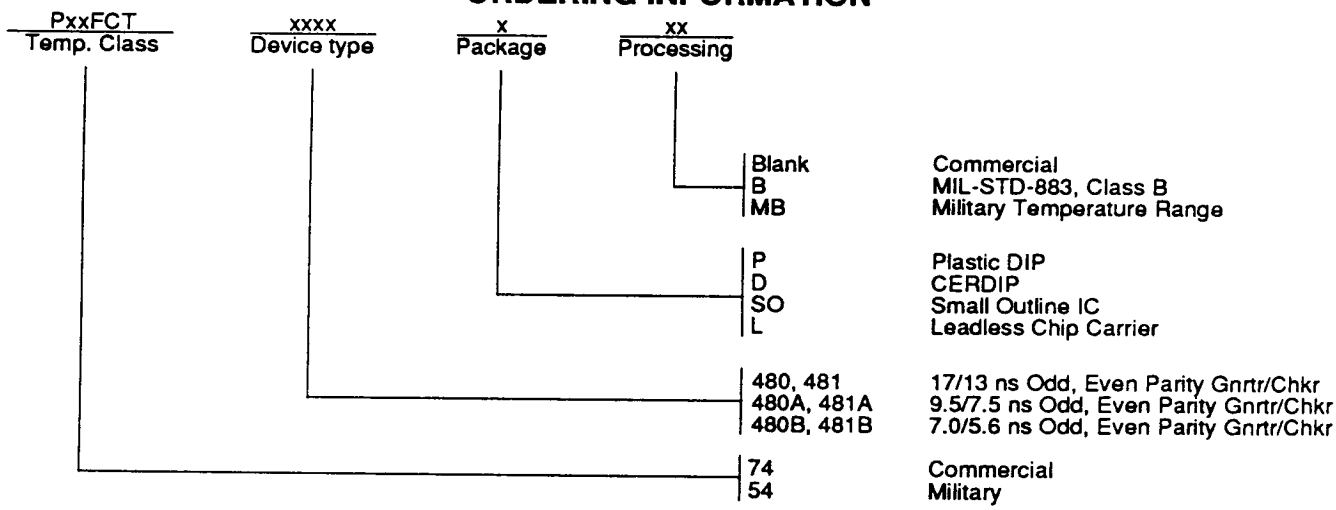
6/1/92-4

'FCT480T TRUTH TABLE

Inputs					Outputs		
A1 to H1	A2 to H2	CHK/nGEN	EPAR1	EPAR2	EVEN1	EVEN2	nPER
Number of A1 to H1 Inputs HIGH is EVEN	Number of A2 to H2 Inputs HIGH is EVEN	H	H	H	L	L	H
			L	H	H	L	L
			H	L	L	H	L
			L	L	H	H	L
		L	X	X	H	H	L
	Number of Inputs HIGH A2 to H2 is ODD	H	H	H	L	H	L
			L	H	H	H	L
			H	L	L	L	H
			L	L	H	L	L
		L	X	X	H	L	L
Number of A1 to H1 Inputs HIGH is ODD	Number of A2 to H2 Inputs HIGH is EVEN	H	H	H	H	L	L
			L	H	L	L	H
			H	L	H	H	L
			L	L	L	H	L
		L	X	X	L	H	L
	Number of A2 to H2 Inputs HIGH is ODD	H	H	H	H	H	L
			L	H	L	H	L
			H	L	H	L	L
			L	L	L	L	H
		L	X	X	L	L	H

1900 Tbl 09

ORDERING INFORMATION



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