

P54/74PCT651/651A P54/74PCT652/652A OCTAL TRANSCEIVERS/REGISTER

T-52-31

FEATURES

- Full CMOS Implementation
- Low Power Operation
- Independent Register for A and B Buses
- Choice of Non-Inverting and Inverting Data Transfer
- Multiplexed Real-Time and Stored Data Transfer
- Bidirectional Bus Transceiver and Registers
- Fully TTL Compatible Input and Output Levels
- 3-State Output
- Produced with PACE Technology™
- Compact Pinout
 - 24-Pin 300 mil DIP, SOIC
 - 28-Pad 450 mil sq. LCC

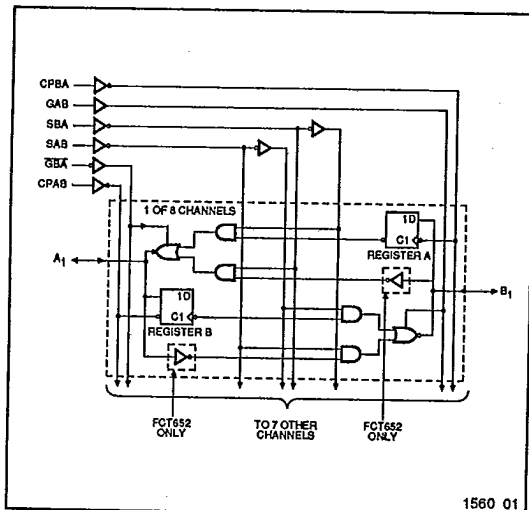
DESCRIPTION

THE P54/74PCT651/A and P54/74PCT652/A consist of bus transceiver circuits, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. GAB and GBA control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

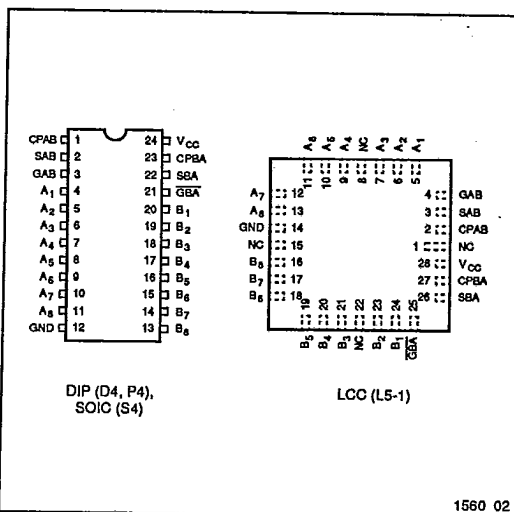
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

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FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



PERFORMANCE
SEMICONDUCTOR CORPORATION

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ABSOLUTE MAXIMUM RATINGS^{1,2}

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +150	°C
T _A	Ambient Temperature Under Bias	-55 to +125	°C
V _{CC}	V _{CC} Potential to Ground	-0.5 to +7.0	V
I _{IN}	Input Current	-30 to +5.0	mA

Notes:

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1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

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Symbol	Parameter	Value	Unit
I _{OUTPUT}	Current Applied to Output	100	mA
V _{IN}	Input Voltage	-0.5 to V _{CC} + 0.5	V
V _{OUT}	Voltage Applied to Output	-0.5 to V _{CC} + 0.5	V

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2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Supply Voltage (V _{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter	Min	Typ ¹	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0		V _{CC} + 0.5	V		
V _{IL}	Input LOW Voltage	-0.5		0.8	V		
V _H	Hysteresis		.35		V		All inputs
V _{CD}	Input Clamp Diode Voltage			-1.2	V	MIN	I _{IN} = -18mA
V _{OH}	Output HIGH Voltage	V _{CC} = 3V, V _{IN} = 0.2V, or V _{CC} - 0.2V		V _{CC} - 0.2	V		I _{OH} = -32μA
		Military/Commercial (CMOS)		V _{CC} - 0.2	V	MIN	I _{OH} = -300μA
		Military (TTL)		2.4	V	MIN	I _{OH} = -12mA
		Commercial (TTL)		2.7	V	MIN	I _{OH} = -15mA
V _{OL}	Output LOW Voltage	V _{CC} = 3V, V _{IN} = 0.2V, or V _{CC} - 0.2V			V		I _{OL} = 300μA
		Military/Commercial (CMOS)		0.2	V	MIN	I _{OL} = 300μA
		Military (TTL)		0.55	V	MIN	I _{OL} = 48mA
		Commercial (TTL)		0.55	V	MIN	I _{OL} = 64mA
I _{IH}	Input HIGH Current			5	μA	MAX	V _{IN} = V _{CC}
I _{IL}	Input LOW Current			-5	μA	MAX	V _{IN} = GND
I _{IH}	Input HIGH Current ³			5	μA	MAX	V _{IN} = 2.7V
I _{IL}	Input LOW Current ³			-5	μA	MAX	V _{IN} = 0.5V
I _{IH}	Input HIGH Current (I/O Pins only)			15	μA	MAX	V _{IN} = V _{CC}
I _{IL}	Input LOW Current (I/O Pins only)			-15	μA	MAX	V _{IN} = GND
I _{IH}	Input HIGH Current ³ (I/O Pins only)			15	μA	MAX	V _{IN} = 2.7V
I _{IL}	Input LOW Current ³ (I/O Pins only)			-15	μA	MAX	V _{IN} = 0.5V
I _{OS}	Output Short Circuit Current ²	-60			mA	MAX	V _{OUT} = 0.0V
C _{IN}	Input Capacitance ³		5	10	pF		All inputs
C _{OUT}	Output Capacitance ³		9	12	pF		All outputs

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Notes:

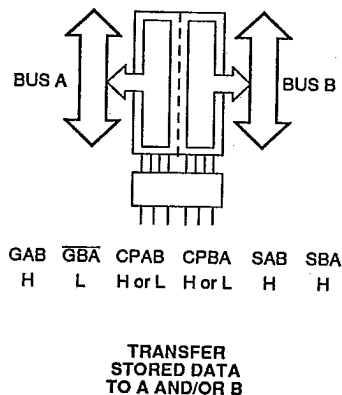
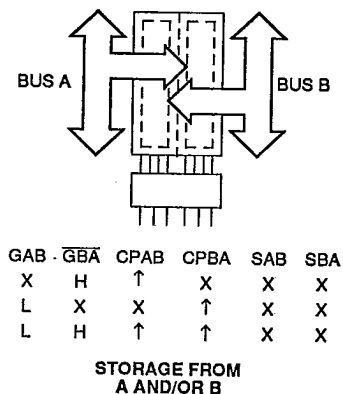
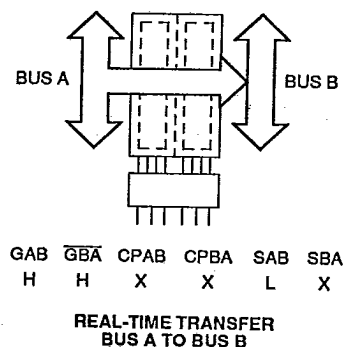
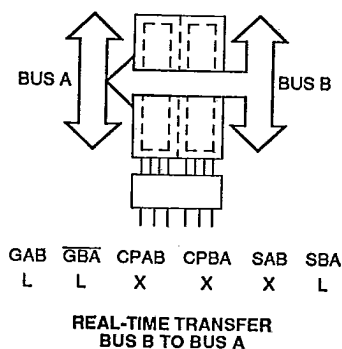
1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.

2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

3. This parameter is guaranteed but not tested.

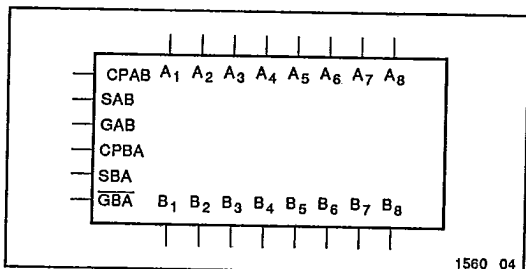
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LOGIC SYMBOL



PIN DESCRIPTION

Pin Names	Description
A ₁ –A ₈	Data Register Inputs Data Register A Outputs
B ₁ –B ₈	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
GAB, $\overline{\text{GBA}}$	Output Enable Inputs

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FUNCTION TABLES

Inputs						Data I/O		Operation or Function	
GAB	GBA	CPAB	CPBA	SAB	SBA	A ₁ thru A ₈	B ₁ thru B ₈	FCT651/A	FCT652/A
L	H	H or L	H or L	X	X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified ¹ Output	Store A, Hold B Store A in both registers	Store A, Hold B Store A in both registers
L	X	H or L	↑	X	X	Unspecified ¹ Output	Input	Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus	Real-Time B Data to A Bus Stored B Data to A Bus
L	L	X	H or L	X	H				
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus	Real-Time A Data to B Bus Stored A Data to B Bus
H	H	H or L	X	H	X				
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

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Notes:

- The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.
H = HIGH, L = LOW, X = Don't Care, ↑ LOW-to-HIGH Transition

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ ¹	Max	Units	Conditions
I_{CCOC}	Quiescent Power Supply Current (CMOS inputs)	.003 Com ¹ l Mil	0.3 0.5	mA mA	$V_{CC} = \text{MAX}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, $f = 0$, Outputs Open
I_{CCOT}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f = 0$, Outputs Open
I_{CCD}	Dynamic Power Supply Current ³		0.25	mA/ MHz	$V_{CC} = \text{MAX}$, One Input Toggling, 50% Duty Cycle, $GAB = GND$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, Outputs Open $G\bar{B}A = GND$, $SAB = CPAB = GND$, and $SBA = V_{CC}$
I_{CC}	Total Power Supply Current ⁵		4.0	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$, $GAB = GND$, $G\bar{B}A = GND$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, $SAB = CPAB = GND$, and $SBA = V_{CC}$
			6.0	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$, $GAB = GND$, $G\bar{B}A = GND$, $V_{IN} = 3.4V$ or $V_{IN} = GND$, $SAB = CPAB = GND$, and $SBA = V_{CC}$
			7.8 ⁴	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz}$, $GAB = GND$, $G\bar{B}A = GND$, $V_{IN} = 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, $SAB = CPAB = GND$, and $SBA = V_{CC}$
			16.8 ⁴	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz}$, $GAB = GND$, $G\bar{B}A = GND$, $V_{IN} = 3.4V$ or $V_{IN} = GND$, $SAB = CPAB = GND$, and $SBA = V_{CC}$

Notes:

- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient and maximum loading.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

$$I_{CC} = I_{CCOC} + I_{CCOT} \cdot D_H \cdot N_T + I_{CCD} (f_0/2 + f_1 N_I)$$

I_{CCOC} = Quiescent Current with CMOS input levels

I_{CCOT} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_1 = Input Frequency
 N_I = Number of Inputs at f_1
 All currents are in milliamperes and all frequencies are in megahertz.

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AC CHARACTERISTICS

AC CHARACTERISTICS														
Sym.	Parameter	P54/74PCT651/652					P54/74PCT651A/652A					Units	Fig. No.	
		$T_A=+25^{\circ}\text{C}$ $V_{CC}=+5.0\text{V}$		MIL		COM'L	$T_A=+25^{\circ}\text{C}$ $V_{CC}=+5.0\text{V}$		MIL		COM'L			
		Typ.	Min. ¹	Max.	Min. ¹	Max.	Typ.	Min. ¹	Max.	Min. ¹	Max.			
t_{PLH}	Propagation Delay	8.0	2.0	10.0	2.0	9.0						ns	1	
t_{PHL}	Bus to Bus	8.0	2.0	10.0	2.0	9.0						ns	5	
t_{PLH}	Propagation Delay	8.0	2.0	11.0	2.0	9.0						ns	1	
t_{PHL}	Clock to Bus	8.0	2.0	11.0	2.0	9.0						ns	5	
t_{PLH}	Propagation Delay	10.0	2.0	12.0	2.0	11.0						ns	1	
t_{PHL}	SBA or SAB to A or B	10.0	2.0	12.0	2.0	11.0						ns	5	
t_{PZH}	Output Enable Time	9.0	2.0	12.0	2.0	10.0						ns	1,	
t_{PZL}	Enable to Bus	9.0	2.0	12.0	2.0	10.0						ns	7, 8	
t_{PHZ}	Output Disable Time	9.0	2.0	12.0	2.0	10.0						ns	1,	
t_{PLZ}	Disable to Bus	9.0	2.0	12.0	2.0	10.0						ns	7, 8	

Note: AC Characteristics guaranteed with $C_L = 50\text{pF}$ as shown in Figure 1.

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AC OPERATING REQUIREMENTS

AC OPERATING REQUIREMENTS															
Sym.	Parameter	P54/74PCT651/652						P54/74PCT651A/652A						Units	Fig. No.
		$T_A=+25^{\circ}\text{C}$ $V_{CC}=+5.0\text{V}$		MIL		COM'L		$T_A=+25^{\circ}\text{C}$ $V_{CC}=+5.0\text{V}$		MIL		COM'L			
		Typ.	Min.	Max.	Min.	Max.	Typ.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_s(\text{H})$	Setup Time, HIGH	3.0	4.5	—	4.0									ns	1
$t_s(\text{L})$	or LOW Bus to Clock	3.0	4.5		4.0									ns	4
$t_h(\text{H})$	Hold Time, HIGH	1.0	2.0	—	2.0									ns	1
$t_h(\text{L})$	or LOW Bus to Clock	1.0	2.0		2.0									ns	4
$t_w(\text{H})$	Pulse Width, HIGH or LOW	4.0	6.0	—	6.0									ns	1
$t_w(\text{L})$		4.0	6.0		6.0									ns	5

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Notes:

- Minimum limits are guaranteed but not tested on Propagation Delays.
- With one data channel toggling, $t_u(L) = t_u(H) = 2.0\text{ns}$ and $t_f = t_r = 1.0\text{ns}$.

ORDERING INFORMATION

PxxPCT	xxxx	x	x	x	
Temp. Class	Device type	Package	Temperature	Processing	
				B	MIL-STD-883, Class B
				C	0°C to +70°C
				M	-55°C to +125°C
				P	Plastic DIP
				D	CERDIP
				S	Small Outline IC
				L	Leadless Chip Carrier
				651	Inverting Octal Transceiver/Register
				652	Non-Inverting Octal Transceiver/Register
				651A	Inverting Fast Octal Transceiver/Register
				652A	Non-Inverting Fast Octal Transceiver/Register
				74	Commercial
				54	Military

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TECHDOC 1560