T-52-33-01

Solutions

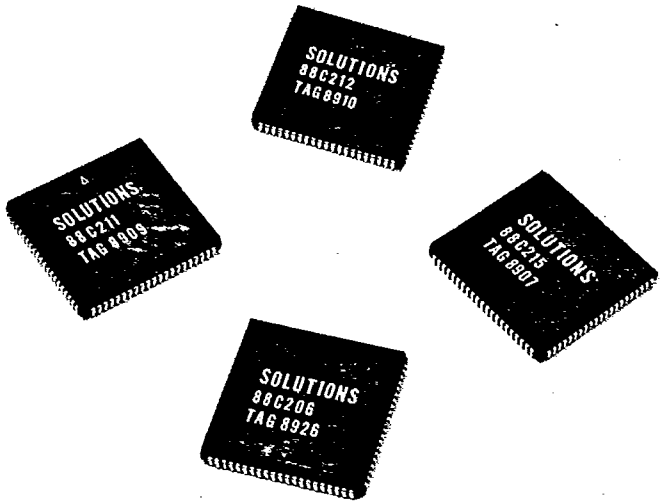
SYSLOGIC TECHNOLOGY CORP.

Chip Set

88C286

SUPER ENHANCED CHIP SET

The 88C286 is an enhanced PC/AT compatible chip set which is a highly integrated VLSI implementation of the control logic used in the IBM AT. Due to its flexible architecture, the 88C286 can be used in any 80286 and 80386SX based systems. The 88C286 chip set consists of four chips which are 88C211 (CPU & Bus Controller), 88C212 (Memory Controller), 88C215 (Data/Address Buffer), and 88C206 (Peripheral Controller).



Main Features and Advantages

- 100% PC/AT compatible enhanced chip set for 12 Mhz, 16 Mhz and 20 Mhz systems.
- Supports Page Interleaved Mode for memory access.
- Supports 16 Mhz 80286 system with 100 ns DRAMs and 20 Mhz systems with 80ns DRAMs.
- Separated CPU and AT Bus clocks.
- Supports LIM EMS 4.0.
- Programmable memory configuration, Command Delays, and Wait States.
- Supports Shadow RAM for Video ROM and BIOS.
- Optimized for OS/2 operation.

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1. 88C211 CPU & BUS CONTROLLER

The 88C211 highly integrates CPU interface and bus control logic. Most of the system functions, except memory access, are taken care of by the 88C211. The main functions of the 88C211 are reset and shutdown, clock generation, clock speed selection, CPU state machine, AT bus state machine, bus arbitration, action codes generation, Port B and NMI generation, DMA, refresh, numeric coprocessor interface, and etc.

2. 88C212 MEMORY CONTROLLER

The 88C212 performs the memory control functions in the 88C286 system. Several distinquished features are integrated in the 88C212 that makes the 88C286 system become one of the most advanced 80286 AT compatible systems in the world. First of all, the 88C212 provides Page Mode to access the memory with interleaved memory banks. By using this so called Page-Interleaved scheme, the 88C212 provides higher performance over the conventional DRAM accessing schemes. As a result, the 88C212 can support a 16 Mhz system with 100 ns DRAM by the use of the Page-Interleaved mode.

The 88C212 also supports up to 8 Mbytes of on board memory. Besides, the 88C212 will automatically re-map the RAM resident in 640 Kbytes to 1 Mbytes area to the top of the 1 Mbyte address space. In order to access the memory resident beyond the 1 Mbyte address space, the 88C212 provides the address translation logic to support the LIM-EMS 4.0. The shadow RAM feature is also integrated into the 88C212 for efficient and fast BIOS execution. In addition, the 88C212 provides OS/2 optimization feature that allows faster switching between the real mode and protected mode. A staggered DRAM refresh scheme is also included to reduce the power supply noise.

2.1 MEMORY ARRAY CONFIGURATION

The memory configuration required by the 80286 PC/AT systems is organized as banks with the width of 18 bits. Sixteen bits out of them are used as data word and split into high and low order bytes. The other 2 bits are used as parity bits and one for each byte. Since the 88C212 also provides the conventional memory accessing scheme, the minimum memory configuration can be a single bank for non-interleaved mode. However, two identical memory banks are required at least for the operation of the Interleaved mode. Table 2.1 shows the commonly used memory configurations.

	DRAM Type				Total Memory	EMS Range
	Bank0	Bank1	Bank2	Bank3		
1	256K	0	0	0	512kb	0
2	1M	0	0	0	2Mb	1Mb to 2Mb
3	256K	256K	0	0	1Mb	1Mb to 1.384Mb
4	1M	1M	0	0	4Mb	1Mb to 4Mb
5	256K	256K	256K	256K	2Mb	1Mb to 2Mb
6	256K	256K	1M	1M	5Mb	1Mb to 5Mb
7	1M	1M	1M	1M	8Mb	1Mb to 8Mb

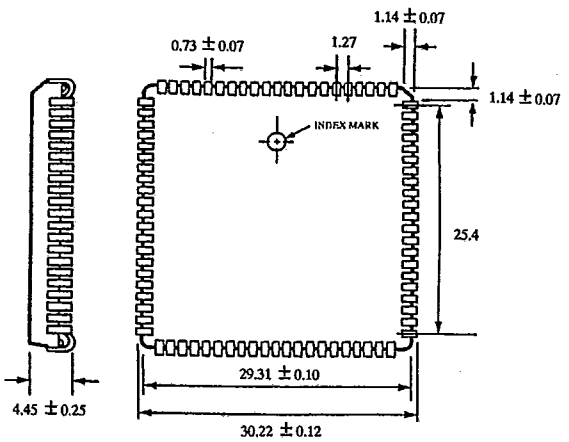
Table 2.1 Commonly Used Memory Configurations

As mentioned above, the possible memory configurations for Page-Interleaved mode are No. 3,4,5,6, and 7 in the Table 2.1.

3. 88C215 DATA/ADDRESS BUFFER

The 88C215 Data / Address buffer, basically, provides the functions of buffering and latching among several buses. The 16 bit to 8 bit bus conversion is also performed by the 88C215 when the conversion is needed. The parity checking will be performed when the 88C215 receives data and the parity bit will be generated when the 88C215 sends data out. The major functions of the 88C215 are address buffering and latching, data buffering and latching, bus conversion, parity checking and parity bit generations.

84-PIN PLCC PACKAGE INFORMATION



Unit (mm)

88CXXX : is the format of Solutions Technology's product names.
88 : Represents Solutions Technology's product series.
C : Represents CMOS technology.
XXX : Represents chip's number.

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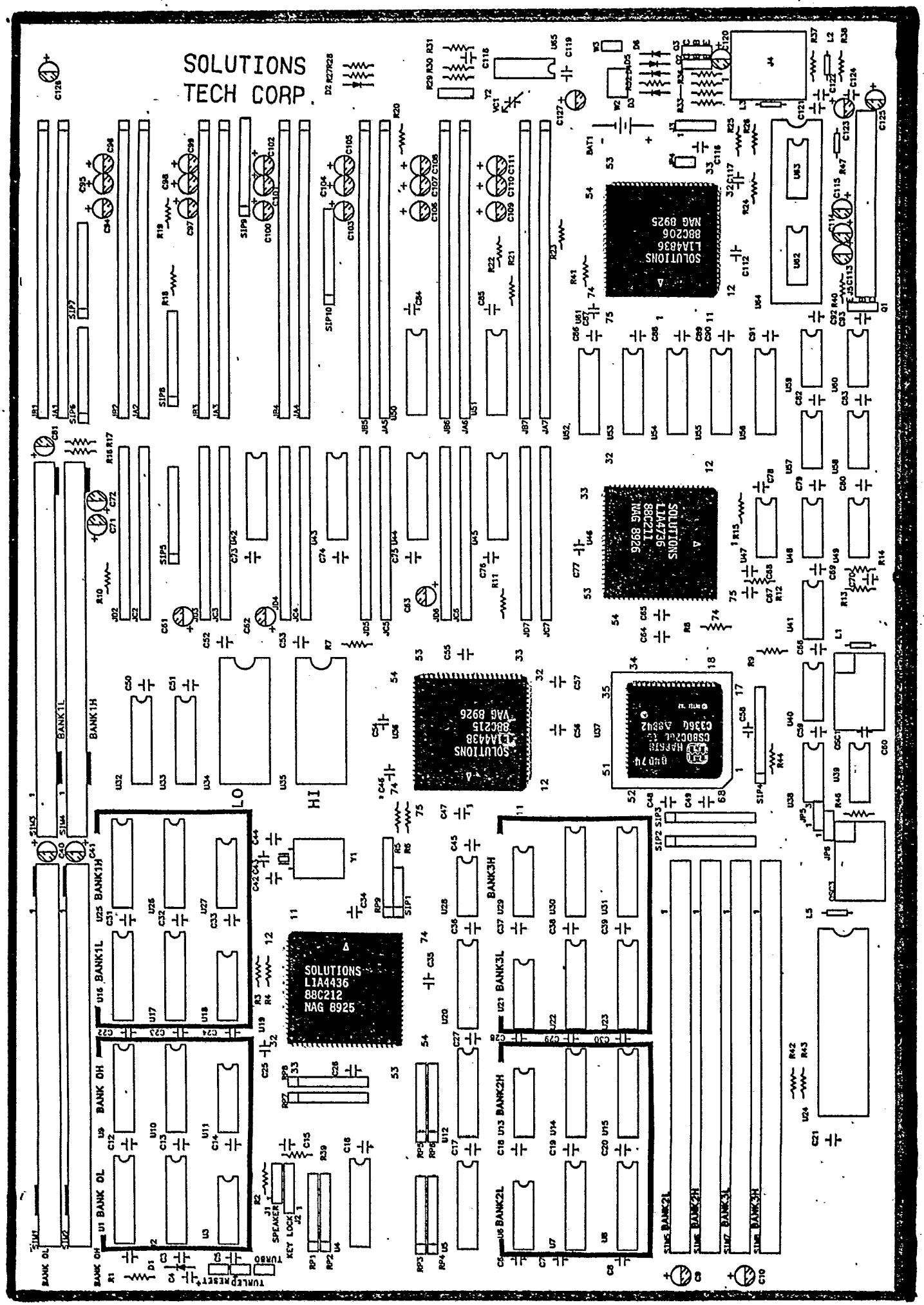
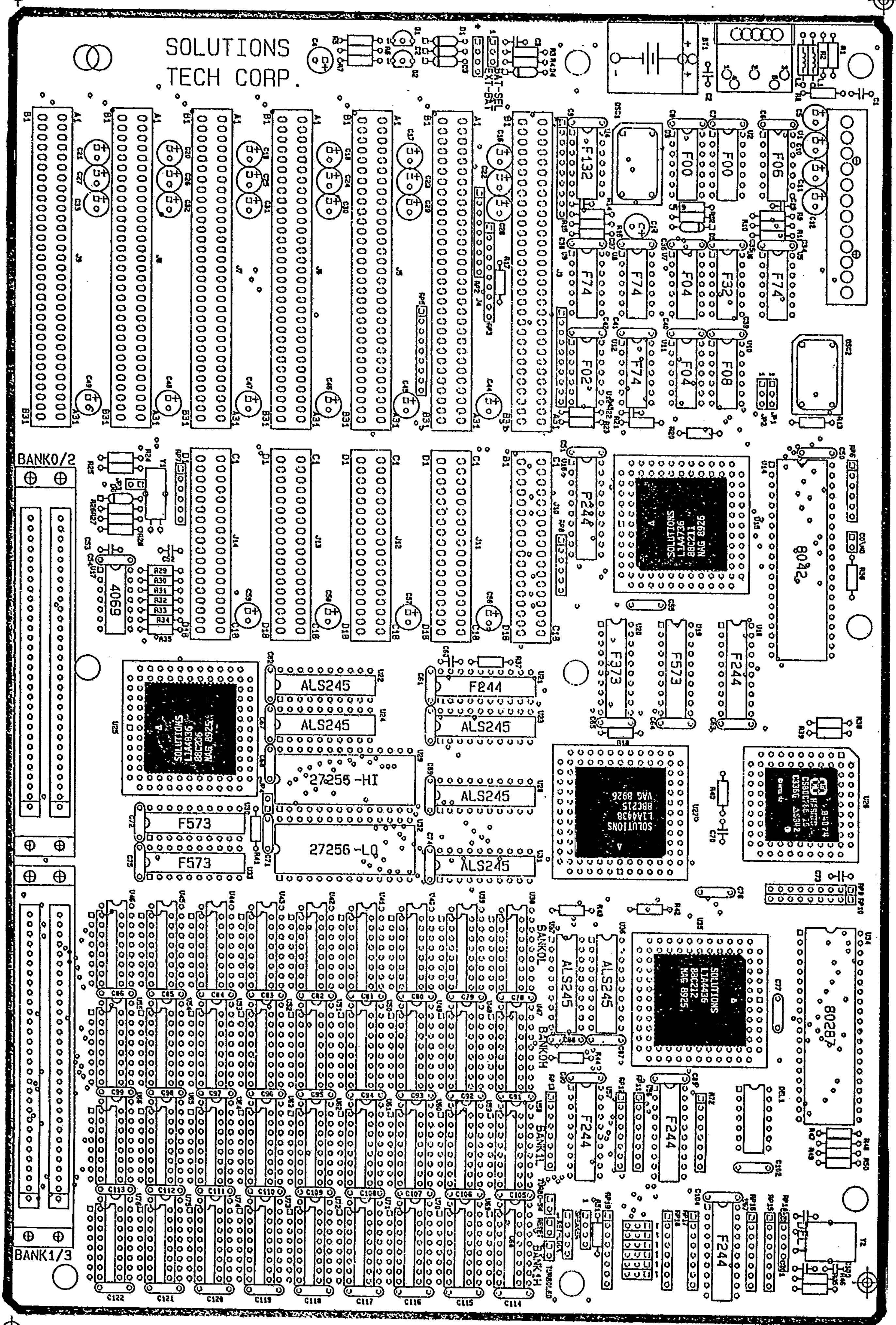
Authorized Distributor


SOLUTIONS
TECH CORP.
SOLUTIONS
L1A4436
88C212
NAG 8925
BANK1L
BANK1H
BANK3H
BANK3L
BANK0H
BANK0L
BANK2H
BANK2L
LO
HI
SPEAKER
KEY LOCK
TURBO
TURBO RESET


SOLUTIONS
TECH CORP.
EXT-BAT
BAT-SEL
F132
F00
F00
F06
F74
F74
F04
F32
F74
F02
F74
F04
F08
BANK0/2
F244
SOLUTIONS L1A4736 88C211 NAG 8925
8042
4069
F373
F573
F244
ALS245
F244
ALS245
ALS245
SOLUTIONS L1A4936 88C206 NAG 8925
27256-HI
ALS245
F573
27256-LO
F573
ALS245
SOLUTIONS L1A4938 88C215 NAG 8926
BANK0L
ALS245
ALS245
SOLUTIONS L1A4436 88C212 NAG 8925
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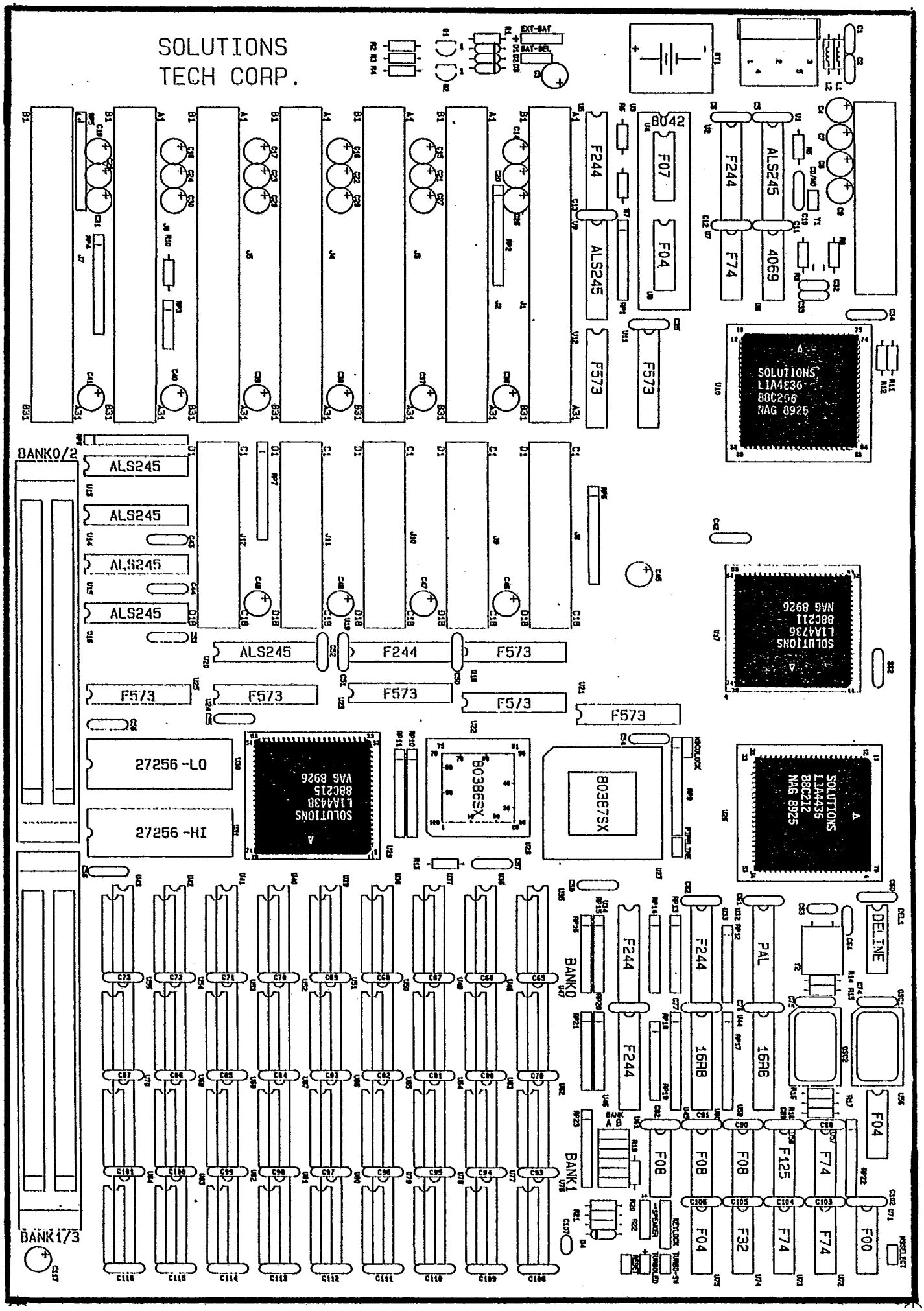
BANK0H
F244
F244
BANK1L
F244
BANK1/3
BANK1H


SOLUTIONS
TECH CORP.
EXT-BAT
BAT-REL
8042
F244
F07
F04
ALS245
F74
4069
F573
SOLUTIONS
L1A4836
88C206
MAG 8925
BANK0/2
ALS245
ALS245
ALS245
ALS245
F244
F573
F573
F573
F573
F573
F573
27256-LO
27256-HI
SOLUTIONS
L1A4438
88C215
MAG 8926
80386SX
80387SX
SOLUTIONS
L1A4736
88C211
MAG 8926
SOLUTIONS
L1A4436
88C212
MAG 8925
BANK1/3
BANK0
BANK1
F244
F244
PAL
DELINE
F244
16R8
16R8
F04
F08
F08
F08
F125
F74
F74
F00
F04
F32
F74
F74
SPEAKER
KEYLOCK
TURBO-LED
TURBO-SW
MODSELECT

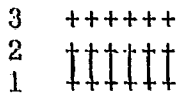
SOLUTIONS 80386SX MOTHER BOARD DRAM INSTALLATION

1) SOLUTIONS 386SX MOTHERBOARD PROVIDES 4 MEMORY BANKS. THE ON BOARD MEMORY CAN BE UP TO 8M BYTES.

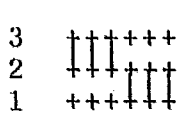
2) BOTH DIP AND SIPP MODULE OF DRAM TYPE 4164/41256/511000 CAN BE USED ON THIS MOTHERBOARD. HOWEVER, IF 1MBIT*9 OR 41256*9 RAM MODULES ARE SELECTED, ONLY SIPP TYPE CAN BE USED.

3) THE DIP AREAS ARE DEFINED AS BANK 0/1 ONLY, AND CAN NOT BE BANK 2/3. HOWEVER, THE SIPP AREAS CAN BE SELECTED TO BE EITHER BANK 0/1 OR 2/3.

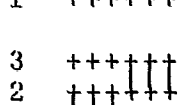
4) THERE IS A 6-BIT JUMPER ON BOARD TO SELECT SIPP AREAS TO BE EITHER MEMORY BANK 0/1 OR 2/3. THESE 6 BITS OF JUMPER ARE SPLIT INTO TWO GROUPS AND ARE USED TO SELECT THE LOCATIONS OF BANK 0 AND 1 RESPECTIVELY. FOR EXAMPLE, IF THE JUMPERS ARE ALL ON THE POSITION 1-2, DIP AREAS ARE DEFINED AS BANK 0 AND 1 AND SIPP AREAS ARE AUTOMATICALLY DEFINED AS BANK 2 AND 3. IF THE JUMPERS ARE ALL ON THE POSITION 2-3, THE SIPP AREAS ARE DEFINED AS BANK 0 AND 1 AND THE DIP AREAS CAN NOT BE USED ANY MORE. THE CONFIGURATIONS ARE ILLUSTRATED AS FOLLOWS :



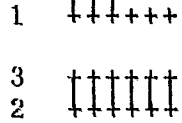
DIP AREAS ARE BANK 0/1, AND
SIPP AREAS ARE BANK 2/3.



BANK 0 IS AT SIPP AREA, AND
BANK 1 IS AT DIP AREA.



BANK 0 IS AT DIP AREA, AND
BANK 1 IS AT SIPP AREA.



BANK 0/1 ARE AT SIPP AREAS, AND
DIP AREAS CAN NOT BE USED ANY MORE.

5) DRAM SPECIFICATION :

100 NS DRAM FOR 16 MHZ ZERO WAIT STATE SYSTEMS.
80 NS DRAM FOR 20 MHZ ZERO WAIT STATE SYSTEMS.

*** SOLUTIONS 386SX MOTHER BOARD ***

JUMPER CONNECTERS FUNCTION DESCRIPTION :

PIPELINE : SHORT = 80386SX RUNS PIPELINE MODE
OPEN = 80386SX RUNS NONPIPELINE MODE

N9CLOCK : SHORT = 80387SX RUNS SYNC. WITH 80386SX CPU SPEED
OPEN = 80387SX RUNS ASYNC. WITH 80386SX CPU SPEED

N9SELECT : SHORT = 80387SX CO_PROCESSOR IS NOT INSTALLED
OPEN = 80387SX CO_PROCESSOR IS INSTALLED

CO/MO : SHORT = COLOR MONITOR IS SELECTED
OPEN = MONOCHROME MONITOR IS SELECTED

RESET : SYSTEM HARDWARE RESET

TURBO-SW : CPU SPEED SELECTION ** SHORT = 8MHZ CPU SPEED
** OPEN = 16MHZ CPU SPEED(TURBO MODE)

TURBOLED : TURBO MODE LED INDICATION ** PIN(+) VCC **

SPEAKER : SPEAKER CONNECTER

KEYLOCK : KEYLOCK & POWER LED CONNECTER

EXT-BAT : EXTERNAL 6VDC BATTERY CONNECTOR ** PIN(+) VCC **

BAT-SEL : INTERNAL OR EXTERNAL BATTERY SELECTOR

BANKAB : RAM BANK SELECTION

** IF 80387SX CO_PROCESSOR IS NOT USED, PLEASE MAKE SURE THAT THE N9SELECT JUMPER IS " SHORT " POSITION.
INCORRECT SETTING WILL CAUSE SYSTEM HANG-UP AFTER DRAM CHECK.