Low-voltage single-chip 8-bit microcontroller 80CL781/83CL781

FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a single package
- 16K x 8 ROM, expandable externally to 64K bytes
- 256 bytes RAM, expandable externally to 64K bytes
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- External memory expandable up to 128K, external ROM up to 64K and/or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector interrupt structure with two priority levels
- Full duplex serial UART
- I^{2}C bus interface for serial transfer on two lines.
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight-byte RAM register banks
  - stack depth limited only by available internal RAM (max. 256 bytes)
  - multiply, divide, subtract and compare instructions
- STOP and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8V to 6.0V
- Frequency range of 32kHz to 12MHz
- Very low current consumption
- Operating temperature range: -40 to +85°C

GENERAL DESCRIPTION

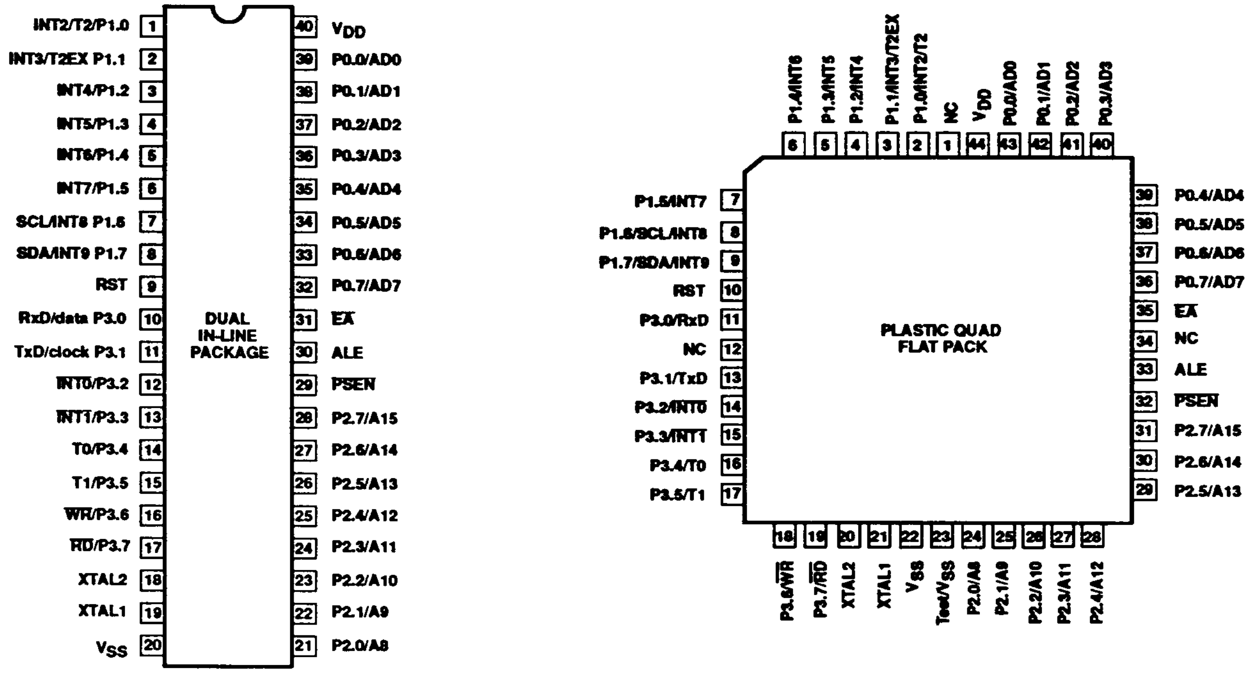
The 83CL781 is manufactured in an advanced CMOS technology. The instruction set of the 83CL781 is based on that of the 8051. The 83CL781 is an 8-bit general purpose microcontroller especially suited for cordless telephone applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the 85CL781 (Piggy-back version) with 256 bytes of RAM is recommended. The 83CL781 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The 83CL781 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA[3] PART ORDER NUMBER				
ROMless	ROM	ROMless	ROM	TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY	DRAWING NUMBER
P80CL781HFP	P83CL781HFP	P80CL781HF N	P83CL781HF N	–40 to +85 40-Pin Plastic DIP[1]	32KHz to 12MHz	SOT129
P80CL781HFH	P83CL781HFH	P80CL781HF B	P83CL781HF B	–40 to +85 44-Pin Plastic QFP[2]	32KHz to 12MHz	SOT205

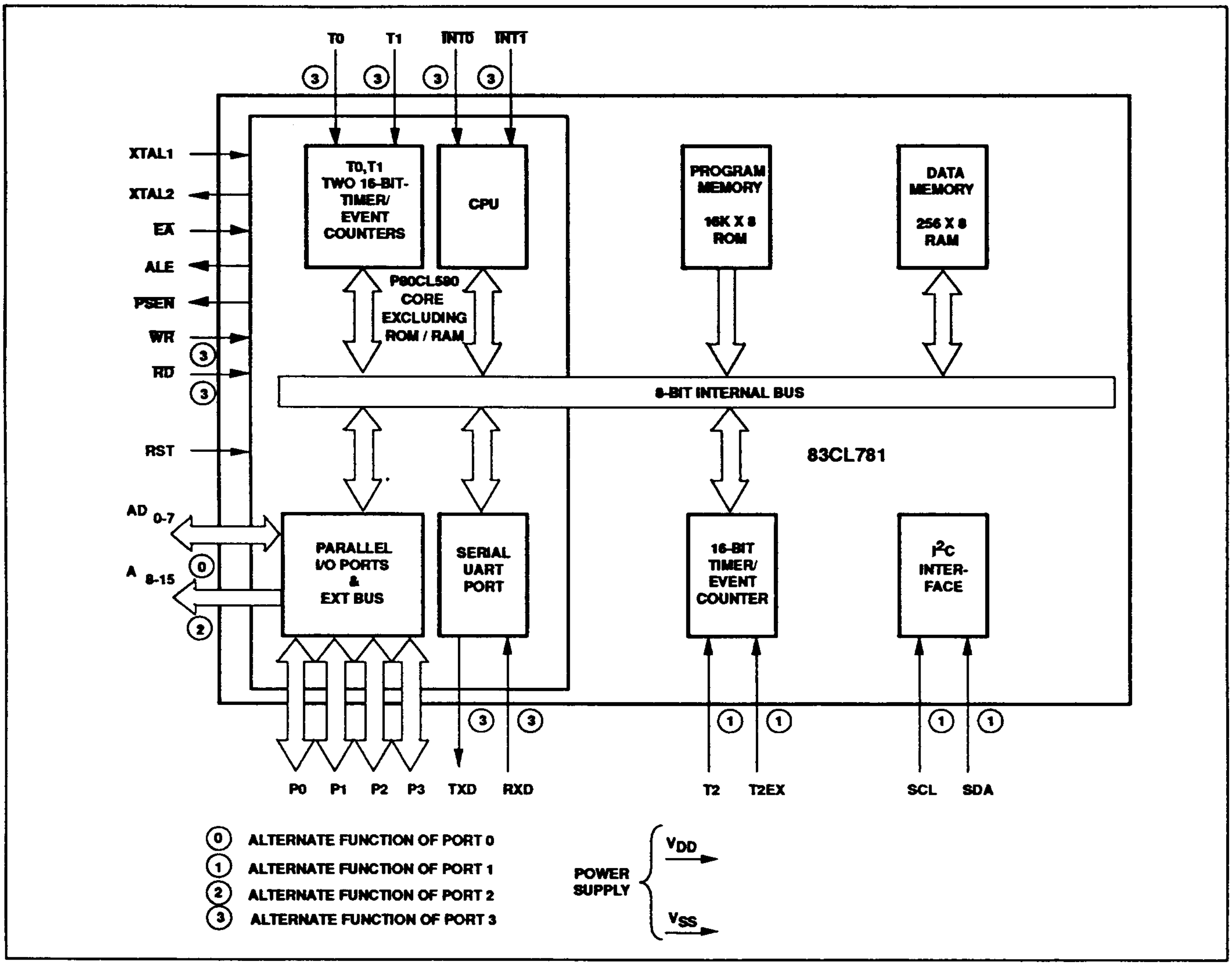
NOTES:
1. DIP = Dual In-line Package
2. QFP = Quad Flat Pack
3. Parts ordered by the Philips North America part number will be marked with the Philips part marking.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	DESIGNATION	FUNCTION
2 3 4 5 6 7 8 9	P1.0/INT2/T2 P1.1/INT3T2EX P1.2/INT4 P1.3/INT5 P1.4/INT6 P1.5/INT7 P1.6/INT8 P1.7/INT9	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled HIGH by the internal pullups, and in that state can be used as inputs. The Port 1 output buffer can sink/source 4 LS TTL loads. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL} in the characteristics) due to the internal pullups. Port 1 also serves the alternative functions INT2 to INT9, and Timer T2 external input.
10	RST	**Reset:** A high level on this pin for two machine cycles while the oscillator is running resets the device.
11,13-19	P3.0 - P3.7	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled HIGH by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL} in the characteristics) due to the internal pull-ups.
11	P3.0/RxD/data	**RXD/data:** serial port receiver data input (asynchronous) or data input/output (synchronous)
13	P3.1/TxD/clock	**TXD/clock:** serial port transmitter data output (asynchronous) or clock output (synchronous)
14	P3.2/$\overline{\text{INT0}}$	**$\overline{\text{INT0}}$:** external interrupt 0.
15	P3.3/$\overline{\text{INT1}}$	**$\overline{\text{INT1}}$:** external interrupt 1.
16	P3.4/T0	**T0:** Timer 0 external input.
17	P3.5/T1	**T1:** Timer 1 external input.
18	P3.6/$\overline{\text{WR}}$	**WR:** external data memory write strobe.
19	P3.7/$\overline{\text{RD}}$	**RD:** external data memory read strobe.
20	XTAL2	**Crystal output**: output of the inverting amplifier of the oscillator. Left open when external clock is used.
21	XTAL1	**Crystal Input**: input to the inverting amplifier of the oscillator, also the input for an externally generated clock source.
22	V_{SS}	**Ground**: circuit ground potential.
23	Test / V_{SS}	**Test Input:** must be connected to V_{SS} or left open.
24 - 26 27 - 31	P2.0 - P2.2 P2.3 - P2.7	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled HIGH by the internal pull-ups, and in that state can be used as inputs. The Port 2 output buffer can sink/source 4 LS TTL loads. Port 2 emits the high-order address byte during accesses to external memory that use 16-bit addresses (MOVX @DPTR). In this application it uses the strong internal pullups when emitting 1s. During accesses to external memory that use 8-bit addresses (MOVX @Ri). Port 2 emits the contents of the P2 Special Function Register.
32	$\overline{\text{PSEN}}$	**Program store enable output**: read strobe to external program memory. When executing code out of external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle. However, during each access to external data memory two $\overline{\text{PSEN}}$ activations are skipped.
33	ALE	**Address Latch Enable**: output pulse for latching the low byte of the address during access to external memory. ALE is emitted at a constant rate of 1/6 of the oscillator frequency, and may be used for external timing or clocking purposes.
35	$\overline{\text{EA}}$	**External Access**: When $\overline{\text{EA}}$ is held High the CPU executes out of internal program memory (unless the program counter exceeds 0FFFH). Holding $\overline{\text{EA}}$ LOW forces the CPU to execute out of external memory regardless of the value of the program counter.
36 - 43	P0.0 - P0.7	**Port 0**: Port 0 is an 8-bit open drain bidirectional I/O port. As an open drain output port it can sink 8 LS TTL loads. Port 0 pins that have 1s written to them float, and in that state will function as high impedance inputs. Port 0 is also the multiplexed low order address and data bus during access to external memory. In this application it uses strong internal pull-ups when emitting logic 1s.
44	V_{DD}	Power supply.


T0
T1
INT0
INT1
3
XTAL1
XTAL2
EA
ALE
PSEN
WR
RD
RST
AD 0-7
A 8-15
0
2
T0,T1 TWO 16-BIT-TIMER/ EVENT COUNTERS
CPU
P80CL580 CORE EXCLUDING ROM / RAM
PROGRAM MEMORY 16K X 8 ROM
DATA MEMORY 256 X 8 RAM
8-BIT INTERNAL BUS
83CL781
PARALLEL I/O PORTS & EXT BUS
SERIAL UART PORT
16-BIT TIMER/ EVENT COUNTER
I²C INTER-FACE
1
P0
P1
P2
P3
TXD
RXD
T2
T2EX
SCL
SDA
0 ALTERNATE FUNCTION OF PORT 0
1 ALTERNATE FUNCTION OF PORT 1
2 ALTERNATE FUNCTION OF PORT 2
3 ALTERNATE FUNCTION OF PORT 3
POWER SUPPLY
VDD
VSS

1 .0 FUNCTIONAL DESCRIPTION

General

The 83CL781 is a stand-alone high-performance CMOS microcontroller designed for use in real-time applications such as instrumentation, industrial control, intelligent computer peripherals and consumer products.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.

The 83CL781 contains a non-volatile 16K byte x 8 read-only program memory; a static 256 byte x 8 read/write data memory; 32 I/O lines; three 16-bit timer/event counters; a fifteen-source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit.

The device has two software selectable modes of reduced activity for power reduction; IDLE and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial I/O and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

In addition, the device provides an I²C-bus serial I/O port with byte oriented master and slave functions, which allows communication with the whole family of I²C-bus compatible ICs and a standard UART serial interface.

CPU timing

A machine cycle consists of a sequence of 6 states. Each state time lasts for two oscillator periods, thus a machine cycle takes 12 oscillator periods or 1 µs if the oscillator frequency is 12 MHz.

1 .1 Memory organization

The 83CL781 has a 16K Program Memory (ROM) plus 256 bytes of Data Memory (RAM) on board. The device has separate address spaces for Program and Data Memory (see Figure 1). Using Ports P0 and P2, the 83CL781 can address up to 64K bytes of external memory. The CPU generates both read and write signals (RD and WR) for external Data Memory accesses, and the read strobe (PSEN) for external Program Memory.

1.1.1 Program Memory

The 83CL781 contains 16K bytes of internal ROM. After reset the CPU begins execution at location 0000H. The lower 16K bytes of Program Memory can be implemented in either on-chip ROM or external Memory. If the EA pin is strapped to V_{DD}, then program memory fetches from addresses 000H through 3FFFH are directed to the internal ROM. Fetches from addresses 4000H through FFFFH are directed to external ROM. Program counter values greater than 3FFFH are automatically addressed to external memory regardless of the state of the EA pin.

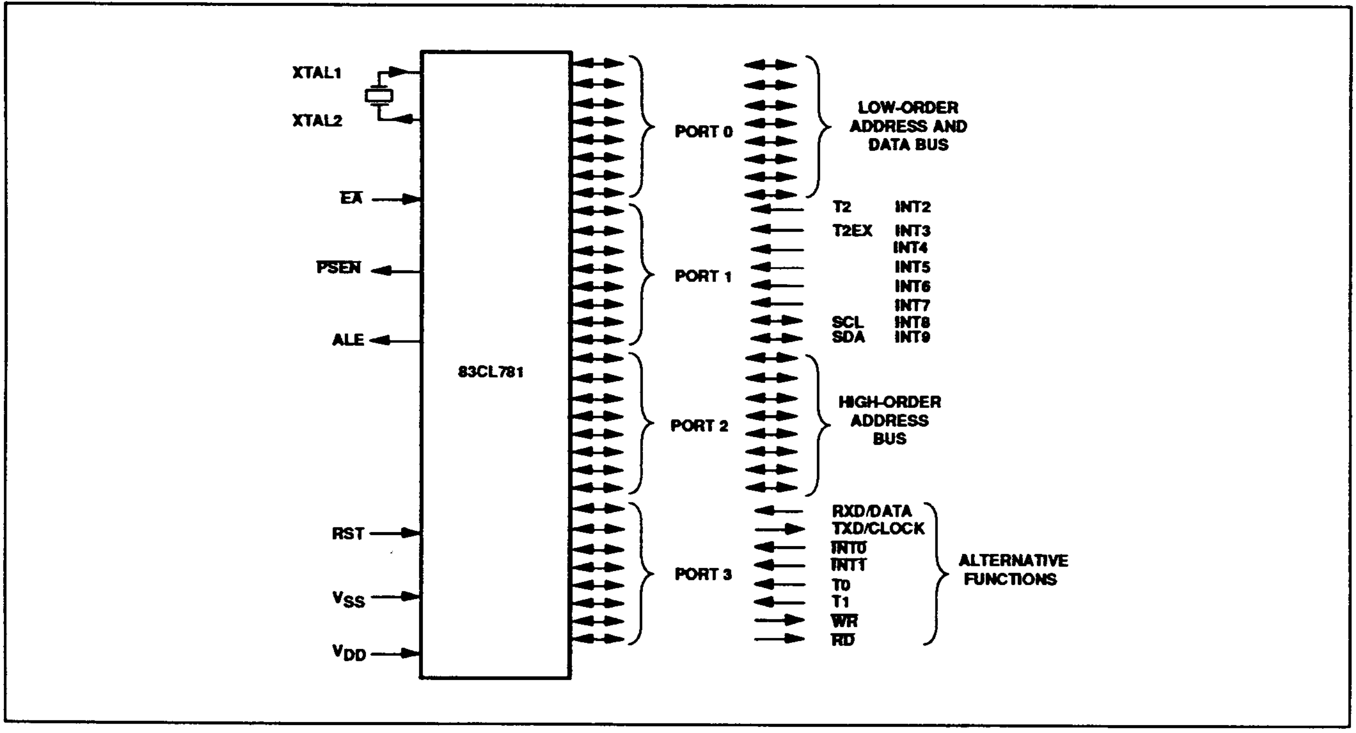
1.1.2 Data Memory

The 83CL781 contains 256 bytes of internal RAM and 38 Special Function Registers (SFR). Figure 1 shows the internal Data Memory space divided into the Lower 128, the Upper 128, and the SFR space. Internal RAM locations 0-127 are directly and indirectly addressable. Internal RAM locations 128-255 are only indirectly addressable. The special function register locations 128-255 are only directly addressable.

1.1.3 Special Function Registers

The upper 128 bytes are the address locations of the SFRs. Figure 3 shows the Special Function Register (SFR) space. SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 bit addressable locations in the SFR address space (SFRs with addresses divisible by eight).

FUNCTIONAL DIAGRAM



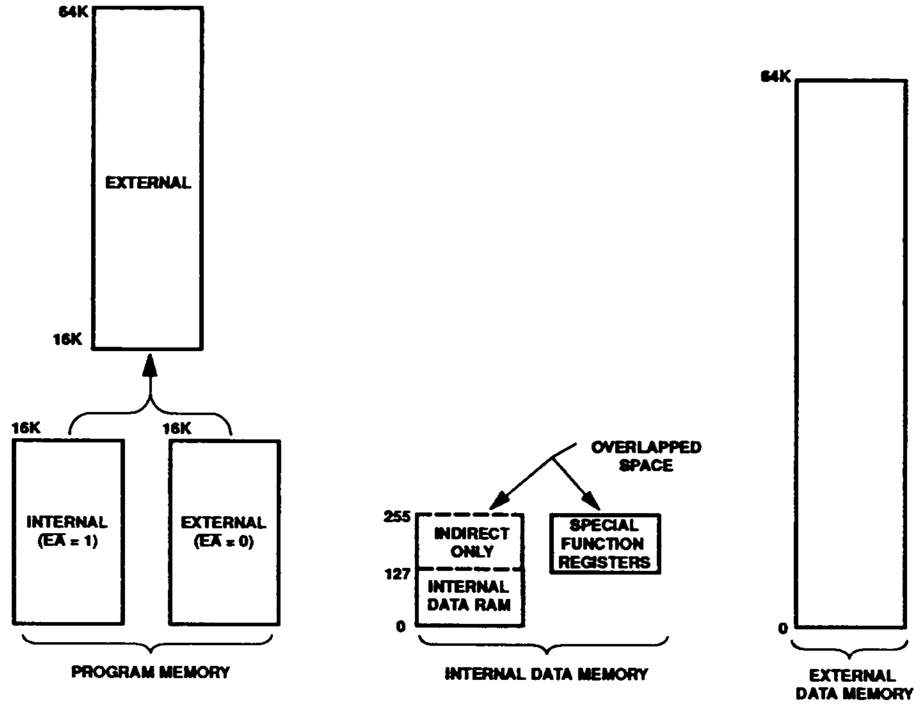


Figure 1. Memory Map

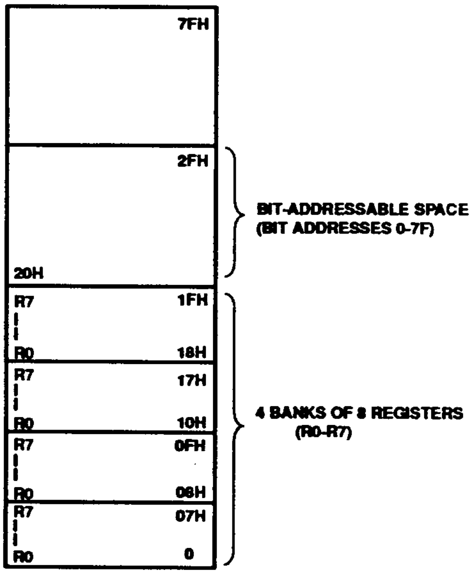


Figure 2. The Lower 128 Bytes of Internal RAM

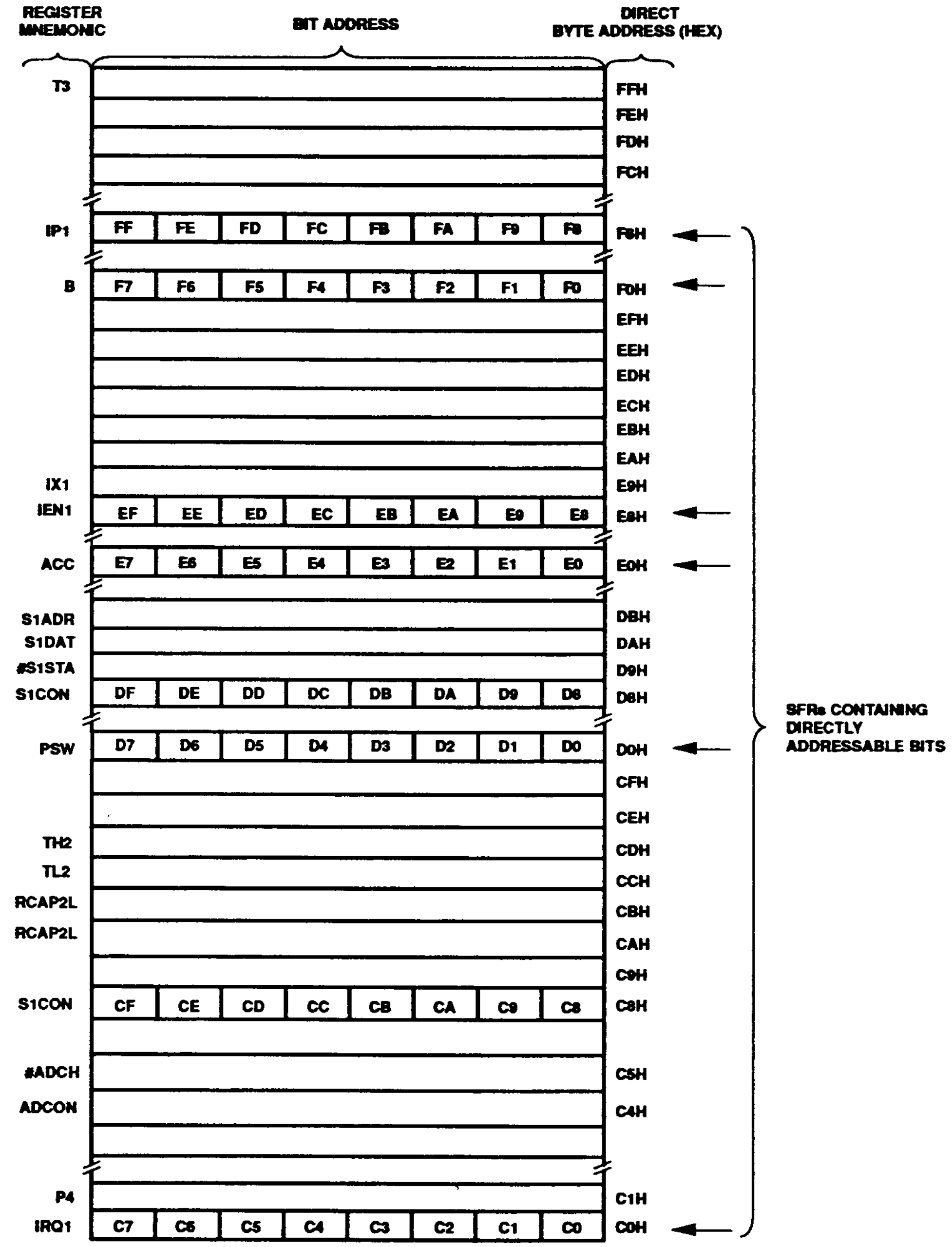
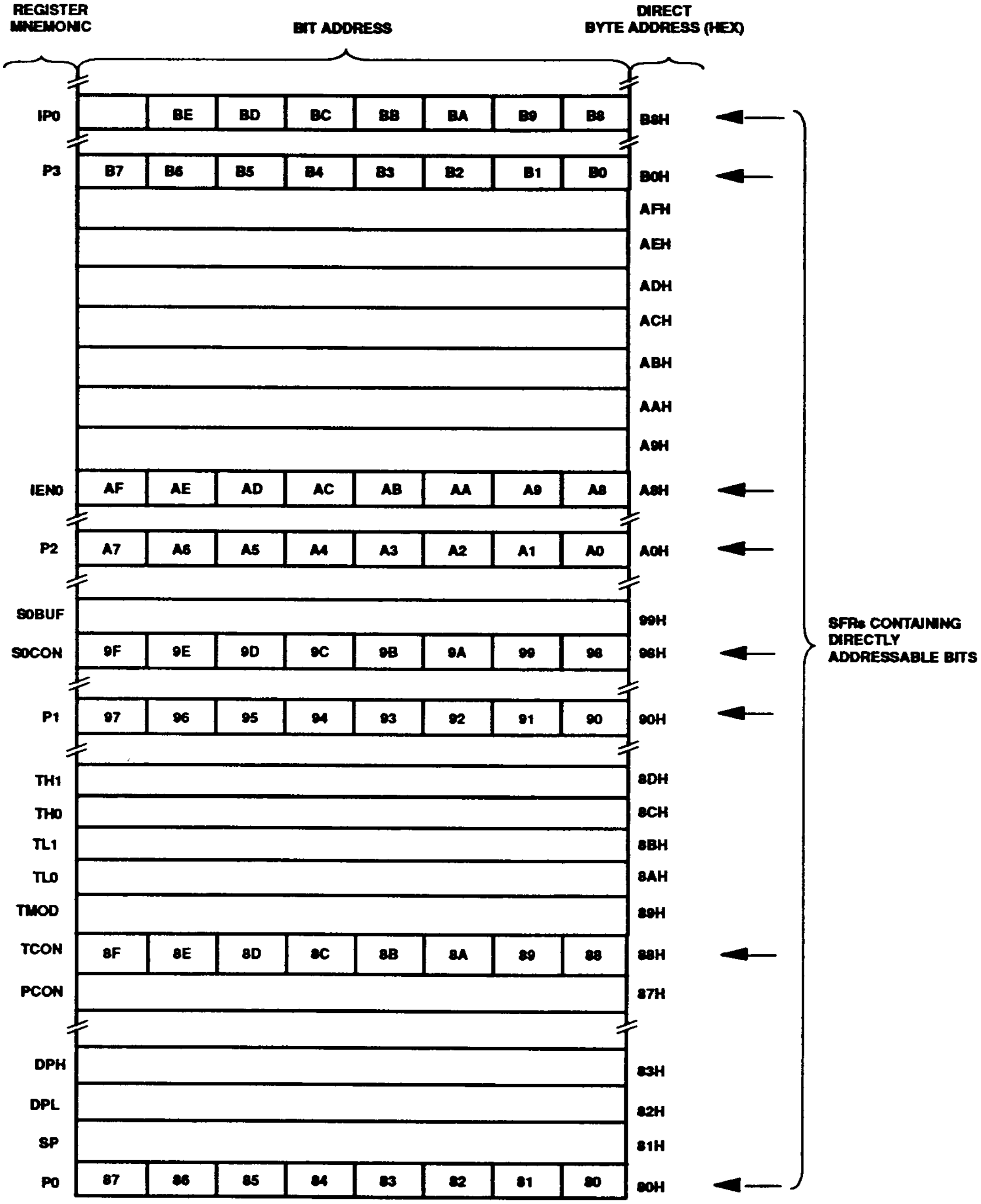

REGISTER MNEMONIC
BIT ADDRESS
DIRECT BYTE ADDRESS (HEX)
T3 FFH
FEH
FDH
FCH
IP1 FF FE FD FC FB FA F9 F8 F8H
B F7 F6 F5 F4 F3 F2 F1 F0 F0H
EFH
EEH
EDH
ECH
EBH
EAH
IX1 E9H
IEN1 EF EE ED EC EB EA E9 E8 E8H
ACC E7 E6 E5 E4 E3 E2 E1 E0 E0H
S1ADR DBH
S1DAT DAH
#S1STA D9H
S1CON DF DE DD DC DB DA D9 D8 D8H
PSW D7 D6 D5 D4 D3 D2 D1 D0 D0H
CFH
CEH
TH2 CDH
TL2 CCH
RCAP2L CBH
RCAP2L CAH
C9H
S1CON CF CE CD CC CB CA C9 C8 C8H
#ADCH C5H
ADCON C4H
P4 C1H
IRQ1 C7 C6 C5 C4 C3 C2 C1 C0 C0H
SFRs CONTAINING DIRECTLY ADDRESSABLE BITS

Figure 3. (a) Special Function Register Memory Map



REGISTER MNEMONIC	BIT ADDRESS								DIRECT BYTE ADDRESS (HEX)
IP0		BE	BD	BC	BB	BA	B9	B8	B8H
P3	B7	B6	B5	B4	B3	B2	B1	B0	B0H
									AFH
									AEH
									ADH
									ACH
									ABH
									AAH
									A9H
IEN0	AF	AE	AD	AC	AB	AA	A9	A8	A8H
P2	A7	A6	A5	A4	A3	A2	A1	A0	A0H
S0BUF									99H
S0CON	9F	9E	9D	9C	9B	9A	99	98	98H
P1	97	96	95	94	93	92	91	90	90H
TH1									8DH
TH0									8CH
TL1									8BH
TL0									8AH
TMOD									89H
TCON	8F	8E	8D	8C	8B	8A	89	88	88H
PCON									87H
DPH									83H
DPL									82H
SP									81H
P0	87	86	85	84	83	82	81	80	80H

Figure 3. (b) Special Function Register Memory Map

1.1.4 Addressing

The 83CL781 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register-plus Index-Register-indirect

The first three methods can be used for addressing destination operands. Most instructions have a "destination/source" field that specifies data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four register banks through register, direct or indirect.
- Internal RAM (256 bytes) through direct or register-indirect.
- Special Function Register through Direct.
- External data memory through Register-Indirect
- Program memory look-up tables through Base-Register-plus index-Register-indirect.

1.2 I/O facilities

1.2.1 Ports

The 83CL781 has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8-bit addressable ports. Port 0, 1, 2 and 3 perform the following alternate functions:

- Port 0: provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.
- Port 1: (1) provides the inputs for the external interrupts INT2 / INT9; (2) External counter/capture of Timer 2; (3) I^2C bus
- Port 2: provides the high-order address when expanding the device with external program or data memory.
- Port 3: pins can be configured individually to provide: (1) external interrupt request inputs; (2) counter input; (3) control signals to read and write to external memories; and (4) UART input and output.

To enable a Port 3 pin alternate function, the Port 3 bit latch in its SFR must contain a logic 1.

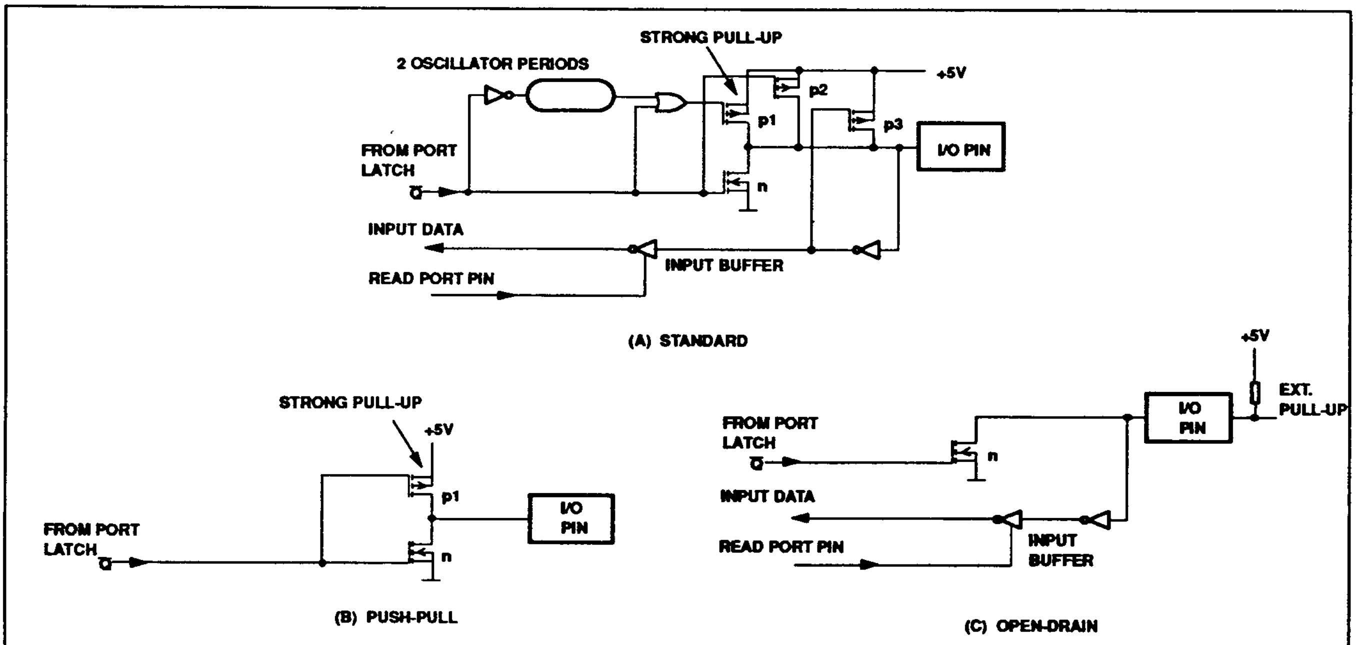
Each port consists of a latch (Special Function Registers P0 to P3), an output driver and an input buffer. Ports 1,2,3 have internal pull-ups. Figure 4(a) shows that the strong transistor p1 is turned on for only 2 oscillator periods after a 0-to-1 transition in the port latch. When on, it turns on p3 (a weak pull-up) through the inverter. This inverter and p3 form a latch which hold the 1. In Port 0 the pull-up p1 is only on when emitting 1s for external memory access. Writing a 1 to a Port 0 bit latch leaves both output transistors switched off so the pin can be used as a high-impedance input.

1.2.2 Port Options

Thirty of the 32 parallel port pins (excluding P1.6 and P1.7 with option '2S' only) may be individually configured with one of the following options (see Figure 4):

Option 1: **Standard Port**; quasi-bidirectional I/O with pull-up. The strong booster pull-up p1 is turned on for two oscillator periods after a 0-to-1 transition in the port latch (see Figure 4(a)).

Option 2: **Open drain**; quasi-bidirectional I/O with n-channel open drain output. Use as an output requires the connection of an external pull-up resistor (see Figure 4(c)).



(A) STANDARD

(B) PUSH-PULL

(C) OPEN-DRAIN

Figure 4. Port Options

Option 3: **Push-Pull**; output with drive capability in both polarities. Under this option, pins can only be used as outputs (see Figure 4(b)).

External Memory Accesses

Option 1: True 0 and 1 are written as address to the external memory (strong pull-up is used).

Option 2: An external pull-up resistor is needed for external accesses.

Option 3: Not allowed for external memory accesses as the port can only be used as output.

I/O Accesses:

Option 1: When writing a 1 to the port-latch, the strong pull-up p1 will be on for two oscillator periods. No weak pull-up exists. Without an external pull-up, this option can be used as a high-impedance input.

Option 2: Open drain; quasi-bidirectional I/O with n-channel open drain output. Use as an output requires the connection of an external pull-up resistor (see Figure 4(c)).

Option 3: Push-Pull; output with drive capability in both polarities. Under this option, pins can only be used as outputs.

Individual mask selection of the post-reset state is available on any of the above pins. Make your selection by appending "S" or "R" to option 1, 2, or 3 above.

Option S: SET; after reset this pin will be initialized HIGH.

Option R: RESET; after reset this pin will be initialized LOW.

1 .3 Timer/event counter

The 83CL781 contains three 16-bit Timer/Counter registers; Timer 0, Timer 1, and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupts requests

Timer 0 and Timer 1 can be independently programmed to operate as follows:

- Mode 0: 8-bit timer or counter with divide-by-32 prescaler
- Mode 1: 16-bit time-interval or event counter
- Mode 2: 8-bit time interval or event counter with automatic reload upon overflow
- Mode 3: Timer 0 establishes TL0 and TH0 as two separate counters.

In the "Timer" function, the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the "Counter" function, the register is incremented in response to a 1-to-0 transition. Since it takes two machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure a given level is sampled, it should be held for at least one full machine cycle.

1.3.1 Timer 2

Timer 2 is a 16-bit Timer/Counter. Like Timers 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/T2 in the Special Function Register T2CON (Figure 5). It has three operating modes: "capture", "auto-load" and "baud rate generator", which are selected by bits in T2CON as shown in Table 1.

Table 1. Timer 2 Operating Modes

RTCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-Bit Auto-reload
0	1	1	16-Bit Capture
1	x	1	Baud Rate Generator
x	x	0	(Off)

(MSB)							(LSB)
TF2	EXF2	GF2	TRCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Symbol	Position	Name and Significance
TF2	T2CON	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	T2CON	Timer 2 external flag set when either a capture or reload is caused by a negative transition of T2EX and EXEN = 1. When Timer 2 Interrupt is enabled, EXF2 + will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
RTCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive and transmit clock in modes 1 and 3. TLCK = 0 causes Timer 1 overflows to be used for the receive and transit clock.
EXEN2	T2CON.3	Timer external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2C ON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T2}$	T2CON.1	Timer or counter select. Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered)
CP/$\overline{RL2}$	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN = 1. When cleaned, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.
GF2		General purpose flag bit

Figure 5. T2CON: Timer/Counter 2 Control Register

In the Capture Mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2=1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. The Capture Mode is illustrated in Figure 6.

In the auto-reload mode there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2=0, then when Timer 2 rolls over it not only set TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2=1, the Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2.

The auto-reload mode is illustrated in Figure 7.

The baud rate generator mode is selected by RTCLK=1. It will be described in conjunction with the serial port.

A conversion already in progress is aborted when the Power-down mode is entered. The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the Idle mode.

1 .4 Idle and Power-down Operation

Idle mode operation permits the interrupt, serial ports, timer blocks to continue functioning while the clock to the CPU is halted.

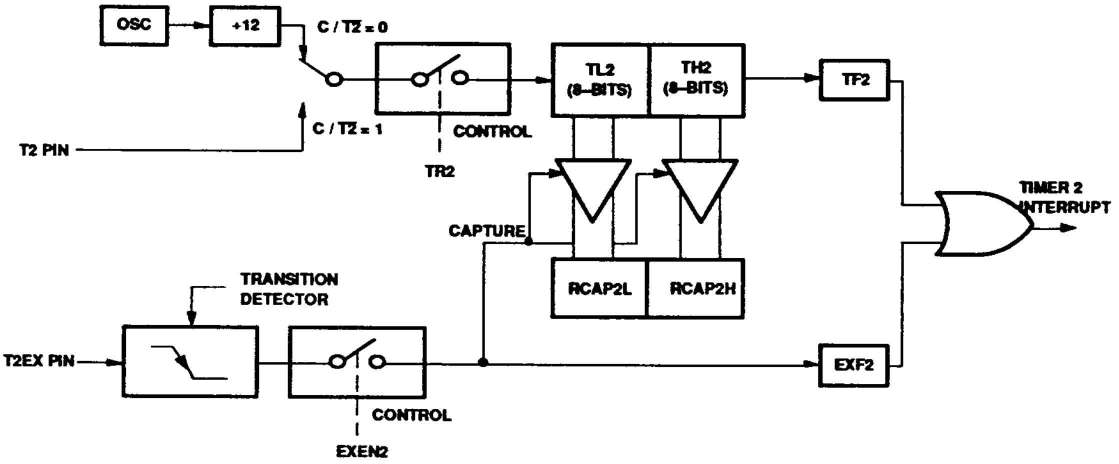


Figure 6. Timer 2 in Capture Mode

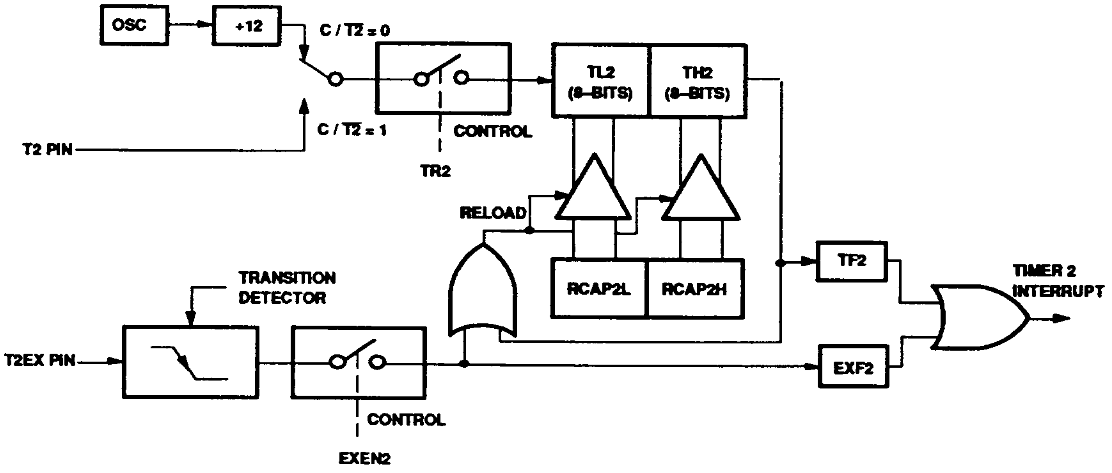


Figure 7. Timer 2 in Auto-Reload Mode

The following functions remain active during Idle mode. These functions may generate an interrupt or reset and thus end the Idle mode.

- Timer 0, Timer 1, Timer 2
- SIO, I^{2}C
- External interrupt

The Power-down operation freezes the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register.

1.4.1 Power control register (PCON)

These special modes are activated by software via the Special Function Register PCON. Its hardware address is 87H. [PCON is not bit-addressable.]

7	6	5	4	3	2	1	0
SMOD	-	-	-	GF1	GF0	PD	IDL
MSB							LSB

BIT	SYMBOL	FUNCTION
PCON.7	SMOD	Double Baud rate bit. When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in 1, 2, or 3.
PCON.6	-	(reserved)
PCON.5	-	(reserved)
PCON.4	-	(reserved)
PCON.3	GF1	General-purpose flag bit
PCON.2	GF0	General-purpose flag bit
PCON.1	PD	Power-down bit. Setting this bit activates Power-down mode.
PCON.0	IDL	Idle mode bit. Setting this bit activates the Idle mode.

If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XX00000).

1.4.2 Power-down mode

The instruction setting PCON.1 is the last executed prior to going into the Power-down mode. In Power-down mode the oscillator is stopped. The contents of the on-chip RAM and SFRs are preserved. The port pins output the values held by their respective SFRs. ALE and PSEN are held LOW.

1.4.3 Wake-up mode

Setting the PD flag in the PCON register forces the controller into the Power-down mode. Setting this flag enables the controller to be awakened from the Power-down mode with either the external interrupts INT2/INT8, or a reset operation.

The wake-up operation after power-down in this controller has two basic approaches:

1.4.3.1 Wake-up using INT2/INT9

If INT2 to INT9 are enabled, the 83CL781 can be awakened from power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods. This is controlled by an on-chip delay counter.

1.4.3.2 Wake-up using RESET

To wake-up the 83CL781 the RESET pin has to be kept HIGH for a minimum of 24 periods. The on-chip delay counter is inactive. The user has to ensure that the oscillator is stable before any operation is attempted. Figure 8 illustrates the two possibilities for wake-up.

1.4.4 Idle mode

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 1.

There are two methods used to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following the return-from-interrupt instruction RETI, the next instruction to be executed will be the one which follows the instruction that wrote a logic 1 to PCON.0.

Flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.

The second method of terminating the Idle mode is with an external hardware reset, or an internal reset caused by an overflow of Timer T3. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation.

Reset redefines all SFRs, but does not affect the on-chip RAM.

In the Power-down mode, V_{DD} may be reduced to minimize power consumption. However, the supply voltage must not be reduced until Power-down mode is active, and must be held active until the oscillator has restarted and stabilized.

The status of the external pins during Idle and Power-down mode is shown in Table 2. If the Power-down mode is activated whilst accessing external memory, port data held in the Special Function Register P2 is restored to Port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor p1 (see Figure 4(a)).

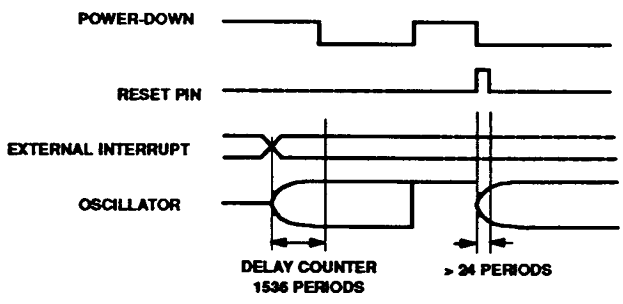


Figure 8. Wake-up Operation

1 .5 I²C Bus Serial I/O

The serial port supports the twin line I²C-bus. The I²C bus consists of a data line (SDA) and a clock line (SCL). These lines also function as I/O port lines P1.7 and P1.6 respectively. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware. The I²C bus serial I/O has complete autonomy in byte handling and operates in four modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver

These functions are controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register and S1ADR the slave address register. Slave address recognition is performed by hardware.

Table 2. Status of the External Pins during Idle and Power-down Modes

MODE	MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle (1)	Internal	1	1	Port data	Port data	Port data	Port data
Idle (1)	External	1	1	Floating	Port data	Address	Port data
Power-down	Internal	0	0	Port data	Port data	Port data	Port data
Power-down	External	0	0	Floating	Port data	Port data	Port data

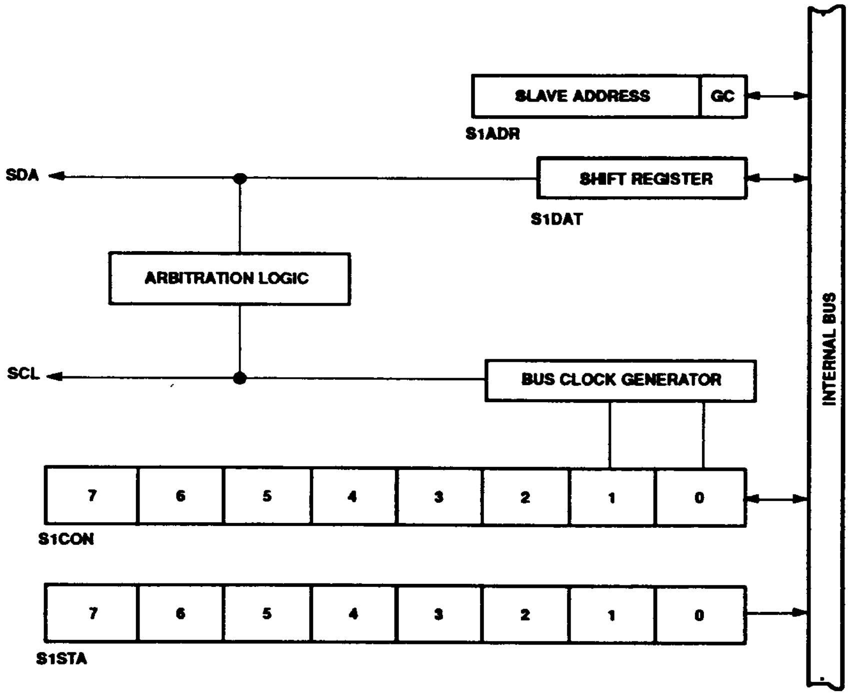


Figure 9. Serial I/O

Serial Control Register S1CON (D8H)

CR2	ENS1	STA	STO	SI	AA	CR1	CR0

CR0, CR1, CR2 These three bits determine the serial clock frequency when SIO is in a master mode. See table 3.

AA Assert Acknowledge bit. When the AA flag is set, an acknowledge (low level SDA) will be returned during the acknowledge clock pulse on the SCL line when:

- own slave address is received
- general call address is received (S1ADR.0=1)
- data byte received while device is programmed as master
- data byte received while device is a selected slave

With AA=0, no acknowledge will be returned. Consequently, no interrupt is requested when the "own slave address" or general call address is received.

SI SIO interrupt flag. When the S1 flag is set, an acknowledge is returned after any one of the following conditions:

- a start condition is generated in master mode
- own slave address received during AA=1
- general call address received while S1ADR.0 and AA=1
- data byte received or transmitted as selected slave
- stop or start condition received as selected slave receiver or transmitter

STO STOP flag. With this bit set while in master mode a STOP condition is generated. When a STOP condition is detected on the bus, the SIO hardware clears the STO flag. In the slave mode, the STO flag may also be set to recover from an error condition. In this case, no STOP condition is transmitted to the I²C bus. However, the SIO hardware behaves as if a STOP condition has been received and releases SDA and SCL. The SIO then switches to the "not addressed" receiver mode. The STO flag is automatically cleared by hardware.

STA START flag. When the STA bit is set in slave mode, the SIO hardware checks the status of the I²C bus and generates a START condition if the bus is free. If STA is set while the SIO is in master mode, SIO transmits a repeated START condition.

ENS1 When ENS1=0, the SIO is disabled. The SDA and SCL outputs are in a high-impedance state; P1.6 and P1.7 function as open drain ports. When ENS=1, the SIO is enabled. The P1.6 and P1.7 port latches must be set to logic 1.

Table 3. SCL Frequency

				Bit Rate (kHz) at fosc		
CR2	**CR1**	**CR2**	**fosc Divided By**	**3.58MHz**	**6 MHz**	**12MHz**
0	0	0	256	14.0	23.4	46.9
0	0	1	224	16.0	26.8	53.6
0	1	0	192	18.6	31.3	62.5
0	1	1	160	22.4	37.5	75.0
1	0	0	960	3.73	6.25	12.5
1	0	1	120	29.8	50	100
1	1	0	60	59.7	100	–
1	1	1	not allowed	–	–	–

Status Register S1STA (D9H)

SC4	SC3	SC2	SC1	SC0	0	0	0

S1STA is an 8-bit read-only special function register. S1STA.3-S1STA.7 hold a status code. S1STA.0-S1STA.2 are held LOW. the contents of S1STA may be used as a vector to a service routine. This optimizes response time of the software and consequently that of the I²C bus.

The following is a list of the status code:

Abbreviations used:

SLA:	7-bit slave address
R:	Read bit
W:	Write bit
ACKNOT:	Acknowlegement (acknowledge bit = 0)
ACK:	Not Acknowledge (acknowledge bit = 1)
DATA:	8-bit byte to or from the I²C bus
MST:	Master
SLV:	Slave
TRX:	Transmitter
REC:	Receiver

MST/TRX Mode
S1STA Value

08H	A START condition has been transmitted
10H	A repeated START condition has been transmitted
18H	SLA and W have been transmitted, ACKNOT received
28H	DATA of S1DAT has been transmitted, ACK received
30H	DATA of S1DAT has been transmitted, ACKNOT received
38H	Arbitration lost in SLA, R/W or DATA

MST/REC Mode
S1STA Value

38H	Arbitration lost while returning ACKNOT
40H	SLA and R have been transmitted, ACK received
48H	SLA and R have been transmitted, ACKNOT received
50H	DATA has been received, ACK returned
58H	DATA has been received, ACKNOT returned

SLV/REC Mode
S1STA Value

60H	Own SLA and W have been received, ACK returned
68H	Arbitration lost in SLA, RW as MST. Own SLA and W have been received, ACK returned.
70H	General Call has been received, ACK returned
78H	Arbitration lost in SLA, RW as MST. General Call has been received.
80H	Previously addressed with own SLA. DATA byte received, ACKNOT returned.
88H	Previously addressed wtih General Call. DATA byte has been received, ACK has been returned.
90H	Previously addressed with General Call. DATA byte has been received, ACK has been returned.
98H	Previously addressed with General Call. DATA byte has been received, ACKNOT has been returned.
A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

SLV/TRX Mode
S1STA Value

A8H	Own SLA and R have been received, ACK returned
B0H	Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned.
B8H	DATA byte has been transmitted, ACK received.
C0H	DATA byte has been transmitted, ACKNOT received.

Miscellaneous
S1STA Value

00H	Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition.

Data Shift Register S1DAT (DAH)

7	6	5	4	3	2	1	0

This register contains the serial data to be transmitted or data that has just been received. Bit 7 is transmitted or received first; i.e., data is shifted from left to right.

Own Address Register S1ADR (DBH)

7	6	5	4	3	2	1	0

This 8-bit register may be loaded with the 7-bit address to which the controller will respond when programmed as a slave receiver/transmitter. The LSB bit (GC) is used to determine whether the general CALL address is recognized.

S1ADR.0, GC: 0 = general CALL address is not recognized.
1 = general CALL is recognized.

S1ADR.7 - 1: own slave address

1 .6 Standard serial interface SIO0: UART

This serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed at Special Function Register S0BUF. Writing to S0BUF loads the transmit register, and reading S0BUF loads the transmit register, and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0: Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud is fixed at 1/12 the oscillator frequency.

Mode 1: 10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2: 11 bits are transmitted (through TxD) or received (through RxD): start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

1 .6.1 Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

1 .6.2 Serial port control register

The serial port control and status register is the Special Function Register S0CON, shown in Figure 13. The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

MSB							LSB
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Where SM0, SM1 specify the serial port mode, as follows:

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	0	Shift register	fosc / 12
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	fosc / 64 or fosc / 32
1	1	3	9-bit variable UART	

SM2 enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1 then R1 will not be activated if the received ninth data bit (RB8) is 0. In Mode 1, if SM2=1 then R1 will not be activated if a valid stopbit was not received. In Mode 0, SM2 should be 0.

REN enables serial reception. Set by software to enable reception. Clear by software to disable reception.

TB8 is the ninth data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.

RB8 in Modes 2 and 3, is the ninth data bit that was received. In Mode 1, if SM2=0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.

TI is transmit interrupt flag. Set by hardware at the end of the eighth bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.

RI is receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial receoption (except see SM2). Must be cleared by software.

Figure 10. Serial Port Control (SCON) Register

Table 4. Timer 1 Generated Commonly Used Baud Rates

BAUD RATE	f_{osc}	SMOD	C/T	TIMER 1 MODE	RELOAD VALUE
Mode 0 Max: 1MHz	12MHz	X	X	X	X
Mode 2 Max: 375K	12MHz	1	X	X	X
Mode 1, 3: 62.5K	12MHz	1	0	2	FFH
19.2K	11.059MHz	1	0	2	FDH
9.6K	11.059MHz	0	0	2	FDH
4.8K	11.059MHz	0	0	2	FAH
2.4K	11.059MHz	0	0	2	F4H
1.2K	11.059MHz	0	0	2	E8H
137.5K	11.986MHz	0	0	2	1DH
110K	6MHz	0	0	2	72H
110K	12MHz	0	0	1	FEEBH

Baud rRates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = Oscillator Frequency / 12. The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is the value on reset), the baud rate is 1/64 the oscillator frequency. If SMOD = 1, the baud rate is 1/32 the oscillator frequency.

Mode 2 Baud Rate = (2^{SMOD}/64)(Oscillator Frequency)

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

Using Timer 1 to Generate Baud Rates
When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

Modes 1,3 Baud Rate = (2^{SMOD}/32)(Timer 1 Overflow Rate)

The Timer 1 interrupt should be disabled in this application . The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In most typical applications, it is configured for "timer operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case the baud rate is given by the formula:

Mode 1, 3 Baud Rate = {(2^{SMOD}/32) x (Oscillator Frequency)} / {12 x (256 - (TH1)}

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload. Table 4 lists various commonly used baud rates and how they can be obtained from Timer 1.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

Using Timer 2 to Generate Baud Rates

Timer 2 is selected as the baud rate generator by setting RTCLK in T2CON (Figure 14). Setting RTCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 14.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

Now, the baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as follows:

Modes 1,3 Baud Rate = (Timer 2 Overflow Rate) / 16

The Timer can be configured for either "timer" or "counter" operation. In the most typical applications, it is configured for "timer" operation (C/T2 = 0). "Timer" operation is a little different for Timer 2 when it's being used as a baud rate generator. Normally, as a timer is would increment every machine cycle (thus at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (thus at 1/2 the oscillator frequency). In that case the baud rate is given by the formula.

Modes 1,3 Baud Rate = (Oscillator Frequency) / {32 x (65536 - (RCAP2H, RCAP2L)}

Where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 14. This Figure is valid only if RTCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Therefore, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt, if desired.

It should be noted that when Timer 2 is running (TR2 = 1) in "timer" function in the baud rate generator mode, one should not try to read or write TH2 or TL2. Under these conditions the Timer is being incremented every state time, and the results of a read or write may not be accurate. The RCAP registers may be read, but shouldn't be written to, because a write might overlap a reload and cause write and/or reload errors. Turn the Timer off (clear TR2) before accessing the Timer 2 or RCAP register, in this case.
this case

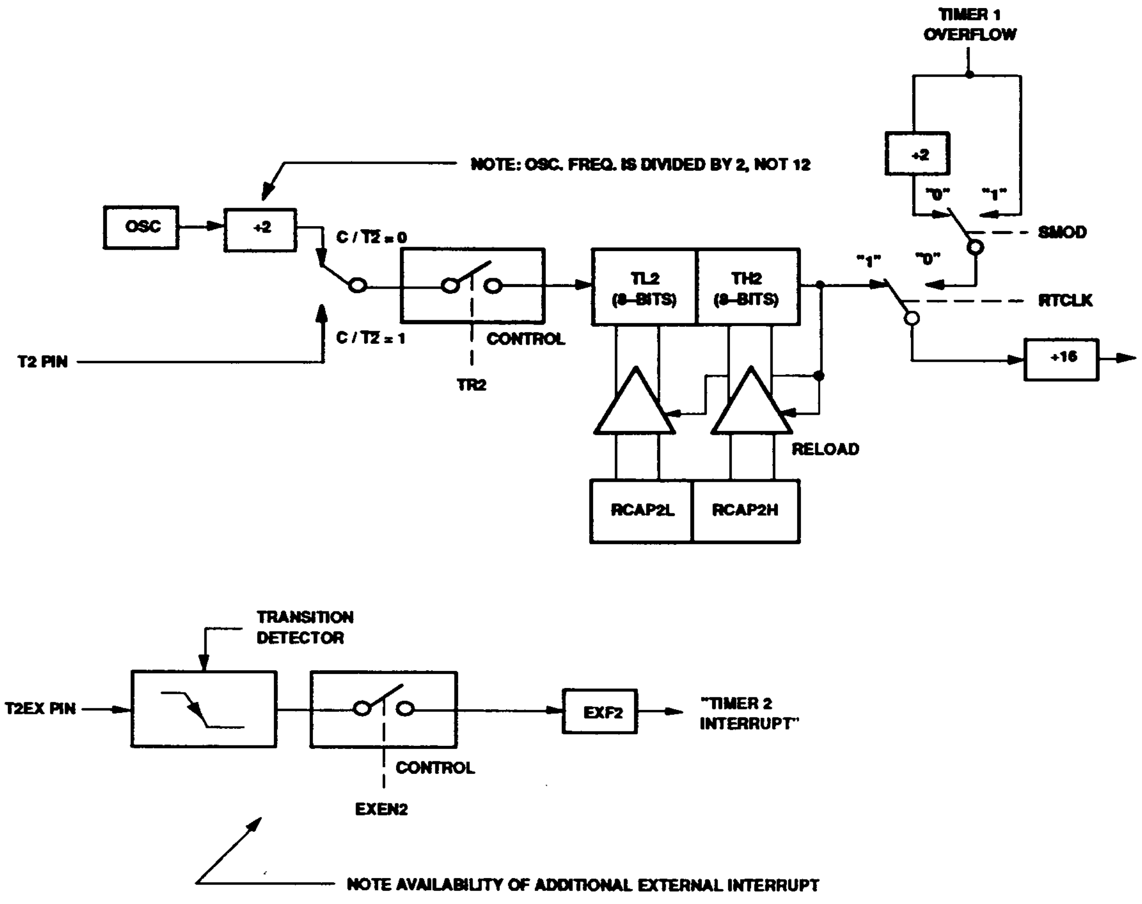


Figure 11. Timer 2 in Baud Rate Generator Mode

1 .7 Interrupt system

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a multiple-source, two-priority-level, nested interrupt system is provided. The 83CL781 acknowledges interrupt requests from fifteen sources as follows:

- INT0 through INT9
- Timer 0, Timer 1, and Timer 2
- I²C bus serial I/O
- UART

Each interrupt vectors to a separate location in program memory for its service routine. Each source can be individually enabled or disabled by corresponding bits in the Interrupt Enable Registers (IE, IE0). The priority level is selected via the Interrupt Priority register (IP0, IP1). All enabled sources can be globally disabled or enabled.

1 .7.1 External Interrupts INT2/INT9

Port 1 lines serve an alternative purpose as seven additional interrupts INT2 to INT9. When enabled, each of these lines may "wake-up" the device from Power-down mode. Using the IX1 register, each pin may be initialized to either active HIGH or LOW. IRQ1 is the interrupt request flag register. Each flag, if the interrupt is enabled, will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled.

The port 1 interrupts are level sensitive. A port 1 interrupt will be recognized when a level (HIGH or LOW depending on Interrupt Polarity Register IX1) on P1x is held active for at least one machine cycle. The Interrupt Request is not served until the next machine cycle.

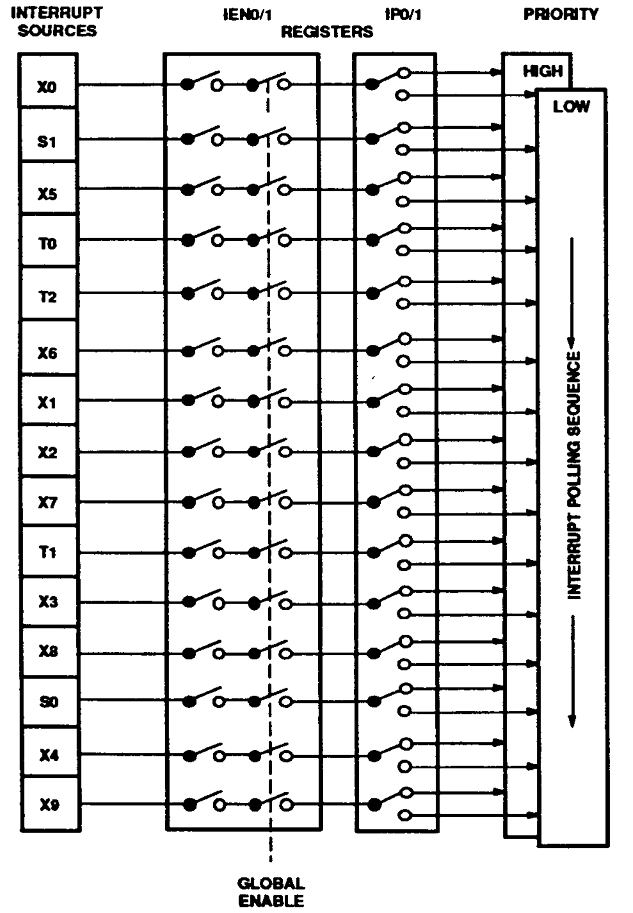


Figure 12. Interrupt System

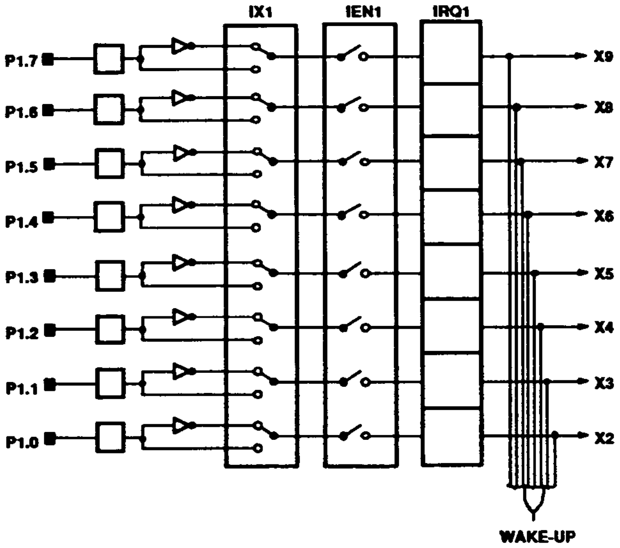


Figure 13. External Interrupt Configuration

Interrupt Enable Register IEN0, IEN1

IEN0 (A8H)	EA	ET2	ES1	ES0	ET1	EX1	ET0	EX0

BIT	SYMBOL	FUNCTION
IEN0.7	EA	General enable/ disable control 0 = no interrupt is enabled; 1=any individually enabled interrupt will be accepted
IEN0.6	ET2	Enable T2 interrupt
IEN0.5	ES1	Enable I²C interrupt
IEN0.4	ES0	Enable UART SIO interrupt
IEN0.3	ET1	Enable Timer T1 interrupt
IEN0.2	EX1	Enable external interrupt 1
IEN0.1	ET0	Enable Timer T0 interrupt
IEN0.0	EX0	Enable external interrupt 0

IEN1 (E8H)	EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

BIT	SYMBOL	FUNCTION
IEN1.7	EX9	Enable external interrupt 9
IEN1.6	EX8	Enable external interrupt 8
IEN1.5	EX7	Enable external interrupt 7
IEN1.4	EX6	Enable external interrupt 6
IEN1.3	EX5	Enable external interrupt 5
IEN1.2	EX4	Enable external interrupt 4
IEN1.1	EX3	Enable external interrupt 3
IEN1.0	EX2	Enable external interrupt 2

where 0 = interrupt disabled
1 = interrupt enabled

Interrupt Priority Register IP0, IP1

IP0 (B8H)	-	PT2	PS1	PS0	PT1	PX1	PT0	PX0

BIT	SYMBOL	FUNCTION
IP0.7	-	Unused
IP0.6	PT2	Timer 2 interrupt priority level
IP0.5	PS1	Unused
IP0.4	PS0	UART SIO interrupt priority level
IP0.3	PT1	Timer 1 interrupt priority level
IP0.2	PX1	External interrupt 1 priority level
IP0.1	PT0	Timer 0 interrupt priority level
IP0.0	PX0	External interrupt 0 priority level

IP1 (F8H)	PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2

BIT	SYMBOL	FUNCTION
IP1.7	PX9	External interrupt 9 priority level
IP1.6	PX8	External interrupt 8 priority level
IP1.5	PX7	External interrupt 7 priority level
IP1.4	PX6	External interrupt 6 priority level
IP1.3	PX5	External interrupt 5 priority level
IP1.2	PX4	External interrupt 4 priority level
IP1.1	PX3	External interrupt 3 priority level
IP1.0	PX2	External interrupt 2 priority level

Interrupt priority is as follows:
0 = low priority
1 = high priority

Interrupt Polarity Register IX1

IX1 (E9H)	IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Writing either a "1" or "0" to an IX1 register bit sets the polarity level of the corresponding external interrupt to active HIGH or LOW respectively.

BIT	SYMBOL	FUNCTION
IX1.7	IL9	External interrupt 9 polarity level
IX1.6	IL8	External interrupt 8 polarity level
IX1.5	IL7	External interrupt 7 polarity level
IX1.4	IL6	External interrupt 6 polarity level
IX1.3	IL5	External interrupt 5 polarity level
IX1.2	IL4	External interrupt 4 polarity level
IX1.1	IL3	External interrupt 3 polarity level
IX1.0	IL2	External interrupt 2 polarity level

Interrupt Request Flag Register IRQ1

IRQ1 (C0H)	IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

BIT	SYMBOL	FUNCTION
IRQ1.7	IQ9	External interrupt 9 request flag
IRQ1.6	IQ8	External interrupt 8 request flag
IRQ1.5	IQ7	External interrupt 7 request flag
IRQ1.4	IQ6	External interrupt 6 request flag
IRQ1.3	IQ5	External interrupt 5 request flag
IRQ1.2	IQ4	External interrupt 4 request flag
IRQ1.1	IQ3	External interrupt 3 request flag
IRQ1.0	IQ2	External interrupt 2 request flag

1 .7.2 Interrupt vectors

(highest)	Vector	Source
X0	0003H	external/0
S1	002BH	I²C port
X5	0053H	external 5
T0	000BH	timer 0
T2	0033H	timer 2
X6	005BH	external 6
X1	0013H	external 1
X2	003BH	external 2
X7	0063H	external 7
T1	001BH	timer 1
X3	0043H	external 3
X8	006BH	external 8
S0	0023H	UART
X4	004BH	external 4
X9	0073H	external 9
(lowest)		

Interrupt Priority
Each interrupt priority source can be set to either high or low priority. If both priorities are requested simultaneously, the controller will branch to the high priority vector.

A low priority interrupt can only be interrupted by a high priority interrupt. A high priority interrupt routine cannot be interrupted.

1 .7.3 Related registers

The following registers are used in conjunction with the interrupt system:

REGISTER	FUNCTION	SFR ADDRESS
IX1	Interrupt polarity register	E9H
IRQ1	Interrupt request flag register	C0H
IEN0	Interrupt enable register	A8H
IEN1	Interrupt enable register (INT2-INT9)	E8H
IP0	Interrupt priority register	B8H
IP1	Interrupt priority register (INT2-INT9)	F8H

1.8 Oscillator circuitry

The on-chip oscillator circuitry of the 83CL781 is a single-stage inverting amplifier biased by an internal feedback resistor (Figure 21). For operation as a standard quartz oscillator, no external components are needed (except at 32 kHz). When using external capacitors, ceramic resonators, coils and RC networks to drive the oscillator, five different configurations are supported (see Figure 22 and oscillator options).

In the Power-down mode the oscillator is stopped and XTAL1 is pulled HIGH. The oscillator inverter is switched off to ensure no current will flow regardless of the voltage at XTAL1. To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Figure 22(f). There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is buffered by a flip-flop.

The following options are provided for optimum on-chip oscillator performance. Please state option when ordering.

1.8.1 Oscillator options (see Figure 22)

32kHz: Figure 22(c). An option for 32kHz clock applications with external trimmer for frequency adjustment. A 4.7MΩ bias resistor is needed for use in parallel with the crystal.

Osc 2: Figure 22(e): An option for low-power, low-frequency operations using LC components.

Osc 3: An option for medium frequency range applications.

Osc 4: An option for high frequency range applications.

RC: Figure 22(g). An option for an RC oscillator.

The equivalent circuit data of the internal oscillator compares with that of matched crystals.

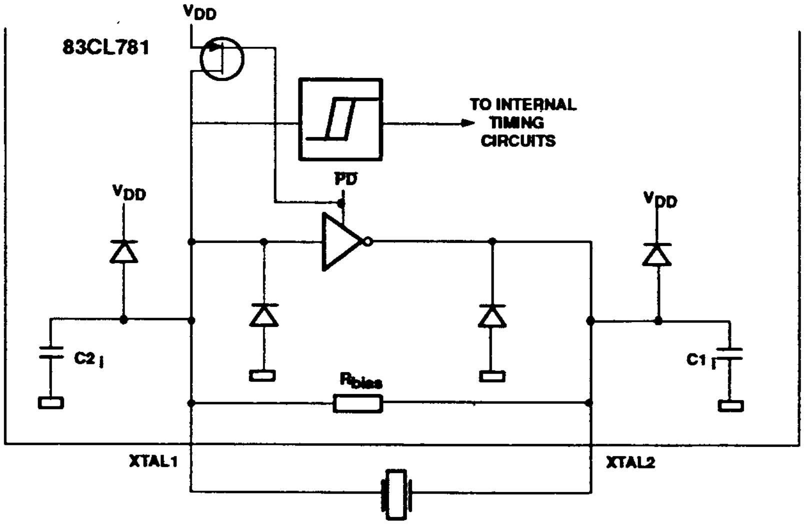


Figure 14. Oscillator

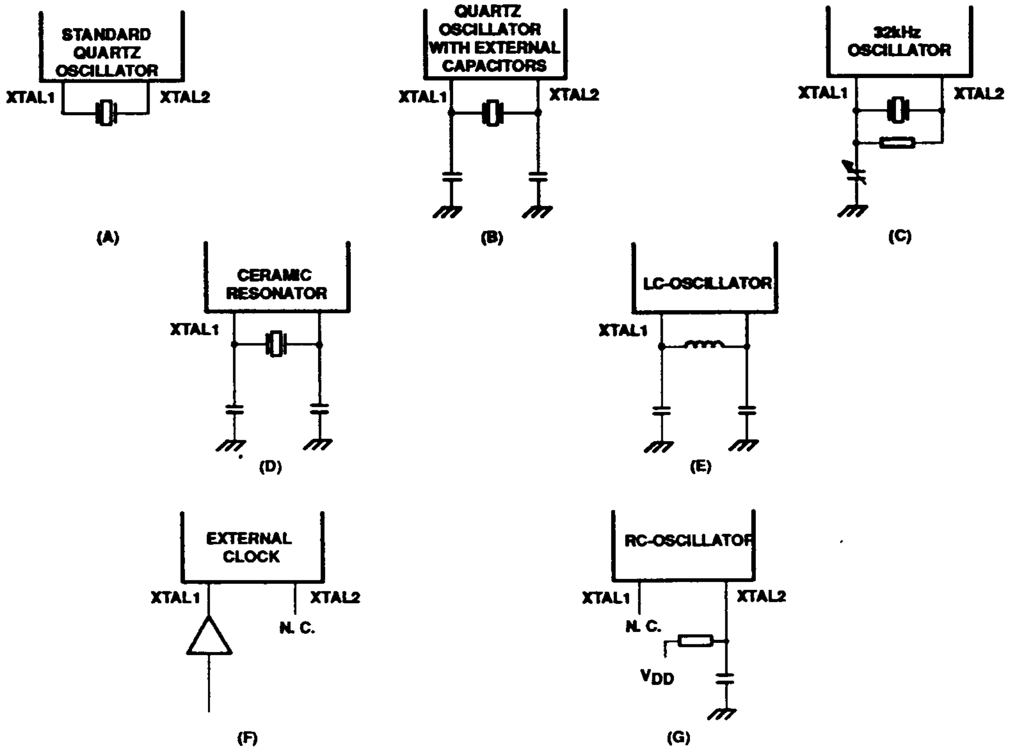


Figure 15. Alternative Oscillator Configurations

OSCILLATOR TYPE SELECTION GUIDE

RESONATOR	f (MHz)	OPTION	C1 EXT. (pF)		C2 EXT. (pF)		MAX. RESONATOR SERIES RESISTANCE
			MIN	MAX	MIN	MAX	15kΩ [4]
Quartz	0.032	32kHz	5	15	0	0	600Ω
Quartz	1.0	Osc.2	0	30	0	30	100Ω
Quartz	3.58	Osc.2	0	15	0	15	75Ω
Quartz	4.0	Osc.2	0	20	0	20	60Ω
Quartz	6.0	Osc.3	0	10	0	10	60Ω
Quartz	10.0	Osc.4	0	15	0	15	40Ω
Quartz	12.0	Osc.4	0	10	0	10	20Ω
PXE	0.455	Osc.2	40	50	40	50	100Ω
PXE	1.0	Osc.2	15	50	15	50	10Ω
PXE	3.58	Osc.2	0	40	0	40	10Ω
PXE	4.0	Osc.2	0	40	0	40	5Ω
PXE	6.0	Osc.2	0	20	0	20	6Ω
PXE	10.0	Osc.3	0	15	0	15	6Ω
PXE	12.0	Osc.4	10	40	10	40	10μH = 1Ω
LC		Osc.2	20	90	20	90	100μH = 5Ω 1mH = 75Ω

NOTES:

2. 32kHz quartz crystals with a series resistance higher than 15kΩ will reduce the guaranteed supply voltage range to 2.5 - 3.5V.

OSCILLATOR EQUIVALENT CIRCUIT PARAMETERS (see Figure 23)

PARAMETER	OPTION	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Transconductance	32kHz	g_m	T = +25°C, V_{DD} = 4.5V	—	15	—	µS
	Osc.2	g_m	T = +25°C, V_{DD} = 4.5V	200	600	1000	µS
	Osc.3	g_m	T = +25°C, V_{DD} = 4.5V	400	1500	4000	µS
	Osc.4	g_m	T = +25°C, V_{DD} = 4.5V	1000	4000	10000	µS
Input capacitance	32kHz	$C1_i$		—	3.0	—	pF
	Osc.2	$C1_i$		—	8.0	—	pF
	Osc.3	$C1_i$		—	8.0	—	pF
	Osc.4	$C1_i$		—	8.0	—	pF
Output capacitance	32kHz	$C2_i$		—	23	—	pF
	Osc.2	$C2_i$		—	8.0	—	pF
	Osc.3	$C2_i$		—	8.0	—	pF
	Osc.4	$C2_i$		—	8.0	—	pF
Output resistance	32kHz	R2		—	3800	—	kΩ
	Osc.2	R2		—	65	—	kΩ
	Osc.3	R2		—	18	—	kΩ
	Osc.4	R2		—	5.0	—	kΩ

1. The equivalent circuit data of internal oscillator compares with that of matched crystals.

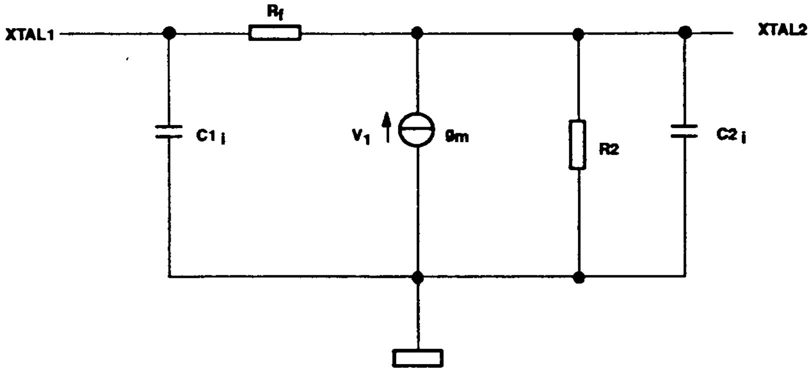


Figure 16. Equivalent Circuit Diagram

1.8.2 RC Oscillator

The externally adjustable RC-oscillator has a frequency range from 100 kHz to 500 kHz.

1.9 Reset circuitry

To initialize the 83CL781, a reset is performed by either of two methods:

- via the RST pin
- via a power-on-reset

It leaves the internal registers as follows:

Register	Content
ACC	0000 0000
B	0000 0000
DPL	0000 0000
DPH	0000 0000
IE0	0000 0000
IE1	0000 0000
IP0	XX00 0000
IP1	0000 0000
IX1	0000 0000
IRQ1	0000 0000
PCH	0000 0000
PCL	0000 0000
PCON	0XX0 0000
P0 - P3	1111 1111
S0BUF	XXXXXXXX
S0CON	0000 0000
S1ADR	0000 0000
S1CON	0000 0000
S1DAT	0000 0000
S1STA	1111 1000
SP	0000 0111
TCON	0000 0000
T2CON	0000 0000
T3	0000 0000
TH0, TH1, TH2	0000 0000
TL0, TL1, TL2	0000 0000
TMOD	0000 0000
PSW	0000 0000
RCAP2L	0000 0000
RCAP2H	0000 0000

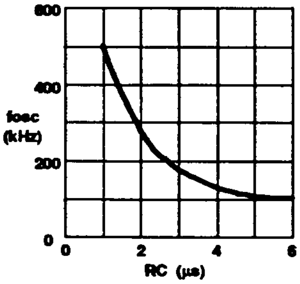


Figure 17. Frequency as a Function of RC

The reset state of the port pins is mask-programmable and can therefore be defined by the user. The standard reset value for port P0-P3 is 1111 1111.

The reset input to the 83CL781 is RST pin 15. A Schmitt trigger qualifies the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle.

A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods), while the oscillator is running. The CPU responds by generating an internal reset. Port pins adopt their reset state immediately after RST goes HIGH. During reset ALE and PSEN are held HIGH.

The external reset is asynchronous to the internal clock. The RST pin is sampled during State 5, Phase 2 of every machine cycle. After a HIGH is detected at the RST pin, an internal reset is repeated every cycle until RST goes LOW.

The internal RAM is not affected by reset. When V_{DD} is turned on the RAM contents are indeterminate.

1.9.1 Power-on reset

The 83CL781 contains on-chip circuitry which switch the port pins to the customer defined logic level as soon as V_{DD} exceeds 1.3 V. As soon as the minimum supply voltage is reached, the oscillator will start up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for a further 1536 oscillator periods.

A hysteresis of approximately 50mV at a typical power-on switching level of 1.3 V will ensure correct operation.

An automatic reset can be obtained at power-on by connecting the RST pin to V_{DD} via a 10 µF capacitor. At power-on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor discharges through the internal resistor R_{RST} to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles.

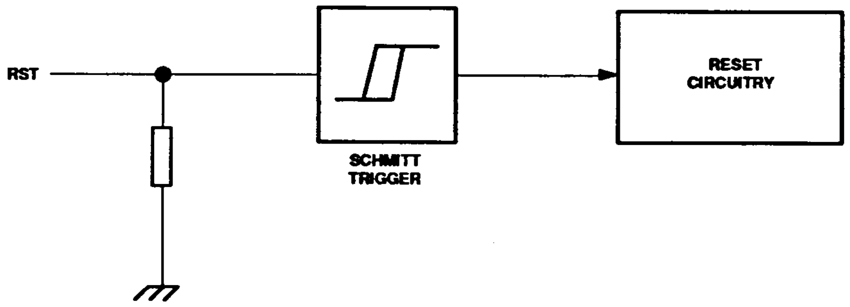


Figure 18. Reset Configuration at RST Pin

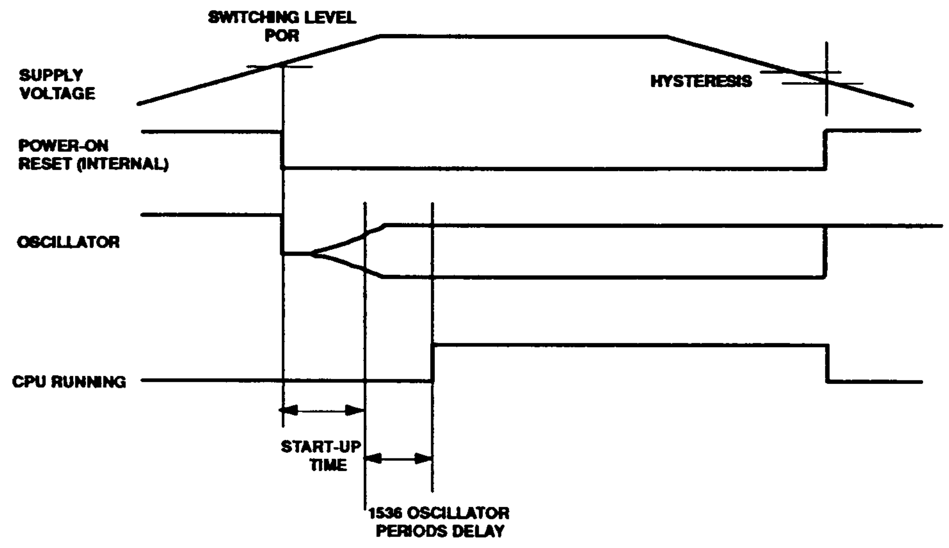


Figure 19. Power-on Reset Switching Level

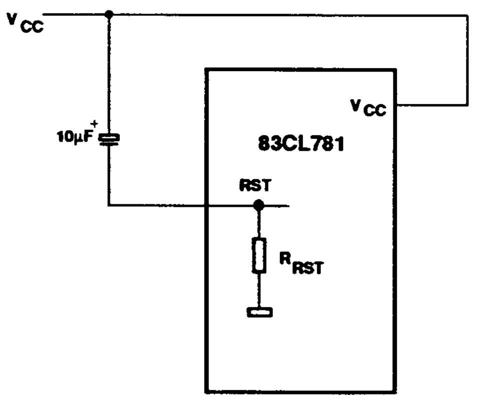


Figure 20. Recommended Power-on Reset Circuitry

2.0 INSTRUCTION SET

The 83CL781 uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes byte efficiency and execution speed. Assigned opcodes add new high-power operation and permit new addressing modes. The instruction set consists of 49 single-byte, 46 two-byte and 16 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 µs and 45 in 2 µs. Multiply and divide instructions execute in 4 µs.

Table 5. Instruction Set Description

MNEMONIC		DESCRIPTION	BYTES/ CYCLES		OPCODE (HEX.)
Arithmetic Operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	ADD immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@R	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@R	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@R	Decrement indirect RAM	1	1	16,17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A & B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4
Logic Operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A, direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANI	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42

Table 5. Instruction Set Description (Continued)

MNEMONIC		DESCRIPTION	BYTES/ CYCLES		OPCODE (HEX.)
Logic Operations (continued)					
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right throught the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4
Data Transfer					
MOV*	A,Rr	Move register to A	1	1	E*
MOV	A,direct	Move direct byte to A	2	1	E5
MOV	A@R	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E3, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	MOV A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5

Table 5. Instruction Set Description (Continued)

MNEMONIC		DESCRIPTION	BYTES/ CYCLES		OPCODE (HEX.)
Data Transfer (continued)					
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7
Boolean Variable Manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and Machine Control					
ACALL	addr11	Absolute subroutine call	2	2	**1addr
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	***1addr
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if no carry flag	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immediate to register and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immediate to ind. and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

NOTES TO TABLE 5:

Data addressing modes

Rr Working register R0-R7.

direct 128 internal RAM locations and any special function register (SFR).

@Ri Indirect internal RAM location addressed by register R0 or R1.

#data 8-bit constant included in instruction.

#data 16-bit constant included in instruction.

bit Direct addressed bit in internal RAM or SFR.

addr16 16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64K-byte program memory address space.

addr11 11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2K-byte page of program memory as the first byte of the following instruction.

rel Signed (two's complement) 8-bit offset byte. Used by SMJP and all conditional jumps. Range is -128 to +128 bytes relative to first byte of the following instruction.

Hexadecimal opcode cross-reference

* : 8, 9, A, B ,C ,D ,E ,F.

** : 11, 31, 51, 71, 91, B1, D1, F1.

*** : 01, 21 , 41, 61, 81, A1, C1, E1.

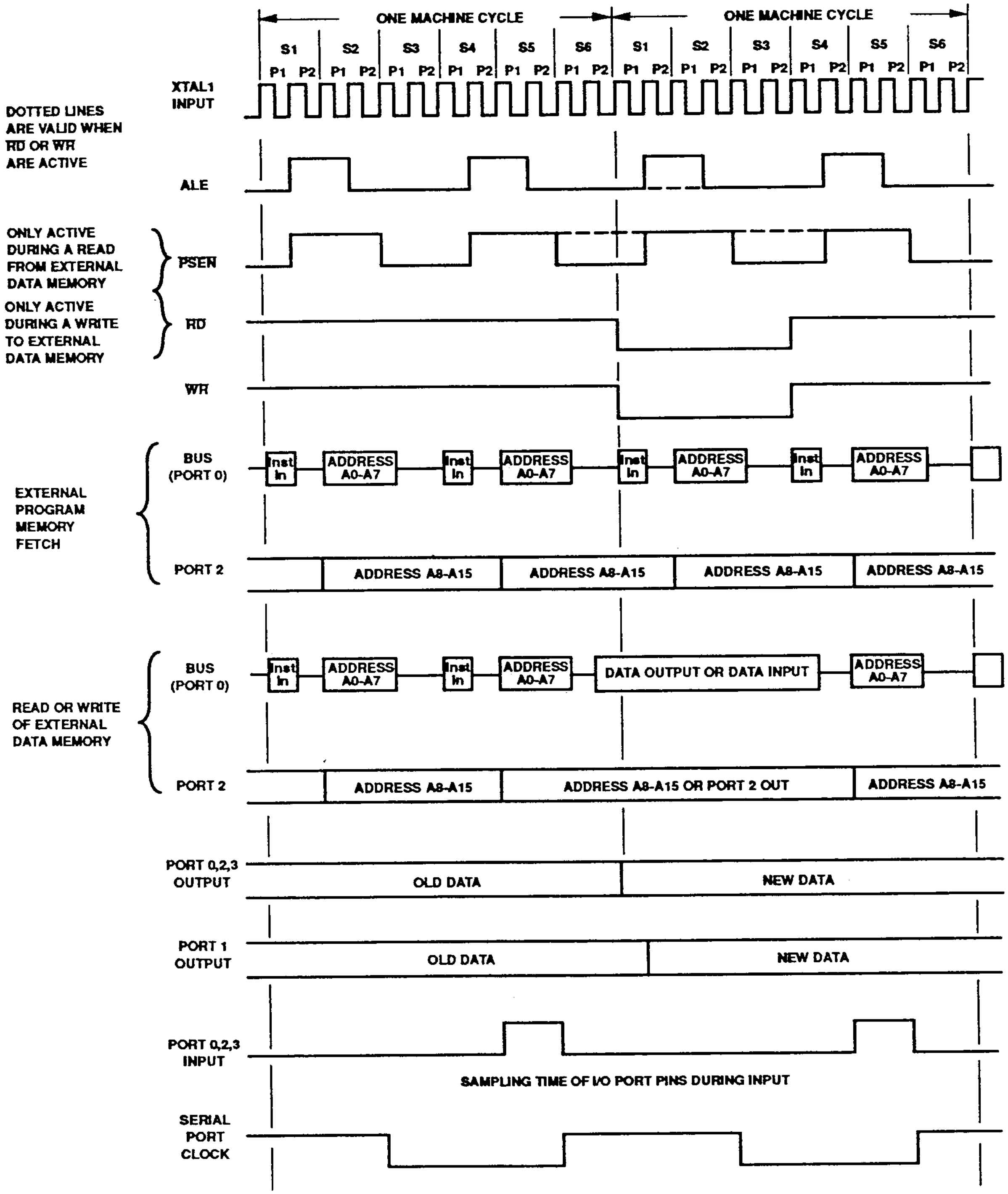

ONE MACHINE CYCLE
ONE MACHINE CYCLE
S1 S2 S3 S4 S5 S6 S1 S2 S3 S4 S5 S6
P1 P2
XTAL1 INPUT
DOTTED LINES ARE VALID WHEN RD OR WR ARE ACTIVE
ALE
ONLY ACTIVE DURING A READ FROM EXTERNAL DATA MEMORY
PSEN
ONLY ACTIVE DURING A WRITE TO EXTERNAL DATA MEMORY
RD
WR
EXTERNAL PROGRAM MEMORY FETCH
BUS (PORT 0)
Inst In
ADDRESS A0-A7
PORT 2
ADDRESS A8-A15
READ OR WRITE OF EXTERNAL DATA MEMORY
DATA OUTPUT OR DATA INPUT
ADDRESS A8-A15 OR PORT 2 OUT
PORT 0,2,3 OUTPUT
OLD DATA
NEW DATA
PORT 1 OUTPUT
PORT 0,2,3 INPUT
SAMPLING TIME OF I/O PORT PINS DURING INPUT
SERIAL PORT CLOCK

Figure 21. Instruction Cycle Timing

3.0 RATINGS

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{DD}	Supply voltage (Pin 40)	-0.5	6.5	V
V_I	All input voltages	-0.5	V_{DD}+0.5	V
I_I, I_O	DC current into any input or output	—	5	mA
P_{tot}	Total power dissipation	—	300	mW
T_{stg}	Storage temperature range	-65	+150	°C
T_{amb}	Operating ambient temperature range	-40	+85	°C
T_j	Operating junction temperature	—	125	°C

4.0 DC ELECTRICAL CHARACTERISTICS

V_{DD} = 1.8V to 6V; V_{SS} = 0V; T_{amb} = -40°C to +85°C, all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Supply voltage		1.8	—	6.0	V
	RAM retention voltage in power-down mode		1.0	—	6.0	V
I_{DD}	Power supply current: Operating (note 1)	V_{DD} = 5V; f_{clk} = 12 MHz	—	—	tbf	mA
		V_{DD} = 3V; f_{clk} = 3.58 MHz	—	—	tbf	µA
	Idle mode (note 2)	V_{DD} = 5V; f_{clk} = 12 MHz	—	—	tbf	mA
		V_{DD} = 3V; f_{clk} = 3.58 MHz	—	—	tbf	mA
I_{PD}	Power-down mode (note 3)	V_{DD} = 1.8V; T_{amb} = 25 °C	—	—	10	µA
V_{IL}	Input low voltage (note 6)		V_{SS}	—	$0.3V_{DD}$	V
V_{IH}	Input high voltage (note 6)		$0.7V_{DD}$	—	V_{DD}	V
I_{OL}	Output sink current LOW, except SDA, SCL	V_{DD} = 5v; V_{OL} = 0.4V	1.6	—	—	mA
		V_{DD} = 2.5V; V_{OL} = 0.4V	0.7	—	—	mA
	Output sink current, SDA, SCL	V_{DD} = 2.5v; V_{OL} = 0.4V	3.0	—	—	mA
$-I_{OH}$	Output source current HIGH, push-pull options only	V_{DD} = 5v; V_{OH} = V_{DD}-0.4V	1.6	—	—	mA
		V_{DD} = 3v; V_{OH} = V_{DD}-0.4V	0.7	—	—	mA
$-I_{IL}$	Input current logic 0	V_{DD} = 5v; V_{IN} = 0.4V	—	—	100	µA
		V_{DD} = 3v; V_{IN} = 0.4V	—	—	50	µA
$-I_{TL}$	Input current logic 0, 1-to-0 transition	V_{DD} = 5v; V_{IN} = $V_{DD}/2$	—	—	1.0	mA
		V_{DD} = 3v; V_{IN} = $V_{DD}/2$	—	—	500	µA
$\pm I_{LI}$	Input leakage current (port P0, $\overline{EA}$)	$V_{SS} < V_I < V_{DD}$	—	—	10	µA
R_{RST}	RST pull-down resistor		10	—	200	kΩ

NOTES:

1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10ns; $V_{IL} = V_{SS}$ +0.5V; $V_{IH} = V_{DD}$ -0.5V; XTAL2 not connected; EA = RST + Port 0 = V_{DD}.
2. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10ns; V_{SS} = 0.5V; $V_{IH} = V_{DD}$ -0.5V; XTAL2 not connected; EA = RST + Port 0 = V_{DD}.
3. The power-down current is measured with all output pins disconnected; XTAL1 not connected; EA = Port 0 = V_{DD}; RST = V_{SS}.
4. Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3 pins when these pins make a 1-to-0 transition during bus operations. In the most adverse conditions (capacitive loading >100 pF) the noise pulse on the ALE line may exceed 0.8 V. In this event it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger strobe input.
5. Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and PSEN to momentarily fall below the 0.9% of V_{DD} specification when the address bits are stabilizing.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^{2}C-bus specification, so an input voltage below 0.3 V_{DD} will be recognized as a logic 0, while an input voltage above 0.7 V_{DD} will be recognized as a logic 1.

5.0 AC CHARACTERISTICS

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V±10%; V_{SS} = 0V; T_{amb} = -40°C to +85°C; C_L = 50pF for Port 0, ALE and PSEN; C_L = 80pF for all other outputs unless otherwise specified.

SYMBOL	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
		MIN	MAX	MIN	MAX	
Program Memory (see Figure 29)						
t_{LL}	ALE pulse duration	127	—	$2t_{CK}$-40	—	ns
t_{AL}	Address set-up time to ALE	43	—	t_{CK}-40	—	ns
t_{LA}	Address hold time after ALE	48	—	t_{CK}-35	—	ns
t_{LC}	Time from ALE to control pulse PSEN	58	—	t_{CK}-25	—	ns
t_{LIV}	Time from ALE to valid instruction input	—	233	—	$4t_{CK}$-100	ns
t_{CC}	Control pulse duration PSEN	215	—	$3t_{CK}$-35	—	ns
t_{CIV}	Time from PSEN to valid instruction input	—	125	—	$3t_{CK}$-125	ns
t_{CI}	Input instruction hold time after PSEN	0	—	0	—	ns
t_{CIF}	Input instruction float delay after PSEN	—	63	—	t_{CK}-20	ns
t_{AC}	Address valid after PSEN	75	—	t_{CK}-8		ns
t_{AIV}	Address to valid instruction input	—	302	—	$5t_{CK}$-115	ns
t_{AFC}	Address float time to PSEN	12	—	0	—	ns

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V; V_{SS} = 0V; T_{amb} = -40°C to +85°C; C_L = 50pF for Port 0; ALE and PSEN, C_L = 40pF for all other outputs unless otherwise specified.

SYMBOL	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
		MIN	MAX	MIN	MAX	
External Data Memory (see Figures 30 and 31)						
t_{RR}	RD pulse duration	400	—	$6t_{CK}$-100	—	ns
t_{WW}	WR pulse duration	400	—	$6t_{CK}$-100	—	ns
t_{LA}	Address hold time after ALE	48	—	t_{CK}-35	—	ns
t_{RD}	RD to valid data input	—	150	—	$5t_{CK}$-165	ns
t_{DFR}	Data float delay after RD	—	97	—	$2t_{CK}$-70	ns
t_{LD}	Time from ALE to valid data input	—	517	—	$8t_{CK}$-150	ns
t_{AD}	Address to valid data input	—	585	—	$9t_{CK}$-165	ns
t_{LW}	Time from ALE to RD and WR	200	300	$3t_{CK}$-50	$3t_{CK}$+50	ns
t_{AW}	Time from address to RD or WR	203	—	4	—	ns
t_{WHLH}	Time from RD or WR HIGH to ALE HIGH	43	123	t_{CK}-130 t_{CK}-40	t_{CK}+40	ns
t_{DWX}	Data valid to WR transition	23	—	t_{CK}-60	—	ns
t_{DW}	Data set-up time before WR	433	—	$7t_{CK}$-150	—	ns
t_{WD}	Data hold time after WR	33	—	t_{CK}-50	—	ns
t_{AFR}	Address float delay after RD	—	12	—	12	ns

NOTES:

1. Interfacing the 83CL781 to devices with float times up to 75ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

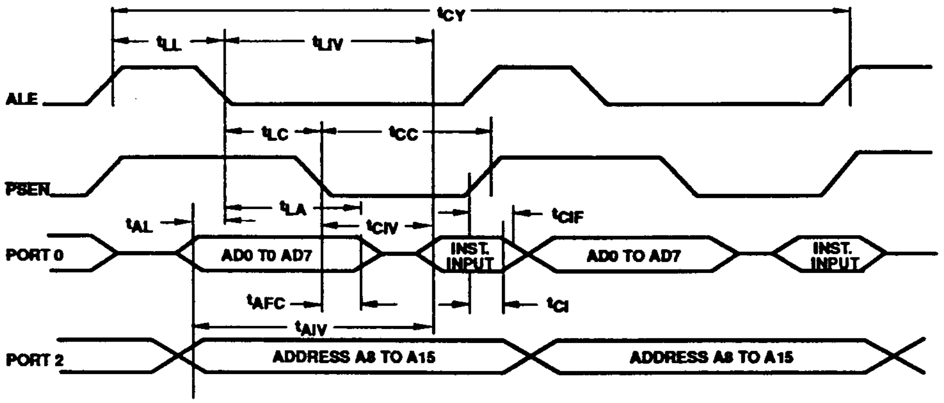


Figure 22. Read from Program Memory

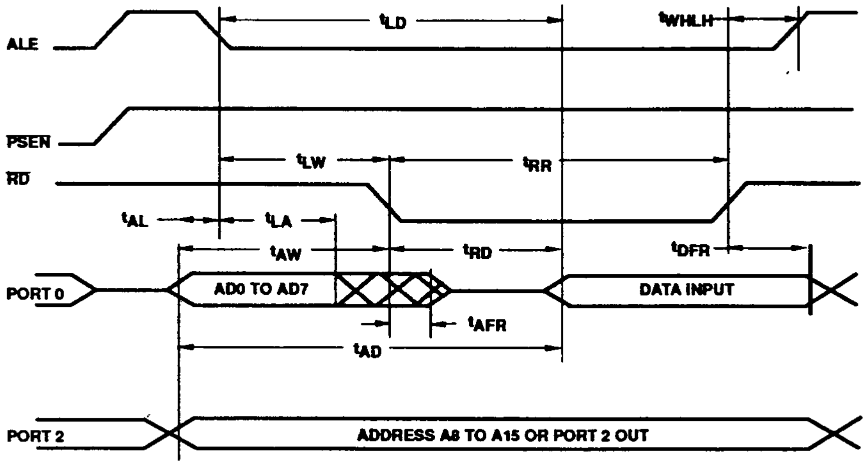


Figure 23. Read from Data Memory

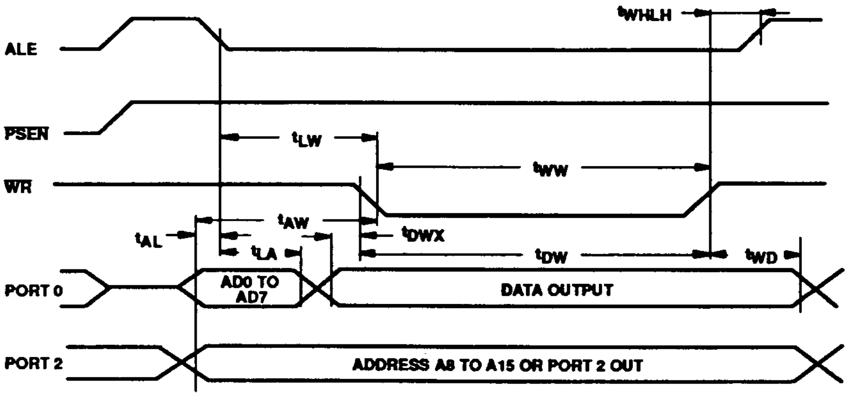


Figure 24. Write to Data Memory

2 .0 CHARACTERISTIC CURVES

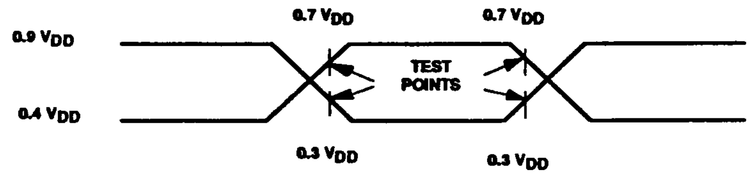


Figure 25. AC Testing Input Waveform

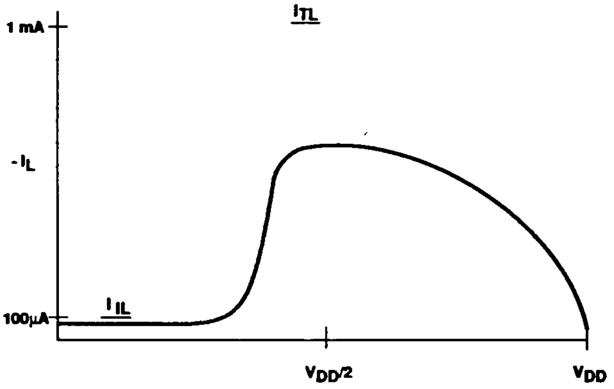


Figure 26. Input Current

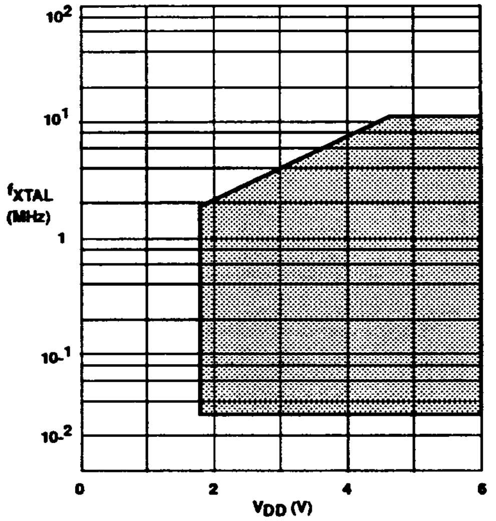


Figure 27. Frequency Operating Range

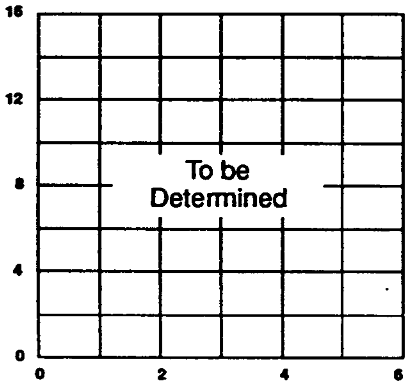


Figure 28. Typical Operating Current vs. Frequency and V_{DD}, T_{amb} = 25°C

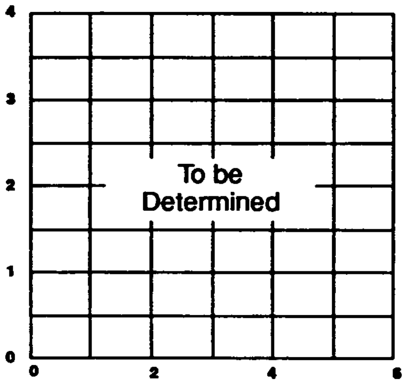


Figure 29. Typical Idle Current vs. Frequency and V_{DD}, T_{amb} = 25°C

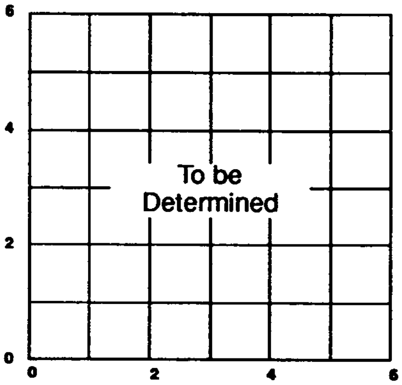


Figure 30. Typical Power-down Current vs. V_{DD}, T_{amb} = 25°C