82072
CHMOS HIGH INTEGRATION FLOPPY DISK CONTROLLER

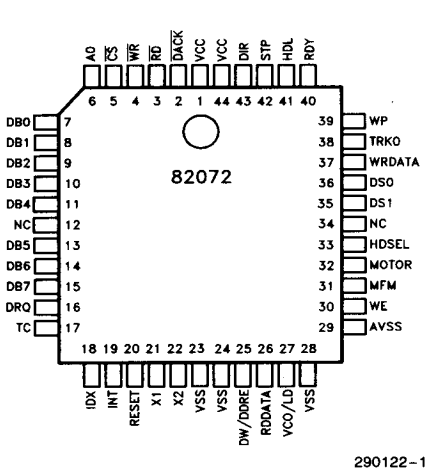
- **Integrated Analog Data Separator with Software Selectable Data Rates (250K, 300K, 500K, Bit/Sec-MFM Mode)**
- **16 Byte FIFO with Programmable Threshold**
- **High Speed Processor Interface**
  - **16 MHz iAPX 386— 1 Wait State**
  - **12.5 MHz iAPX 286—1 Wait State**
  - **8 MHz iAPX 286— 0 Wait State**
- **Programmable Internal Write Precompensation Delays**
- **Programmable Drive Motor On/Off Delays**
- **Addresses Up to 256 Tracks Directly, Supports Unlimited Tracks**
- **Implied Seek with Read/Write Disk Commands**
- **Software Compatible with 8272A**
- **Controls 8", 5¼" and 3½" Floppy Disk Drives**
- **Plastic 40 Pin DIP or 44 Pin PLCC Packages**

(See Packaging Spec. Order #231369)

The 82072 CHMOS high integration floppy disk controller solves the many complex disk drive and microprocessor interface issues that exist today, while maintaining software compatibility with the industry standard 8272A. Features include a sophisticated on-chip analog phase lock loop with software selectable data rates, write precompensation delay, and motor on/off delays to simplify the disk drive interface. System interfacing is enhanced with the addition of a FIFO which allows a more flexible system to be designed.

The standard 82072 supports a maximum data rate of 500 Kbits per second.

The 82072 is fabricated on Intel's advanced CHMOS III technology for minimal power consumption and is available in a plastic 40 pin DIP or a plastic 44-leaded chip carrier (PLCC) package.



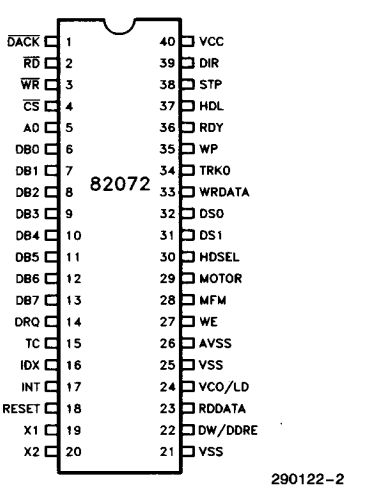


Figure 1. 82072 Pinout

October 1989
Order Number: 290122-006

Table 1. 82072 Pin Description

Symbol	DIP	PLCC	I/O	Function
$\overline{DACK}$	1	2	I	**DMA ACKNOWLEDGE:** DMA control line that qualifies the $\overline{RD}$ and $\overline{WR}$ inputs during DMA cycles.
$\overline{RD}$	2	3	I	**READ:** Control signal to transfer data to the data bus from the 82072.
$\overline{WR}$	3	4	I	**WRITE:** Control signal to transfer data into the 82072 from the data bus.
$\overline{CS}$	4	5	I	**CHIP SELECT:** Control signal that qualifies the $\overline{RD}$ and $\overline{WR}$ inputs.
A0	5	6	I	**ADDRESS:** **A0 $\overline{RD}$ $\overline{WR}$ Function** 0 0 0 Illegal * 0 0 1 Read Main Status Register 0 1 0 Write to the Data Rate Select Register ** 0 1 1 No Action 1 0 0 Illegal * 1 0 1 Read from FIFO 1 1 0 Write into FIFO 1 1 1 No Action * User must ensure that these inputs do not occur. ** Change from 8272A—was illegal.
DB0–7	6–13	7–11, 13–15	I/O	**DATA BUS:** Bidirectional 8-bit data bus. A0 determines whether transfer is to/from the FIFO or Main Status Register.
DRQ	14	16	O	**DMA REQUEST:** Used to request service from a DMA controller.
TC	15	17	I	**TERMINAL COUNT:** Control line from a DMA controller used to terminate requests for data transfers. Disk read and write commands complete the transfer to the current sector with valid CRC checking/generation.
IDX	16	18	I	**INDEX:** Disk drive signal that indicates the beginning of a track. It is used to count retries and delay periods for internal (i.e. Motor On/Off) timers and is rising edge triggered.
INT	17	19	O	**Interrupt:** Interrupt to host to indicate command completion or that a data transfer is required (depending upon the data transfer mode). Command completion interrupts are cleared by reading the ST0 Status Register. Data transfer interrupts are cleared when the amount of data in the FIFO reaches the full or empty level (depending on FIFO direction) or a TC is issued.
RESET	18	20	I	**RESET:** Places the 82072 in a known idle state. All disk outputs are set to a low level. All registers, except those set by the SPECIFY command, are cleared. From the trailing edge of Reset, there is a maximum delay of 8 microseconds until the Main Status register is valid. Following reset, the 82072 defaults to polling enabled. The default values for the new features are: internal data separator enabled, write precompensation value is 125 ns, MOTOR on delay is 0.0 sec., MOTOR off delay is 5.2 sec., data rate is dependent on DDRE setting, FIFO disabled.

Table 1. 82072 Pin Description (Continued)

Symbol	DIP	PLCC	I/O	Function
X1	19	21	I	**CRYSTAL 1:** External connection for a fundamental mode parallel resonant 24 MHz crystal for the internal oscillator. May be driven with a MOS level clock instead of a crystal. Refer to the D.C. Specifications.
X2	20	22	I	**CRYSTAL 2:** If an external clock is supplied on X1, this input must be left unconnected (floating).
V_{SS}	21, 25	23, 24, 28		**LOGIC GROUND.**
DW/DDRE	22	25	I	**DATA WINDOW/DEFAULT DATA RATE ENABLED:** Clock from the external PLL logic used to sample the Read Data input. When the internal PLL is used, this input pin is used to define the data rate and write precompensation values after RESET. DDRE tied high will cause the data rate and precompensation bits of the DSR to be reinitialized to the default values of 250 Kbps and 125 ns delay when a hardware/software reset is issued. DDRE tied low will cause the current data rate and precompensation values in the DSR to be retained when a hardware reset is issued. When a software reset is issued, the DSR will contain those values written into the register. DDRE tied low should be used in applications where data rate and precompensation information needs to be retained regardless of chip reset.
RDDATA	23	26	I	**READ DATA:** Serial FM or MFM encoded data from the disk drive.
VCO/LD	24	27	O	**READ DATA GATE:** This active high output enables an external PLL to synchronize to Read Data input from the disk drive. **LOW DENSITY:** This active high output is used by quad density disk drives to modify Read/Write head and data channel characteristics. This signal is activated when internal PLL is enabled and a data transfer rate of 250 or 300 Kbps is chosen.
AVSS	26	29		Analog ground for the Data Separator. It is recommended that care be taken to keep AVSS as noise free as possible. A separate connection to the ground plane is suggested.
WE	27	30	O	**WRITE ENABLE:** Disk drive control signal that enables the head to write onto the disk.
MFM	28	31	O	**MFM MODE:** When an external PLL is used, this output selects between single and double density (FM and MFM) modes. 1 = MFM, 0 = FM mode.
MOTOR	29	32	O	**MOTOR ENABLE:** Output used to activate the drive motor on the selected drive. Delays are programmable. With one output, this pin must be qualified with the drive select logic to provide motor enables for each drive.
HDSEL	30	33	O	**HEAD SELECT:** Signal used to select one of two sides on the disk. A 0 = side 0, a 1 = side 1.
DS1, 0	31, 32	35, 36	O	**DRIVE SELECT:** These outputs select one of four disk drives. DS0, DS1 = 0, 0 will select drive 0.
WRDATA	33	37	O	**WRITE DATA:** FM or MFM encoded serial data to the disk drive. No external precompensation is required.
TRK0	34	38	I	**TRACK 0:** Control line from the disk drive that indicates the head is on physical track 0 (outermost track).
WP	35	39	I	**WRITE PROTECT:** Input from the disk drive that indicates if the disk is physically write protected.

Table 1. 82072 Pin Description (Continued)

Symbol	DIP	PLCC	I/O	Function
RDY	36	40	I	**READY:** Input from the disk drive that indicates whether the drive is ready for an operation.
HDL	37	41	O	**HEAD LOAD:** This output loads the head onto the disk drive if required. Typically used by 8" drives.
STP	38	42	O	**STEP:** Output used to supply step pulses to the disk drive.
DIR	39	43	O	**DIRECTION:** This output, in conjunction with STP, causes the drive to move the head outward if a "0", and inward if a "1".
VCC	40	1, 44		Logic DC power supply.

NOTE:
1. Pins 12, 34 of the 44 pin PLCC package are not connected.

INTRODUCTION

The 82072 has integrated all of the complex circuitry required to interface microprocessor systems with disk drives that comply with the IBM System 34 Double Density (MFM) format or the IBM 3740 single density format (FM). The 82072 is a superset of the 8272A. Control over the new features was accomplished by adding extra registers and commands to the 82072. The 82072 will function like the 8272A Floppy Disk Controller (FDC) after being reset, with the added features being set to 8272A compatible default values. When accessing the disk drives, the 82072 is programmed the same as the 8272A.

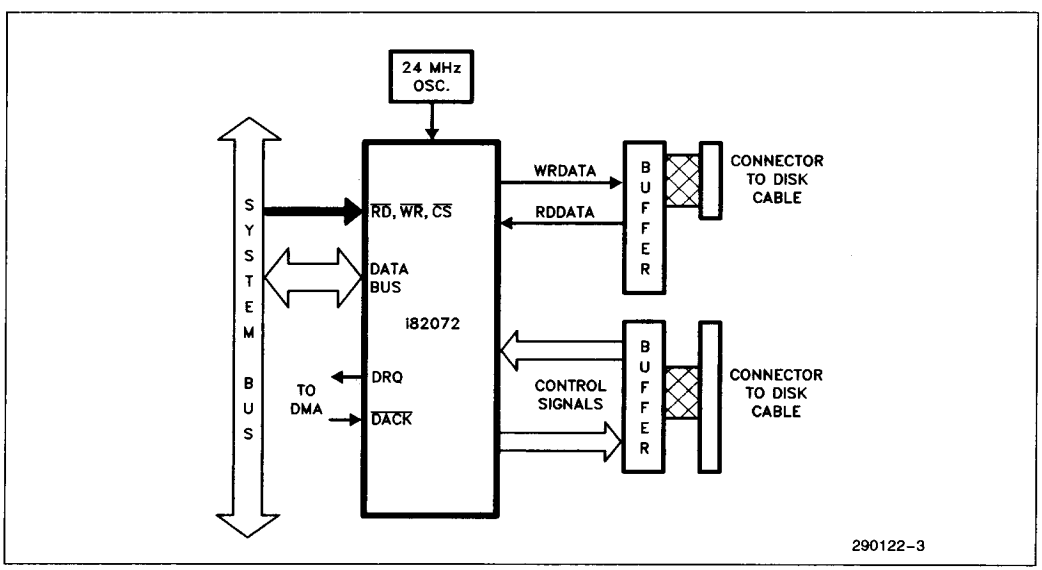


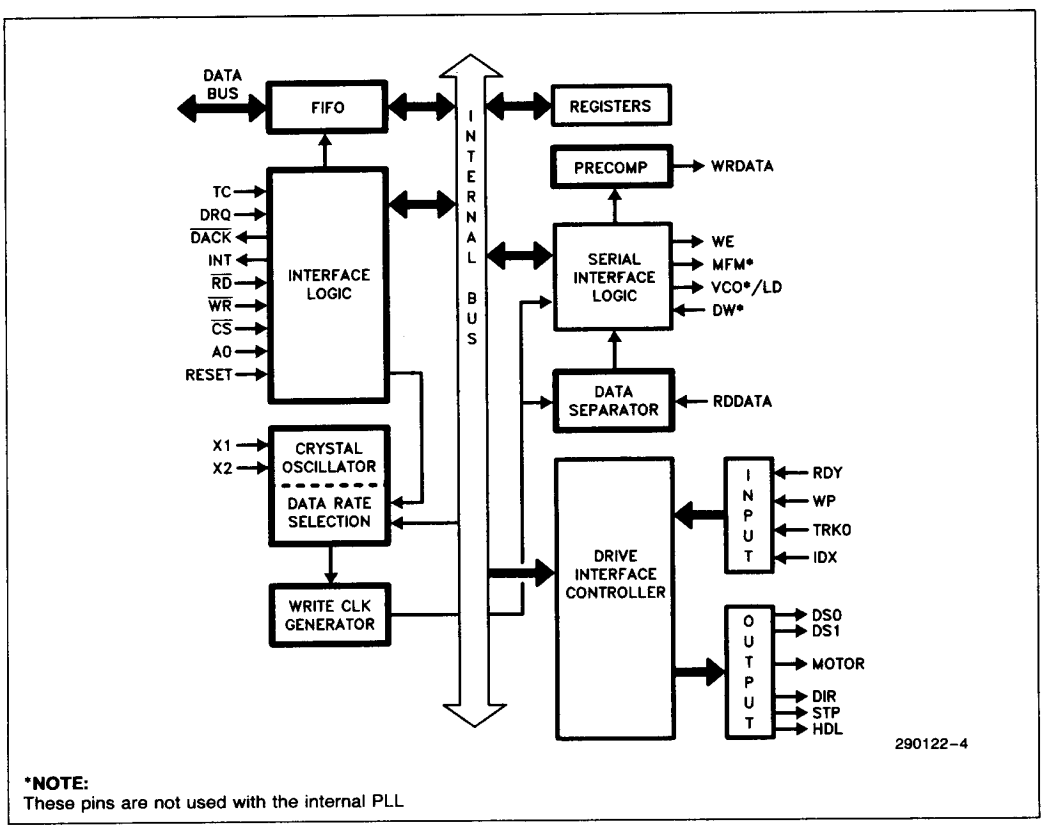
Figure 2. 82072 Typical System Block Diagram

The microprocessor interface was enhanced by adding a 16 byte FIFO to reduce the timing constraints that most floppy disk controllers impose upon a system. The point at which the 82072 generates a request for a data transfer is selectable within the 16 byte range of the FIFO. The interface was further enhanced to support todays faster microprocessors (i.e., 8 MHz 80286, 10 MHz 80186) without incurring wait states. A powerdown mode has been added for low power or portable applications. With one command, the 82072 resets itself and then disconnects the power from the internal oscillator. Reset will reconnect the clock and once the 82072 is reprogrammed (if necessary), it will be ready to read and write disks again.

All of the control logic of the disk interface has been integrated into the 82072. Flexibility is maintained by allowing the user to select read and write data rates (without any external hardware); write precompensation delays; motor on/off delay; and the track to start the precompensation on. The typical design will need the 82072, a crystal and high current drivers for the signals that interface to the disk drive. The new features (when used) need only to be chosen once after reset (although they may be modified at any time). From then on, the user programs the 82072 for disk accesses in the same manner as the 8272A.

ARCHITECTURE

Figure 3 is a block diagram of the 82072. The highlighted blocks represent areas that are either completely new or highly enhanced. All new features were adopted with the requirement of being software compatible with the 8272A.



*NOTE:
These pins are not used with the internal PLL

Figure 3. 82072 Block Diagram

Summary of Differences Between the 8272A and the 82072

Table 2 lists the features that are different between the 8272A and the 82072. The Scan commands are not supported by the 82072.

Table 2. Summary of Differences Between 82072 and 8272A

Features	82072	8272A
Process	CHMOS III	HMOS II
Data Separator	Internal	User Supplied
Data Rates	Up to 500 Kbit/sec. Software Selectable Without Hardware	Up to 500 kbit/sec External Hardware Needed
Power Down Mode	Internal	None
Commands	Superset of 8272A	
Host Interface	16 byte FIFO	1 byte Register
Software Reset	Yes	None
Implied Seeks	Yes	None
Relative Seek	Yes	None
Motor Delays	Yes	External Hardware
Write Precompensation Delays	Yes	External Hardware
Recalibrate	Issues 255 Step Pulses	Issues 77 Step Pulses

Crystal Oscillator Specification

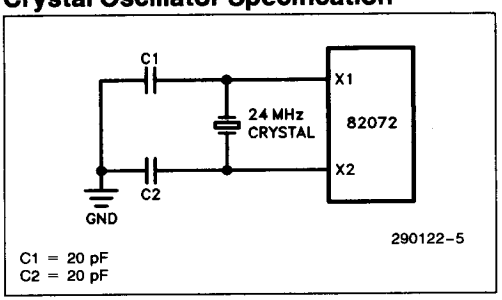


Figure 4. Crystal Oscillator Circuit

Specification of the parallel resonant crystal (typical values):

Frequency:	24 MHz ±0.1%
Mode:	Parallel resonant Fundamental mode
Series Resistance:	R_S = <40Ω
Motional Inductance:	L = 2.2 mH
Motional Capacitance:	C = 0.02 pF
Shunt Capacitance:	C0 = 4.5 pF

The 24 MHz clock can be supplied either by a crystal or a MOS level square wave. All internal timings are referenced to this clock or a scaled count (which is determined by the data rate selection).

The crystal oscillator must be allowed to run for 10 mS after the VCC supply has reached 4.5 volts or 1 ms after the chip has been taken out of the Power-down mode before it is guaranteed to have stabilized.

MICROPROCESSOR INTERFACE

There are three ports accessible from the host's point of view; the FIFO, the Main Status Register (MSR) and the Data rate Select Register (DSR). Communication between the microprocessor and the 82072 is done by reading the Main Status register to determine if the controller is ready. If it is ready, a command, followed by the correct parameters, is sent to the 82072 through the FIFO (data port). The MSR can be read at any time and the DSR can be written at any time (before, during and after a command). The FIFO should only be accessed when the RQM bit in the MSR is set, or when DRQ is active if a DMA transfer is in progress.

MAIN STATUS REGISTER

RQM	DIO	NDM	CB	D3B	D2B	D1B	D0B
7	6	5	4	3	2	1	0

Bit 7—RQM (Request For Master)

This bit indicates that the host can access the FIFO (data port) if a "1". No accesses should be attempted if set to a "0".

Bit 6—DIO (Data In/Out)

Indicates the direction of the data transfer only when RQM is a "1". If DIO is a "1" the host should remove the bytes in the FIFO. A "0" means that the host should write into the FIFO.

Bit 5—NDM (Non-DMA Mode)

If the non-DMA mode is selected in the SPECIFY command, this bit will be set = "1" during the execution phase of a command. This bit is intended to support polled data transfers along with RQM and DIO. If DMA mode is selected, it remains a "0". This bit differentiates between the execution and result phases of a non-DMA READ DATA command.

Bit 4—CB (Controller Busy)

CB is set to a "1" when a command is in progress and indicates that the controller is processing a command. This bit will go active in the command phase after the command byte has been accepted. CB goes inactive at the end of the result phase which indicates the start of the next command phase. If the command has no result phase (i.e. SEEK and RECALIBRATE) the CB bit is cleared after receiving the last byte in the command phase.

Bit 0–3; Drive Busy

These bits are set only when a drive is in the seek portion of a command, including implied seeks, overlapped seeks and recalibrates.

FIFO

A 16 byte FIFO was added to increase the flexibility of a system when transferring data between the disk and memory by increasing the amount of time before service is required. This permits the 82072 to have a lower priority in servicing without losing data.

The 82072 FIFO is 16 bytes deep with the threshold set at any point (the threshold is set with the Configure command). The CONFIGURE command can enable the FIFO and set the FIFO threshold level. During writes into the FIFO (from the host), the 82072 will request service (via DRQ or INT-depending upon the selected transfer mode) when there are the programmed threshold number of bytes left in the FIFO. The request will go inactive once the FIFO is filled. When reading from the FIFO (to the host), service is requested when there are more than (16-threshold number) bytes in the FIFO. The request for service goes inactive when the FIFO is emptied. When the FIFO is disabled, a single byte per transfer protocol is enforced. The FIFO is still present and storage still occurs in each of the 16 bytes in sequence. Only the transfer protocol is changed.

During the Command phase (see next section), the FIFO action is disabled and data must be sent only after the RQM bit in the Main Status register has indicated that it is ready. Improper operation will result if command bytes are sent before the 82072 if ready. The 82072 does not ask for command parameters by generating interrupts or DMA requests. All command parameters are sent by polling the MSR.

As the 82072 enters the execution phase, it clears the FIFO of any data to ensure that invalid data is not written or read from the disk. During writes to the disk, if the host fails to respond in time, "00" will be written to the disk. During reads from the disk, the 82072 will not go into the Result phase until all data has been removed from the FIFO or a Terminal Count (TC) has been issued.

An overrun or underrun condition will terminate the transfer of data between the FIFO and the host. Writes to the disk will complete the current sector (using "00"s) and generate CRC. Reads will require the host to read all data bytes out of the FIFO so that the Result phase may begin. The proper error bit will be set in the Status register. A Terminal Count (TC) will always get the 82072 into the Result phase at the end of the current sector.

During the Result phase, the FIFO is disabled and the result bytes are read out one at a time.

During disk transfers between the FIFO and the host (or DMA controller), the FIFO must be serviced within a specified period after the appropriate indicator is set (INT, DRQ). Table 3 gives an example of the delays. The 1.5 μs delay is to convert the parallel data into serial MFM/(FM) data (with a clock speed of 24 MHz). Other data rate service delays are determined by:

$$\text{Threshold \#} \times \left[\frac{1}{\text{data rate}} \times 8\right] - 1.5\ \mu s = \text{DELAY}$$

Table 3. FIFO Service Delay

FIFO Threshold Examples	Maximum Delay to Servicing at 500 Kbps Data Rate
1 byte	1 × 16 μs − 1.5 μs = 14.5 μs
2 bytes	2 × 16 μs − 1.5 μs = 30.5 μs
8 bytes	8 × 16 μs − 1.5 μs = 126.5 μs
15 bytes	15 × 16 μs − 1.5 μs = 238.5 μs

FIFO Threshold Examples	Maximum Delay to Servicing at 250 Kbps Data Rate
1 byte	1 × 32 μs − 1.5 μs = 30.5 μs
2 byte	2 × 32 μs − 1.5 μs = 62.5 μs
8 byte	8 × 32 μs − 1.5 μs = 254.5 μs
15 byte	15 × 32 μs − 1.5 μs = 478.5 μs

The FIFO defaults to FIFO disabled. If the FIFO is enabled, DRQ stays active until the FIFO is emptied/filled. If the FIFO is disabled with the EFIFO bit in the CONFIGURE command, individual DRQ's are issued. Refer to the section on DMA transfers for more detail.

COMMAND EXECUTION PHASES

For simplicity, command handling in the 82072 can be divided into three phases: command, execution and result. Each phase is described in the following paragraphs.

Command Phase

After a RESET, the 82072 enters the Command phase and is ready to accept a command from host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the 82072 before the command phase is complete. (Please refer to the Command Description section). These bytes of data must occur in the order prescribed. For example:

SEEK Command

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	1	1	1	1	1st byte to the 82072
0	0	0	0	0	HDS	DS1	DS0	2nd byte to the 82072
< — — — — — — — — — — NCN — — — — — — — — — — >								3rd byte to the 82072

Before writing to the 82072, the host must examine the RQM and DIO bits of the Main Status Register. RQM, DIO must be equal to "1" and "0", respectively before command bytes may be written. RQM is set false by the 82072 after each write cycle until the received byte is processed. The 82072 asserts RQM again to request each parameter byte of the command, unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0", and the 82072 automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to retain compatibility with the 8272A, and to provide for the proper handling of the "invalid command" condition.

Execution Phase

All data transfers to or from the 82072 occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the SPECIFY command.

After RESET, the FIFO is disabled. Each data byte is transferred by an INT or DRQ depending on the DMA mode. The CONFIGURE command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the 82072 when service is requested from the host, and ranges from 1 to 16. The parameter FIFOTHR which the user programs is one less, and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request, for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

NON-DMA MODE, Transfers from the FIFO to the Host:

The INT pin and RQM bits in the Main Status Register are activated when the FIFO contains (16 – <threshold>) bytes, or the last bytes of a full sector transfer have been placed in the FIFO. The INT pin can be used for interrupt driven systems and RQM can be used for polled systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The 82072 will deactivate the INT pin and RQM bit when the FIFO becomes empty.

NON-DMA MODE, Transfers from the Host to the FIFO:

The INT pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The INT pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The 82072 will also deactivate the INT pin and RQM bit when TC goes active, indicating that no more data is required. The 82072 enters the results phase after the last byte is taken by the 82072 from the FIFO (i.e., FIFO empty condition).

DMA MODE, Transfers from the FIFO to the Host:

The 82072 activates the DRQ pin when the FIFO contains (16 – <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The 82072 will deactivate the DRQ pin when the FIFO becomes empty. DRQ goes inactive after $\overline{DACK}$ goes active for the last byte of a data transfer (or on the active edge of $\overline{RD}$, on the last byte, if no edge is present on $\overline{DACK}$). A data underrun may occur if DRQ is not removed in time to prevent an unwanted cycle. Refer to the section on DMA Transfers for more detail.

DMA MODE, Transfers from the Host to the FIFO:

The 82072 activates the DRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the $\overline{DACK}$ and $\overline{WR}$ pins, and placing data in the FIFO. DRQ remains active until the FIFO becomes full. DRQ is again set true when the FIFO has <threshold> bytes remaining in the FIFO. The 82072 will also deactivate the DRQ pin when TC becomes true, indicating that no more data is required. DRQ goes inactive after $\overline{DACK}$ goes active for the last byte of a data transfer (or on the active edge of $\overline{WR}$ on the last byte, if no edge is present on $\overline{DACK}$). A data overrun may occur if DRQ is not removed in time to prevent an unwanted cycle. Refer to the section on DMA Transfers for more detail.

The 82072 supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multisector transfer. If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the 82072 will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the 82072's FIFO, the internal sector count will be complete when the 82072 reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the 82072 to read the last 16 bytes from the FIFO. The host must tolerate this delay.

If before the execution of a command, the RDY pin is "0", the 82072 will set the corresponding bit in Status Register 0, and terminate the command phase. When an external TC signal is received, the external transfer is suspended, but the sector transfer is completed internally before the command phase is ended. The command phase is also terminated if the last sector on the track has been read or written, (as defined by the EOT parameter).

The 82072 activates INT to indicate the beginning of the result phase. The first reading of status from the 82072 resets the INT pin.

Result Phase

The generation of INT determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the 82072 before the result phase is complete. (Refer to the Command Description section). These bytes of data must be read out for another command to start.

RQM and DIO must be equal to "1" and "1", before the result bytes may be read from the FIFO. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared. This indicates that the 82072 is ready to accept the next command.

DATA RATE SELECT REGISTER (DSR)

The Data rate Select Register gives the user control over the read and write disk data. The user can select between an internal or external data separator, the data rate of the data separator and the delays for the write precompensation logic. The internal data separator requires no external control logic or analog components with its selectable data rates. SOFTWARE RESET and the POWERDOWN mode are invoked by setting the appropriate bit in this register.

When the processor writes into the DSR, the data is loaded after a delay to synchronize to an internal machine state. The processor must not perform successive writes into the DSR until this synchronization time (24 clock periods or 1 microsecond at 24 MHz) has elapsed. This register should be programmed before issuing a command that accesses the disk and uses values that this register controls. There is a 2 millisecond delay between writing the data rate select bits and having the PLL stabilize at the new frequency. This can be hidden by overlapping it in the

stepping and head load delays. There is no minimum delay between writing this register and accessing the FIFO and status registers.

A write to this register during data transfers will alter the contents of this register and the logic it controls. Data rate and precompensation values will change which may give undesirable results.

Changing the data rate also changes the timings of the drive control signals that are initialized with the SPECIFY command. To ensure that drive timings are not violated, the user should either choose values of drive timings such that the fastest data rate would not violate a drive timing specification or should follow a write to the data rate select bits with a new SPECIFY command. Refer to the SPECIFY command for more detail on these timings.

The Data rate Select Register (DSR) is a write only register. The functions of the DSR are indicated below:

SWR	PD	$\overline{\text{EPLL}}$	PRE-COMP			DRATESEL	
7	6	5	4	3	2	1	0

Bit 7—SWR; (SOFTWARE RESET)

When set to "1", enables software reset of the 82072. A software reset causes the hardware reset line to go active internally. Refer to Figure 5 for an illustration. This method ensures that software and hardware resets perform the same function. One function not reset is the DSR (since it contains the software reset bit). Since a hardware reset is being performed, the MSR will not be valid for up to 4 microseconds after the Software Reset is issued. The users software should wait that period before attempting to read the Main Status register. Software reset can also be cleared with a hardware reset.

In the case of software reset, the DSR retains the values loaded into it if DDRE is tied low. If DDRE is tied high, the precompensation and Data Rate Select bits will be reset to "00010". Upon hardware reset, the DSR will be configured based on DDRE setting. When DDRE is tied high, the DSR is configured as follows upon power up and reset:

SWR	PD	$\overline{\text{EPLL}}$	PRE-COMP			DRATESEL	
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0

Default values: 250 Kbit/sec., Internal data separator, Precompensation = 125 ns.

When DDRE is tied low, the DSR retains the current data rate and precompensation values:

SWR	PD	$\overline{\text{EPLL}}$	PRE-COMP			DRATESEL	
7	6	5	4	3	2	1	0
0	0	0	X	X	X	X	X

Default values: X = current value, Internal data separator.

Bit 6—PD; (POWER DOWN)

When set to "1", the 82072 goes into its POWER DOWN mode. A SOFTWARE RESET is performed and held when entering POWER DOWN to ensure that no disk control pins are in the active state. The powerdown mode deactivates the internal clocks and shuts off the oscillator. Only writes to the DSR are allowed during powerdown and ALL input signals must be held in a valid state (either D.C. 1 or 0). The only exceptions are the data bus may be floated and an external crystal, which may remain running. There will be no increase in the ICC specification. To exit the Power down mode, either a hardware or software reset must be given. Once reset is given, there is a delay of 1 ms for the oscillator to stabilize at the correct frequency.

The 82072 preserves the contents of the PCN register during POWERDOWN. However, all status registers are cleared. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the SENSE INTERRUPT STATUS command.

Bit 5—EPLL; (Enable PLL)

When set to "0", the internal PLL data separator supplies the data window input and the DW/DDRE pin operates in DDRE mode. The data rate of the internal PLL is determined by the DRATESEL bits. When set to "1", the internal data separator is disconnected from the serial interface controller and an external data separator is required to supply the DW signal. Refer to the section on the internal data separator for more detail.

Bits 2–4—PRECOMP; (Pre-compensation)

The write precompensation circuitry adjusts the write data pulse before it is sent to the drive on the WRDATA pin. A programmed compensation interval is added to or subtracted from the normal write pulse timing as a function of the data pattern. The CONFIGURE command is used to specify the track number that precompensation starts upon. If a CONFIGURE command is not issued, the 82072 defaults to beginning pre-compensation on Track 0.

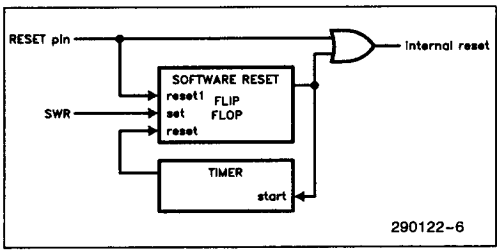


Figure 5. Reset Block Diagram

Table 5. Pre-Compensation Delays

PRECOMP 432	Pre-Compensation Delay
111	0.00 ns–DISABLED
001	41.67 ns
010	83.34 ns
011	125.00 ns
100	166.67 ns
101	208.33 ns
110	250.00 ns
000	DEFAULT

If the Data rate Select Register (DSR) is programmed with bits 2–4 set to zeroes, a default precompensation value is automatically chosen depending upon the data rate select bits (bits 0 and 1). The default values corresponding to the data rate select values are illustrated in Table 5A.

Table 5A. Default Pre-Compensation Delays

Data Rate	Pre-Compensation Delays
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

Bits 0, 1—DRATESEL; (Data Rate Select)

Programs both the read and write data rates. For single density (FM mode), data rates are one half the values stated for the double density (MFM) mode. MFM or FM selection is made in the disk read and write commands.

Table 4. Data Rates

DRATESEL 1	DRATESEL 0	DATA RATE MFM	DATA RATE FM
1	1	Illegal	Illegal
0	0	500 Kbps	250 Kbps
0	1	300 Kbps	150 Kbps
1	0	250 Kbps	125 Kbps

WRITE CLOCK

The basic "core" of the 8272A was carried over to the 82072 virtually unchanged. To keep the flexibility of the 8272A, where the user could vary data rates by changing the frequency on the WRCLK pin, and to minimize the external logic, a prescaler for the internal WRCLK was added. The prescaler divides down the 24 MHz clock to rates that are equivalent to those used with the 8272A. The user changes the prescaler value with the data rate selection bits in the DATA RATE SELECT register.

POLLING OF DRIVES

The 82072 defaults to polling enabled. Polling can be disabled by issuing a CONFIGURE command. When enabled, the 82072 polls the drives and looks for a change in the state of the RDY pin. Each of the drives is selected for a period of time and its RDY pin sampled. After a delay, the next drive is selected. This sequence occurs whenever the 82072 is waiting for a command or during SEEKs and RECALIBRATE, (but not IMPLIED SEEKs). The drives are assumed to be not ready after RESET and a "ready" value for each drive is saved in an internal register. An interrupt will be issued when a drive signals that it changed state from not ready to ready. This interrupt must be followed with a SENSE INTERRUPT STATUS command from the host. Each time that the drive changes its state from not ready to ready, an interrupt will again be issued.

The length of time that a drive is selected is dependent upon the selected data rate. At 500 Kbps, drives 0–2 are selected for approximately 40 μs, and drive 3 to about 880 μs. At 250 Kbps, the selected period is doubled for all drives. This period continues to scale with the data rate selection. The amount of time that the 82072 actually samples the RDY pin is about 1 microsecond after the drive select changes at 500 Kbps and also scales with the data rate. This value is equal for all drives. The remaining time the drive is selected, changes on RDY will not be sampled.

NOTE:
Polling is disabled when an Implied Seek is in progress.

TERMINAL COUNT (TC)

TC completes the current disk data transfer and then puts the 82072 into the result phase.

DRQ or RQM/INT in the Non-DMA mode will go inactive immediately after TC is received. There will be no more requests for data transfers. In a write command, all remaining bytes in the FIFO are read out by the 82072. The remaining space in the disk sector will be filled with "00"s. For read's, the remaining data bytes are "dumped" internally and CRC is checked. An overrun/underrun error will not be reported in the result phase. The FIFO will be reset upon entering the result phase. This ensures that any remaining data bytes sent by the host do not interfere with the result bytes.

It should be noted that if TC is asserted without an accompanying $\overline{DACK}$ or $\overline{CS}$ and $\overline{RD}/\overline{WR}$ (FIFO transfer), then DRQ remains high until the pending FIFO transaction is performed. However, the receipt of TC is sufficient to internally inhibit further data requests.

The 82072 supports terminal count implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfer, the EOT parameter can define the last sector to be transferred in a single or multisector transfer. If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector and the 82072 will complete the transfer in the same way as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

It is recommended that the TC be issued with the last byte transferred, or shortly thereafter. The user must issue a TC before GPL byte times of the request for the last byte of the sector, or the 82072 will continue on to the next sector. This may cause an error condition such as reading past end-of-track, underrun/overrun of the FIFO, or a sector not found. Terminal count will always get the 82072 out of the execution phase which would be caused by the host failing to perform the correct action.

DMA TRANSFERS

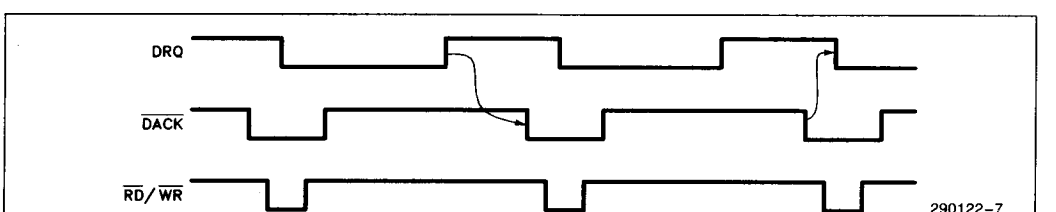
DMA transfers are initiated by the 82072 when it activates its DRQ (DMA Request) pin. When ready, the DMA controller responds by activating $\overline{DACK}$ (DMA Acknowledge). If the DMA transfer mode is selected in the 82072 (with the SPECIFY command), DRQ must be used as the RQM bit signal since RQM is not activated. $\overline{DACK}$ or CS = 0 and A0 = 1 can be used to respond to the request.

If the FIFO is enabled, DRQ will go active for a transfer and stay active until the FIFO is filled or cleared (write and read respectively).

If the FIFO is disabled (default value) by setting the EFIFO bit in the CONFIGURE command, each byte to be transferred will request a cycle. Figure 6 is an example of the handshaking that occurs.

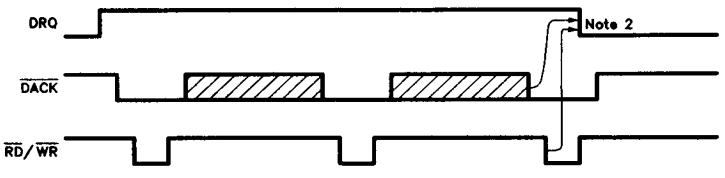
The 82072 can be given pulsed $\overline{DACK}$'s (which is compatible with the iAPX186 and most two cycle DMA controllers) or $\overline{DACK}$'s that stay active until the transfer is complete (compatible with the Intel 8237A controller). A pulsed $\overline{DACK}$ provides more time for the DMA controller to determine if DRQ should be removed (since $\overline{DACK}$ goes active before RD). If $\overline{DACK}$ is not pulsed, then the active going edge of RD is used for this decision. The edge of RD may be too late for DRQ to be removed and prevent an unwanted DMA cycle.

There is a small delay after $\overline{DACK}$ (or RD) goes active at the 82072 before DRQ is removed. This may not satisfy the DMA controller specification ($\overline{DACK}$ active to DRQ inactive) to prevent an unwanted DMA cycle. It is the users responsibility to ensure that an unwanted cycle does not happen due to DRQ not going inactive quickly enough. It may be



NOTE:
The falling edge of $\overline{DACK}$ asynchronously removes DRQ.

Figure 6. Disabled FIFO DMA Cycles



NOTES:
1. DACK can be either active the entire period or can be active for each cycle.
2. Either edge will remove DRQ, but DACK provides more setup time for the 82072 and the DMA controller.

Figure 7. DMA Transfers with the FIFO Enabled

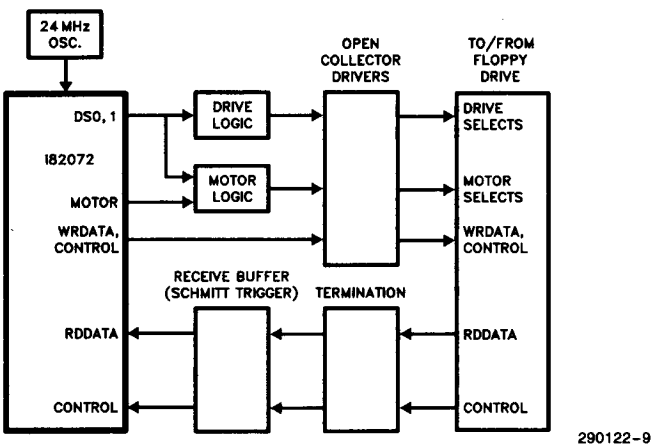


Figure 8. Drive Interface Block Diagram

necessary for the design to generate a pulsed DACK, one that is earlier than the one supplied by the DMA controller or add wait states.

Note that if the DMA controller (i.e., 8237A) is programmed to function in verify mode, a pseudo read is performed by the 82072 based only on DACK. This mode is only available when the 82072 has been configured into byte mode and is programmed to do a read operation.

DRIVE INTERFACE

Figure 8 is a block diagram of the floppy drive interface for the 82072. The external logic needed are high current buffers to drive the cable, termination and MOTOR and drive select generation.

When a read operation begins, the sync detect logic samples the read data stream until it finds a valid sync field, which is a pattern of eight contiguous zero bit cells. This is found with an internal one-shot. It assumes that this is a synchronization field (Refer to the FORMAT command for detail) and will switch the VCO from the reference clock to the data stream after waiting the delay specified in the GAP parameter of the READ and WRITE commands. The sync logic then switches the READ DATA stream to the input of the data separator. The clock that the PLL is synchronized to is forced to be in phase with the read data as the switch over occurs. The PLL of the data separator starts with almost zero phase error, which greatly reduces the capture time. Once VCO is activated and the PLL has locked onto the serial data, it is searched for an ID address mark. If the first non-sync data is not an ID address mark, the VCO line is deactivated and the search for a sync.

field begins again with the data separator waiting for the one-shot to find another sync. field. If the address mark was good, the ID field is examined for the correct parameters and CRC is checked. When the 82072 is not looking at the disk data, it remains synchronized to the programmed data rate. This method ensures that the PLL does not lock onto harmonics. It also allows a faster lock-up time when disk data is fed into the PLL.

DATA SEPARATOR

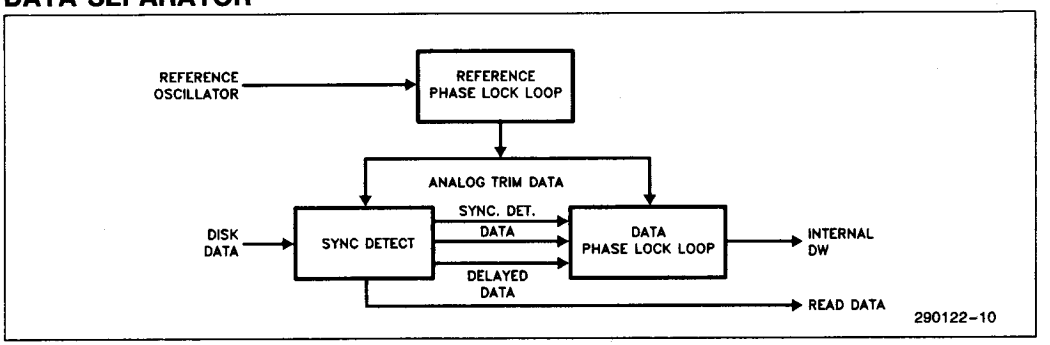


Figure 9. Data Separator Block Diagram

The function of the data separator is to lock onto the incoming serial read data. When lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called Data Window, is used to internally sample the serial data. One state of Data Window is used to sample the data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

To support reliable disk reads the data separator must track fluctuations in the disk data frequency. Frequency errors primarily arise from two sources: drive rotation speed variation and instantaneous speed variation (ISV). A second condition, and one that opposes the ability to track frequency shifts is the response to bit jitter.

The internal data separator consists of two analog phase lock loops (PLLs) as shown in Figure 9. The two PLLs are referred to as the reference PLL and the data PLL. The reference PLL (the master PLL) is used to bias the data PLL (the slave PLL). The reference PLL adjusts the data PLL's operating point as a function of process, junction temperature and supply voltage. Using this architecture it was possible to eliminate the need for external trim components.

Figure 10 shows the data PLL. The reference PLL has control over the loop gain by its influence on the

PHASE LOCK LOOP OVERVIEW

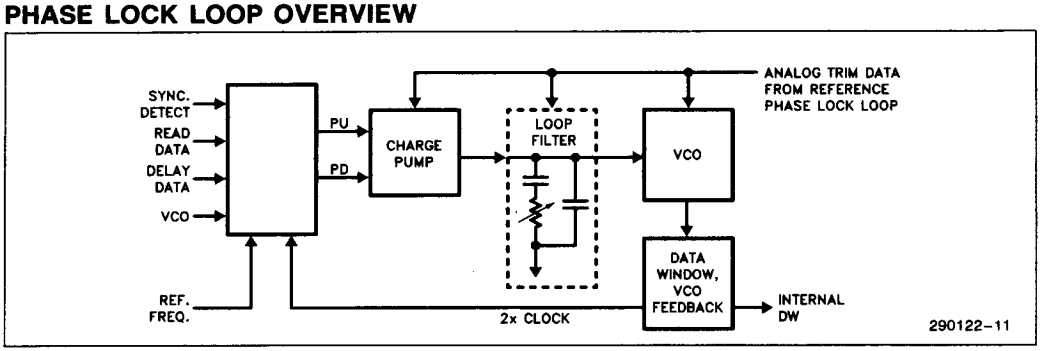


Figure 10. Data PLL

charge pump and the VCO. In addition the reference PLL controls the loop filter time constant. As a result the closed loop transfer function of the data PLL is controlled, and immune, to the first order, to environmental factors, and process variation.

Systems of this type are often very sensitive to noise. In the design of this data separator many steps were taken to avoid noise sensitivity problems. The analog section of the chip has a separate VSS pin (AVSS) which should be connected externally to a noise free ground. This provides a clean basis for VSS referenced signals. In addition many analog circuit features were employed to make the overall system as insensitive to noise as possible. To insure reliable operation the designer should take steps to provide a noise free operating environment for the chip.

LOCKTIME (tLOCK)

The lock, or settling time of the data PLL is designed to be 64 bit times. This corresponds to 4 sync bytes in the FM mode and 8 sync bytes in the MFM mode. This value assumes that the sync field jitter is 5% the bit cell or less. This level of jitter should be easily achieved for a constant bit pattern, since intersymbol interference should be equal, thus nearly eliminating random bit shifting.

CAPTURE RANGE (tRANGE)

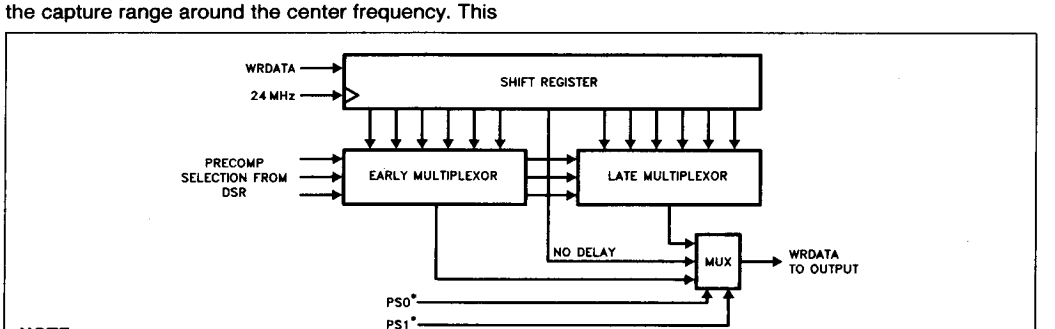
The 82072 data separator is designed to lock onto RDDATA with a maximum frequency error of approximately ±5.5%. The graphs in Figures 17 and 18 in the Data Separator Characteristics Section illustrate the capture range around the center frequency. This value is made up of two components: drive motor speed error and ISV. Frequency is a factor which may determine the maximum level of the ISV component. In general, as frequency increases the allowed magnitude of the ISV component will decrease. The designer has a certain level of flexibility in the composition of this sum, however the total must never exceed ±5.5%. In order to insure the reliability of dual drive systems, designers should require drives with a motor speed variation of ±2.75%, resulting in a worse case of ±5.5% when media is switched between drives.

WRITE PRECOMPENSATION

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. The shifting of bits is a known phenomena of magnetic media and is dependent upon the disk media AND the floppy drive.

The 82072 monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late (or not at all) relative to the surrounding bits. Figure 11 is a block diagram of the internal circuit.

The top block is a 13 bit shift register with the no delay tap being in the center. This allows 6 levels of early and late shifting with respect to nominal. The shift register is clocked at the main clock rate (24 MHz). The output is fed into 2 multiplexors—one for early and one for late. A final stage of multiplexors combines the early, late and normal data stream back into one which is the WRDATA output.



NOTE:
PS0, 1 are 8272A control signals but are not available as outputs on the 82072.

Figure 11. Precompensation Block Diagram

COMMAND SET

Table 5B. 82072 Command Set

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
READ DATA										
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and main-system
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				
READ DELETED DATA										
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and main-system
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				
WRITE DATA										
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the main-system and FDD
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				

Table 5B. 82072 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
WRITE DELETED DATA										
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and main-system
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				
READ TRACK										
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and main-system. FDC reads all of cylinders contents from index hole to EOT
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				
READ ID										
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Disk status after the Command has completed.
	R					R				
	R					N				

Table 5B. 82072 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
FORMAT TRACK										
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	———			N		———			Bytes/Sector
	W	———			SC		———			Sectors/Cylinder
	W	———			GPL		———			Gap 3
	W	———			D		———			Filler Byte
For Each Sector Repeat:	W	———			C		———			Input Sector Parameters
	W	———			H		———			
	W	———			R		———			
	W	———			N		———			
Execution										FDC formats an entire cylinder
Result	R	———			ST 0		———			Status information after Command execution
	R	———			ST 1		———			
	R	———			ST 2		———			
	R	———			Undefined		———			
	R	———			Undefined		———			
	R	———			Undefined		———			
	R	———			Undefined		———			
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	———			ST 0		———			Status information at the end of each seek operation about the FDC
	R	———			PCN		———			
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	——— SRT ——— > < ——— HUT ———								
	W	——— HLT ——— > ND								
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	MOT	0	0	0	0	HDS	DS1	DS0	
Result	R	———			ST 3		———			Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	———			NCN		———			
Execution										Head is positioned over proper Cylinder on Diskette
CONFIGURE										
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	HSDA < ——— MOFF ——— <					> ——— MON ——— >			
	W	0	EIS	EFIFO	POLL		< ——— FIFOTHR ——— >			
	W	< ——— PRETRK ———					——— >			
MOTOR ON/OFF										
Command	W	On/Off	DS1	DS0	0	1	0	1	1	Command Code
RELATIVE SEEK										
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	———			RCN		———			

Table 5B. 82072 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
DUMPREG										
Command	W	0	0	0	0	1	1	1	0	*Note
Execution										Registers placed in FIFO
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	< SRT >				< HUT >				
	R	< HLT >							ND	
	R	< SC/EOT >								
	R	HSDA < MOFF >				< MON >				See Note
	R	0	EIS	EFIFO	POLL	< FIFOTHR >				
	R	< PRETRK >								
INVALID										
Command	W	Invalid Codes								Invalid Command Codes (NoOp — FDC goes into Standby State)
Result	R	ST 0								ST 0 = 80 (16)

SC is returned if the last command that was issued was the FORMAT command. EOT is returned if the last command was a READ or WRITE.

NOTES:
1. Symbols used in this table are described below.
2. A_0 = 1 for all operations.

PARAMETER ABBREVIATIONS:

Symbol	Description
C	Cylinder address. The currently selected cylinder address, 0 to 255.
D	Data pattern. The pattern to be written in each sector data field during formatting.
DS0, DS1	Disk Drive Select.

DS1	DS0	
0	0	drive 0
0	1	drive 1
1	0	drive 2
1	1	drive 3

Symbol	Description
DTL	Special sector size. By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
EOT	End of track. The final sector number of the current track.
GPL	Gap length. The gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head address. Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head load time. The time interval that 82072 waits after loading the head and before initiating a read or write operation. Refer to the SPECIFY command for actual delays.
HUT	Head unload time. The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the SPECIFY command for actual delays.
MFM	MFM/FM mode selector. A one selects the double density (MFM) mode. A zero selects single density (FM) mode.
MT	Multi-track selector. When set, this flag selects the multi-track operating mode. In this mode, the 82072 treats a complete cylinder, under head 0 and 1, as a single track. The 82072 operates as if this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector

Symbol	Description
	under head 1 when the 82072 finishes operating on the last sector under head 0.
N	Sector size code. This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the users responsibility to not select combinations that are not possible with the drive.

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

Symbol	Description
NCN	New cylinder number. The desired cylinder number.
ND	Non-DMA mode flag. When set to 1, indicates that the 82072 is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the 82072 operates in DMA mode, interfacing to a DMA controller by means of the DRQ and DACK# signals.
PCN	Present cylinder number. The current position of the head at the completion of SENSE INTERRUPT STATUS command.
R	Sector address. The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
SC	Number of sectors per track. The number of sectors per track to be initialized by the FORMAT command.
SK	Skip flag. When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of READ DATA. If READ DELETED is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step rate interval. The time interval between step pulses issued by the 82072. Programmable from 1.0 to 16.0 milliseconds, in increments of 1.0 ms at the 500 Kbps data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status register 0–3. Registers within the 82072 that store status information after a command has been executed. This status information is available to the host during the result phase after command execution.

Commands can be written whenever the 82072 is in the command phase. The command set falls into two categories as is shown in Table 6. The encoding of the bits used in this description can be found in the Parameter Abbreviation section which follows this section.

Each command has a unique set of parameters that are needed and that are returned as status. The 82072 checks to see that the first byte received while in the command phase is a valid command. If valid, there will be no change in the status bits in the MSR. If the value was not a valid command, an interrupt is issued. The user would issue the SENSE INTERRUPT STATUS command which would return an invalid command error condition.

DATA TRANSFER COMMANDS

The READ DATA, READ DELETED DATA, WRITE DATA, WRITE DELETED DATA and READ TRACK require and return the same parameter and status bytes respectively. The only differences being the coding of bits 0–4 in the first byte sent to the 82072.

Table 6. Command Summary

Data Transfer	Control	
Read Data	Recalibrate	Configure *
Read Deleted Data	Sense Interrupt Status	Motor On/Off *
Write Data	Specify	Relative Seek*
Write Deleted Data	Sense Drive Status	Dumpreg *
Read Track	Seek	
Format Track	Read ID	

***NOTE:**
These commands are not present in the 8272A.

Table 7. Data Transfer Command Summary

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MFM	SK	0	X	X	X	X	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	———	———	———	———	C	———	———	———	
	W	———	———	———	———	H	———	———	———	
	W	———	———	———	———	R	———	———	———	
	W	———	———	———	———	N	———	———	———	
	W	———	———	———	———	EOT	———	———	———	
	W	———	———	———	———	GPL	———	———	———	
	W	———	———	———	———	DTL	———	———	———	
Execution										Data Transfer Occurs.
Result	R	———	———	———	———	ST0	———	———	———	Status After
	R	———	———	———	———	ST1	———	———	———	Command Has
	R	———	———	———	———	ST2	———	———	———	Completed.
	R	———	———	———	———	C	———	———	———	Disk Status
	R	———	———	———	———	H	———	———	———	After The
	R	———	———	———	———	R	———	———	———	Command Has
	R	———	———	———	———	N	———	———	———	Completed.

Table 8. Command Encoding

Command	D3	D2	D1	D0
Read Data	0	1	1	0
Read Deleted Data	1	1	0	0
Write Data	0	1	0	1
Write Deleted Data	1	0	0	1
Read Track	0	0	1	0

IMPLIED SEEK FOR READ AND WRITE COMMANDS

The 82072 will execute an implied seek for any disk transfer command that specifies the cylinder number. The implied seek execution is transparent to the user. This means that the user would issue a READ DATA command, send all of the parameter bytes, see step pulses issued and start reading data.

After the parameter bytes are received, a comparison is made between PCN and C. If C does not equal PCN and the Implied Seek bit in the CONFIGURE command was set, then a SEEK command is issued. This would be indicated by the DRIVE BUSY bits in the Main Status Register being set. If the stepping completes successfully, DRIVE BUSY in the MSR will go inactive and then the disk transfer command starts. If the SEEK failed, the status bytes of the command are sent to the FIFO. ST0 contains the cause of the error and C would contain the cylinder number on which the SEEK failed.

READ DATA COMMAND

A set of nine (9) bytes is required to place the 82072 into the Read Data Mode. After the READ DATA command has been issued, the 82072 loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the SPECIFY command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the 82072 reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one, and the data from the next logical sector is read and ouput via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the 82072 stops sending data, but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector terminate the READ DATA Command.

N determines the number of bytes per sector (See Table 8A Below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the 82072 transfers the specified number of bytes to the host. For reads, it continues to read the entire 128 byte sector and checks for CRC errors. For writes it completes the 128 byte sector by filling in zeroes. If N is not set to 00 Hex, DTL should be set to FF Hex, and has no impact on the number of bytes transferred.

Table 8A. Sector Sizes

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the 82072 depends upon MT (multi-track) and N (Number of bytes/sector).

MT	N	Max. Transfer Capacity	Final Sector Read from Disk
0	1	256 × 26 = 6,656	26 at side 0 or 1
1	1	256 × 52 = 13,312	26 at side 1
0	2	512 × 15 = 7,680	15 at side 0 or 1
1	2	512 × 30 = 15,360	15 at side 1
0	3	1024 × 8 = 8,192	8 at side 0 or 1
1	3	1024 × 16 = 16,384	16 at side 1

The Multi-Track function (MT) allows the 82072 to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at the last sector of the same track at Side 1.

At the completion of the READ DATA Command, the head is not unloaded until after the Head Unload Time Interval (specified in the SPECIFY command) has elapsed. If the host issues another command before the head unloads then the head settling time may be saved between subsequent reads.

If the 82072 detects a pulse on the IDX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the 82072 sets the IC code in Status Register 0 to "01" (Abnormal termination), and sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the READ DATA Command.

After reading the ID and Data Fields in each sector, the 82072 checks the CRC bytes. If a CRC error occurs in the ID or data field, the 82072 sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the READ DATA Command.

Table 8B below describes the affect of the SK bit on the READ DATA command execution and results.

Table 8B. Skip Bit vs. READ DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	No	Normal Termination.
0	Deleted Data	Yes	Yes	Address Not Incremented. Next Sector Not Searched For.
1	Normal Data	Yes	No	Normal Termination.
1	Deleted Data	No	Yes	Normal Termination Sector Not Read ("Skipped").

Except where noted in Table 8B, the C or R value of the sector address is automatically incremented (see Table 8D).

WRITE DATA

After the WRITE DATA command has been issued, the 82072 loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the SPECIFY command), and begins reading ID Fields. When the sector address read from the diskette matches the sector address specified in the command, the 82072 reads the data from the host via the FIFO, and writes it to the sector's data field.

After writing data into the current sector, the 82072 computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the 82072 continues writing to the next data field. The 82072 continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros.

The 82072 reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID Fields, it sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the WRITE DATA command.

The WRITE DATA command operates in much the same manner as the READ DATA command. The following items are the same. Please refer to the READ DATA Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command.
- Definition of DTL when N = 0 and when N does not = 0.

READ DELETED DATA

This command is the same as the READ DATA command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 8C describes the affect of the SK bit on the READ DELETED DATA command execution and results.

Table 8C. Skip Bit vs READ DELETED DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	Yes	Address Not Incremented. Next Sector Not Searched For.
0	Deleted Data	Yes	No	Normal Termination.
1	Normal Data	No	Yes	Normal Termination Sector Not Read ("Skipped").
1	Deleted Data	Yes	No	Normal Termination.

Except where noted in Table 8C above, the C or R value of the sector address is automatically incremented (See Table 8D).

WRITE DELETED DATA

This command is almost the same as the WRITE DATA command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

READ TRACK

This command is similar to the READ DATA command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the IDX pin, the 82072 starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the 82072 finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The 82072 compares the ID information read from each sector with the specified value in the command, and sets the ND flag of Status Register 1 to a "1" if there is no comparison. Multi-track or skip operations are not allowed with this command. The SK bit should always be set to "0".

This command terminates when the EOT specified number of sectors have been read. If the 82072 does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, then it sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

REGISTER INFORMATION FOR HOST TERMINATION

If the host terminates a read or write operation in the 82072, then the ID information in the result phase is dependent upon the state of the MT bit and EOT byte.

Table 8D. Result Phase Table

MT	Head	Final Sector Transferred to Host	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
1	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	LSB	01	NC

NC: no change, the same value as the one at the beginning of command execution.
LSB: least significant bit, the LSB of H is complemented.

FORMAT COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	MFM	0	0	1	1	0	1	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	—	—	—	—	N	—	—	—	
	W	—	—	—	—	SC	—	—	—	
	W	—	—	—	—	GPL	—	—	—	
	W	—	—	—	—	D	—	—	—	
For Each	W	—	—	—	—	C	—	—	—	Input Sector
Sector Repeat:	W	—	—	—	—	H	—	—	—	Parameter
	W	—	—	—	—	R	—	—	—	
	W	—	—	—	—	N	—	—	—	
Execution										Data Transfer Occurs
Result										
	R	—	—	—	—	ST0	—	—	—	Status After
	R	—	—	—	—	ST1	—	—	—	Command Has
	R	—	—	—	—	ST2	—	—	—	Completed.
	R	—	—	—	—	Undefined	—	—	—	
	R	—	—	—	—	Undefined	—	—	—	
	R	—	—	—	—	Undefined	—	—	—	
	R	—	—	—	—	Undefined	—	—	—	

The FORMAT command allows an entire track to be formatted. After a pulse from the IDX pin is detected, the 82072 starts writing data on the disk including Gaps, Address Marks, ID Fields and Data Fields, per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID Field for each sector is supplied by the host; that is, four data bytes per sector are needed by the 82072 for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the 82072 for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector

is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the 82072 encounters a pulse on the IDX pin again and it terminates the command.

Table 9 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

Table 9. Typical Values for Formatting

		Sector Size	N	SC	GPL1	GPL2
8″ Drives	FM	128	0	1A	07	1B
		256	1	0F	0E	2A
		512	2	08	1B	3A
		1024	3	04	47	8A
		2048	4	02	C8	FF
		4096	5	01	C8	FF
	MFM	256	1	1A	0E	36
		512	2	0F	1B	54
		1024	3	08	35	74
		2048	4	04	99	FF
		4096	5	02	C8	FF
5.25″ Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5″ Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in read and write commands to avoid splice point between data field and ID field of contiguous sections.
GPL2 = suggested GPL value in FORMAT TRACK command.

NOTE:
All values are in Hex.

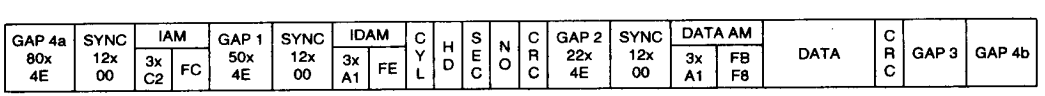


Figure 12. System 34 Format Double Density

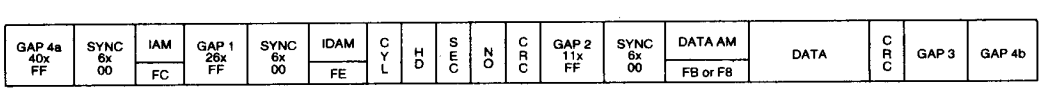


Figure 13. System 3740 Format Single Density

CONTROL COMMANDS

Each of the control commands has a unique set of parameters that are sent and returned. Control commands differ in that they do not have a data transfer in the execution phase.

CONTROL COMMANDS WITH INTERRUPTS

READ ID COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	MFM	0	0	1	0	1	0	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										1ST ID Field Located.
Result	R	———	———	———	———	ST0	———	———	———	Status After
	R	———	———	———	———	ST1	———	———	———	Command Has
	R	———	———	———	———	ST2	———	———	———	Completed.
	R	———	———	———	———	C	———	———	———	Disk Status
	R	———	———	———	———	H	———	———	———	After The
	R	———	———	———	———	R	———	———	———	Command Has
	R	———	———	———	———	N	———	———	———	Completed.

The READ ID command is used to find the present position of the recording heads. The 82072 stores the values from the first ID Field it is able to read into its registers. If the 82072 does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, it then sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the SENSE INTERRUPT STATUS command. Otherwise, valuable interrupt status information will be lost.

RECALIBRATE COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	0	1	1	1	Command Code
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head Retracts To Track 0.
										Interrupt

This command causes the read/write head within the FDD to retract to the track 0 position. The 82072 clears the contents of the PCN counter, and checks the status of the TRK0 pin from the FDD. As long as the TRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the TRK0 pin goes high, the SE bit in Status Register 0 is set to "1", and the command is terminated. If the TRK0 pin is still low after 255 step pulses have been issued, the 82072 sets the SE and the EC bits of Status Register 0 to "1", and terminates the command. Disks capable of handling more than 256 tracks per side may require more than one RECALIBRATE command to return the head back to physical Track 0.

The RECALIBRATE command does not have a result phase. SENSE INTERRUPT STATUS command must be issued after the RECALIBRATE command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the 82072 is in the BUSY state, but during the execution phase it is in a NON BUSY state. At this time another RECALIBRATE command may be issued, and in this manner, parallel RECALIBRATE operations may be done on up to 4 drives at once.

Upon power up, the software must issue a RECALIBRATE command to properly initialize all drives and the controller.

SEEK COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	1	1	1	1	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	———— NCN ————								
Execution										Head is Moved to Specified Track.

The read/write head within the FDD is moved from track to track under the control of the SEEK Command. The 82072 compares the PCN which is the current head position with the NCN and performs the following operation if there is a difference:

—PCN < NCN: Direction signal to FDD set to "1" (step in), and issues step pulses.

—PCN > NCN: Direction signal to FDD set to "0" (step out), and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN, then the SE bit in Status Register 0 is set to "1", and the command is terminated.

During the command phase of the seek or recalibrate operation, the 82072 is in the BUSY state, but during the execution phase it is in the NON BUSY state. At this time another SEEK or RECALIBRATE command may be issued, and in this manner, parallel seek operations may be done on up to 4 drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR bit in Status Register 0 is set to "1", and the command is terminated.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1) SEEK command; Step to the proper track
2) SENSE INTERRUPT STATUS command; Terminate the Seek command
3) READ ID. Verify head is on proper track
4) Issue READ/WRITE command.

The SEEK command does not have a result phase. Therefore, it is highly recommended that the SENSE INTERRUPT STATUS Command after the SEEK command be issued to effectively terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return a "0". When exiting POWERDOWN mode, the 82072 clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the SENSE INTERRUPT STATUS command.

CONTROL COMMANDS WITHOUT INTERRUPTS

These commands have no execution phase and do not generate an interrupt upon completion. Their primary use is to follow one of the commands that do not have an execution phase, although they may be issued whenever the 82072 is in the command phase.

SENSE INTERRUPT STATUS COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	1	0	0	0	Command Code
Result	R	———— ST0 ————								
	R	———— PCN ————								

An interrupt signal on INT pin is generated by the 82072 for one of the following reasons:

1. Upon entering the Result Phase of:
   a. READ DATA Command
   b. READ TRACK Command
   c. READ ID Command
   d. READ DELETED DATA Command
   e. WRITE DATA Command
   f. FORMAT TRACK Command
   g. WRITE DELETED DATA Command
2. RDY pin changes state
3. End of SEEK, RELATIVE SEEK or RECALIBRATE Command
4. 82072 requires a data transfer during the execution phase in the non-DMA Mode

The SENSE INTERRUPT STATUS command resets the interrupt signal and via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

Table 10. Interrupt Identification

SE	IC	Interrupt Due To
0	11	RDY pin changes state
1	00	Normal Termination of SEEK or RECALIBRATE command
1	01	Abnormal Termination of SEEK or RECALIBRATE command

The SEEK, RELATIVE SEEK and the RECALIBRATE commands have no result phase. SENSE INTERRUPT STATUS command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a SENSE INTERRUPT STATUS is not issued, the drive, will continue to be BUSY and may effect the operation of the next command.

SENSE DRIVE STATUS

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	0	1	0	0	Command Code
	W	MOT	0	0	0	0	HD5	DSI	DS0	
Result	R	———	———	———	———	ST3	———	———	———	

SENSE DRIVE STATUS obtains drive status information. It has no execution phase and goes directly to the result phase from the command phase. STATUS REGISTER 3 contains the drive status information. If Bit 7 of the second command byte is set (MOT), there is no delay before the drive is accessed for status information. If Bit 7 is not set, and the motor is off or a drive different from the current drive is selected. The 82072 waits the motor ON/OFF delay period before accessing the drive. In either case, the motor is always turned on before the status information is accessed.

SPECIFY COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	0	0	1	1	Command Code
	W	<———	SRT	———>		<———	HUT	———>		
	W	<———	———	———	HLT	———	———	———	ND	
Execution										Values Placed Into Regs.

The SPECIFY command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between the Head Load signal goes high and the read, write operation starts. The values change with the data rate speed selection and are documented in Table 11. The values are the same for MFM and FM.

Table 11. Drive Control Delays (ms)

	HUT			SRT		
	500K	300K	250K	500K	300K	250K
1	256	426	512	16	26.7	32
2	16	26.7	32	15	25	30
..	..	..	..	..	..	..
E	224	373	448	2	3.33	4
F	240	400	480	1	1.67	2

	HLT		
	500K	300K	250K
00	256	426	512
01	2	3.3	4
02	4	6.7	8
..	..	..	.
7F	252	420	504
7F	254	423	508

The choice of DMA or NON-DMA operations is made by the ND bit. When this bit is "1", the NON-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signalled by the DRQ pin. Non-DMA mode uses the RQM bit and the INT pin to signal data transfers.

NEW CONTROL COMMANDS

CONFIGURE COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	1	0	0	1	1	Configuration Information
	W	HSDA	<— — MOFF — —>			<— — — MON — — >				
	W	0	EIS	EFIFO	POLL	<— — FIFOTHR— —>				
	W	<— — — — — — — — — PRETRK — — — — — — — — —>								

Issued to select the special features of the 82072. A CONFIGURE command need not be issued if the default values of the 82072 meet the system requirements.

CONFIGURE DEFAULT VALUES:

EIS —No Implied Seeks
EFIFO —FIFO Disabled
POLL —Polling Enabled
FIFOTHR —FIFO Threshold Set to 1 Byte
PRETRK —Pre-Compensation Set to Track 0
HSDA —Disabled
MOFF —Set to Motor Off Delay of 5.2 Seconds
MON —Set to 0.0 Second

EIS—Enable implied seek. When set to "1", the 82072 will perform a SEEK operation before executing a read or write command. Defaults to no implied seek.

EFIFO—A "1" puts the FIFO into the 8272A compatible mode where the FIFO is disabled. This means data transfers are asked for on a byte by byte basis. Defaults to "1", FIFO disabled. The threshold defaults to one.

POLL—Disable polling of the drives. Defaults to "0", polling enabled. When enabled, each of the drives is selected for a period of time, and its RDY pin sampled. After a delay, the next drive is selected. This sequence occurs whenever the 82072 is in the idle state. An interrupt is generated if the 82072 detects a change in the drive RDY signal. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR—The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. 00 selects one byte, 0F select 16 bytes.

PRETRK—Pre-compensation start track number. Programmable from track 0 to 255. Defaults to track 0. 00 selects track 0, FF selects track 255.

HSDA—High Speed Disk Adjust causes the motor on/off delays to be doubled. This is necessary for disks that rotate at high rates (i.e., 600 RPM vs 300 RPM). Defaults to a "0" which is disabled.

MOFF—Programs the number of index pulses to be counted before the MOTOR pin is deactivated (if high). All 82072 commands restart the motor off timer upon their completion. The MOFF bits increment the count value by 4. The HSDA bit doubles that value for disks that spin extremely fast. This chart is simplified to illustrate the count delays. All combinations are legal and no checking is done by the 82072.

The motor off delay is ignored while any drive is BUSY. Defaults to 110 (5.2 sec. at 300 RPM).

MOFF Bits	HSDA	Revolutions	Delay			
			300 RPM	360 RPM	600 RPM	
000 *	0	2	0.4	0.33	0.2	SEC.
000	1	4	—	—	0.4	
001	0	6	1.2	1.0	0.6	
001	1	12	—	—	1.2	
010	0	10	2.0	1.67	1.0	
010	1	20	—	—	2.0	
•	•	•	•	•	•	
•	•	•	•	•	•	
110	0	26	5.2	4.33	2.6	
110	1	52	—	—	5.2	
111	0	30	6.0	5.0	3.0	
111	1	60	—	—	6.0	

NOTE:
If MOFF and MON and HSDA are all zero, Motor Off Delay is infinite. MOTOR Pin must be given a command to go On/Off.

MON

Programs the number of Index pulses that are counted after the MOTOR pin goes active before a command can proceed into the execution phase. This is to give the floppy drive time to spin up and stabilize at the proper speed. If MOTOR is already active, no delay will be generated even if the same drive is selected. The MON bits increment the index count by one and the HSDA bit will double that value if active. All combinations are legal and no checking is done by the 82072.

Defaults to 0000 (0.0 sec. at 300 RPM).

MON	HSDA	Motor on to Command Execution Delay				
		Revolutions	300 RPM	360 RPM	600 RPM	
0000		Zero Motor On Delay				
0001	0	1	0.2	0.17	0.1	SECS.
0001	1	2	—	—	0.2	
0010	0	2	0.4	0.33	0.2	
0010	1	4	—	—	0.4	
0011	0	3	0.6	0.5	0.3	
0011	1	6	—	—	0.6	
:	:	:	:	:	:	
1111	0	15	3.0	2.5	1.5	
1111	1	30	—	—	3.0	

NOTE:
Actual index counts depend upon the position of the disk and when the command begins processing. There is an error rate of −1/+0 revolutions.

The MOTOR logic provides a programmable motor enable signal to the FDDs. This is to allow the drive time to spin up the floppy and stabilize before attempting a read or write. Most floppy drives do not require the drive to be selected (through the DSx line) or to be ready. The application should qualify the MOTOR pin with the drive select outputs. The 82072 will activate the appropriate drive select outputs along with the MOTOR pin. Figure 14 is an example of the interface logic. If a drive is not currently selected or the MOTOR signal is not on, DS and MOTOR are activated the programmed time before the drive is accessed.

NOTE:
This interface logic assumes polling is disabled. undesired drive selects will occur if polling is enabled.

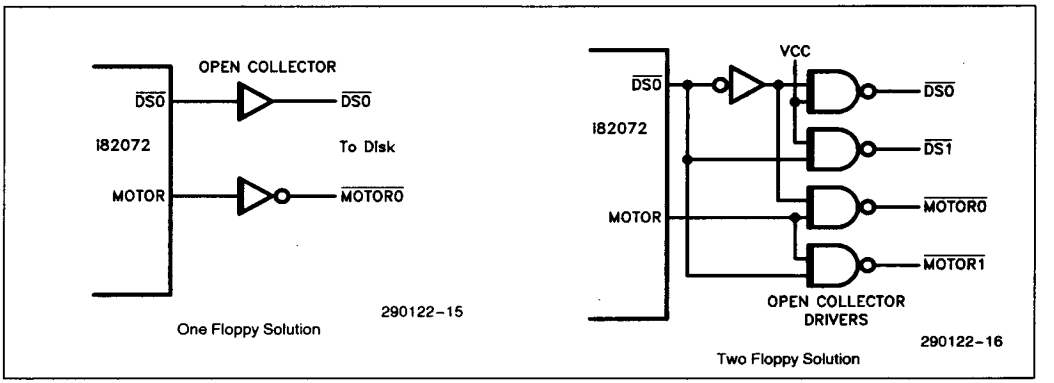


Figure 14. MOTOR and Drive Select Interface

MOTOR ON/OFF COMMAND

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	ON/OFF	DS1	DS0	0	1	0	1	1	Command Code

ON/OFF

Determines whether the command sets the MOTOR pin high or low independent of the internal timer. A "0" takes the MOTOR pin low immediately and a "1" takes the pin to a high. The 82072 returns to the command phase.

The internal timer takes drive changes into account. When switching between drives, the MOFF time will be ignored so that the newly selected drive can be accessed as soon as the MOTOR ON delay has expired. The MOTOR ON/OFF command allows the user to override the programmed delays. The typical implementation would not use the MOTOR ON/OFF command to enable the drive motor because the delays would be the responsibility of the host system.

RELATIVE SEEK

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	<————————			RCN		————————		—>	

NOTE:
The command is coded the same as for SEEK, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control.

DIR	Action
0	Step Head Out
1	Step Head In

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The RELATIVE SEEK command differs from the SEEK command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The SEEK command is good for drives that support a maximum of 256 tracks. RELATIVE SEEKs cannot be overlapped with other RELATIVE SEEKs. Only one RELATIVE SEEK can be active at a time. RELATIVE SEEKs may be overlapped with SEEKs and RECALIBRATEs. Bit 4 of Status Register 0 (EC) will be set if RELATIVE SEEK attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks and that the host needs to read track 300 and the head is on any track (0–255). If a SEEK command was issued, the head would stop at track 255. If a RELATIVE SEEK command was issued, the 82072 would move the head the specified number of tracks, regardless of the internal cylinder position register (but would increment the register). If the head had been on track 40 (D), the maximum track that the 82072 could position the head on using RELATIVE SEEK, would be 296 (D), the initial track, +256 (D). The maximum count that the head can be moved with a single RELATIVE SEEK command is 256 (D).

The internal register, PCN, would overflow as the cylinder number crossed track 255 and would contain 40 (D). The resulting PCN value is thus (NCN + PCN) mod 256. Functionally, the 82072 starts counting from 0 again as the track number goes above 255(D). It is the users responsibility to compensate 82072 functions (precompensation track number) when accessing tracks greater than 255. The 82072 does not keep track that it is working in an "extended track area" (greater than 255). Any command issued would use the current PCN value except for the RECALIBRATE command which only looks for the TRACK0 signal. RECALIBRATE would return an error if the head was farther than 255 due to its limitation of issuing a maximum 256 step pulses. The user simply needs to issue a second RECALIBRATE command. The SEEK command and implied seeks will function correctly within the 44 (D) track (299–255) area of the "extended track area". It is the users responsibility not to issue a new track position that would exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0–255) of tracks, a RELATIVE SEEK would be issued to cross the track 255 boundary.

A RELATIVE SEEK can be used instead of the normal SEEK but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a READ ID command to ensure that the head is physically on the track that software assumes it to be. Different 82072 commands will return different cylinder results which may be difficult to keep track of with software without the READ ID command.

DUMPREG

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	1	1	1	0	*Note
Execution										Registers Placed into FIFO
	R	<			PCN-Drive 0				>	
	R	<			PCN-Drive 1				>	
	R	<			PCN-Drive 2				>	
	R	<			PCN-Drive 3				>	
Result	R	<	SRT	>		<	HUT	>		
	R	<			HLT			>	ND	
	R	<			SC/EOT				>	See Note
	R	HSDA	<	MOFF	>	<	MON		>	
	R	0	EIS	EFIFO	POLL	<	FIFOTHR		>	
	R	<			PRETRK				>	

NOTE:
SC is returned if the last command that was issued was the Format command. EOT is returned if the last command issued was a Read or Write.

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug.

STATUS REGISTER ENCODING

The contents of these registers are available only through a command sequence.

Status Register 0

Bit No.	Symbol	Name	Description
7, 6	IC	Interrupt Code	00-Normal termination of command. The specified command was properly executed and completed without error. 01-Abnormal termination of command. Command execution was started, but was not successfully completed. 10-Invalid command. The requested command could not be executed. 11-Abnormal termination. During the command execution, the RDY signal changed state.
5	SE	Seek End	The 82072 completed a SEEK or RECALIBRATE command, or a READ or WRITE with implied seek command.
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 256 step pulses in the RECALIBRATE command. 2. The RELATIVE SEEK command causes the 82072 to step outward beyond Track 0.
3	NR	Not Ready	RDY pin became a "0" while executing a read, write, seek, or recalibrate command.
2	H	Head Address	The current head address.
1, 0	DS1, 0	Drive Select	The current selected drive.

Status Register 1

Bit No.	Symbol	Name	Description
7	EN	End of Cylinder	The 82072 tried to access a sector beyond the final sector of the track (255D).
6	—	—	Unused. This bit is always "0".
5	DE	Data Error	The 82072 detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the 82072 does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3	—	—	Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. READ DATA, READ DELETED DATA command, the 82072 did not find the specified sector. 2. READ ID command, the 82072 cannot read the ID field without an error. 3. READ TRACK command, the 82072 cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the 82072 is executing a WRITE DATA, WRITE DELETED DATA, or FORMAT TRACK command.
0	MA	Missing Address Mark	Any one of the following: 1. The 82072 did not detect an ID address mark at the specified track after encountering the index pulse from the IDX pin twice. 2. The 82072 cannot detect a data address mark or a deleted data address mark on the specified track.

Status Register 2

Bit No.	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: 1. READ DATA command, the 82072 encounters a deleted data address mark. 2. READ DELETED DATA command, the 82072 encounters a data address mark.
5	DD	Data Error in Data Field.	The 82072 detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82072.
3	—	—	Unused. This bit is always "0".
2	—	—	Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82072 and is equal to FF hex which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The 82072 cannot detect a data address mark or a deleted data address mark.

Status Register 3

Bit No.	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5	RDY	Ready	Indicates the status of the RDY pin.
4	T0	TRACK 0	Indicates the status of the TRK0 pin.
3	—	—	Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1, 0	DS1, 0	Drive Select	Indicates the status of the DS1, DS0 pins.

D.C. SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage ..... −0.5 to +8.0V
Voltage on Any Input .....GND − 2V to 6.5V
Voltage on Any Output..GND − 0.5V to VCC+0.5V
Power Dissipation .....1 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS

T_A = 0°C to = 70°C, V_{CC} = +5V ±10%, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Input Low Voltage, X1	−0.5	0.8	V	
V_{IHC}	Input High Voltage, X1	3.9	V_{CC} +0.5	V	
V_{IL}	Input Low Voltage (all pins except X1)	−0.5	0.8	V	
V_{IH}	Input High Voltage (all pins except X1)	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output High Voltage	3.0 V_{CC} −0.4		V V	I_{OH} = −2.5 mA I_{OH} = 100 μA
I_{CC}	V_{CC} Supply Current (Digital and Analog)		tbd tbd 25 35	mA mA mA mA	(Note 1, 3, 5, 6) (Note 1, 4, 5, 6) (Note 2, 3, 5, 6) (Note 2, 4, 5, 6)
I_{CCSB}	I_{CC} in Powerdown		(Note 7)	mA	(Note 3)
I_{IL}	Input Load Current (all input pins)		10 −10	μA μA	V_{IN} = V_{CC} V_{IN} = 0V
I_{OFL}	Data Bus Output Float Leakage		±10	μA	0.45 < V_{OUT} < V_{CC}

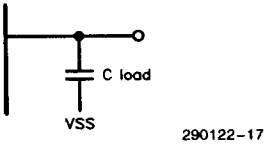
NOTES:
1. Tested at the 1 Mbps data rate.
2. Tested at the 500 kbps data rate.
3. V_{IL} = V_{SS}, V_{IH} = V_{CC}; Outputs not connected to D.C. loads.
4. V_{IL} = 0.8, V_{IH} = 2.0; Outputs not connected to D.C. loads.
5. These are the only inputs that may be floated.
6. Tested while reading a sync field of "00".
7. Currently no maximum value is supported. I_{CCSB} is typically seen as 1 mA in powerdown mode.

Capacitance

C_{IN}	Input Capacitance	10	pF	F = 1 MHz, T_A = 25°C
C_{IN1}	Clock Input Capacitance	20	pF	Sampled, not 100% Tested
$C_{I/O}$	Input/Output Capacitance	20	pF	

NOTE:
All pins except pins under test are tied to AC ground.

LOAD CIRCUIT



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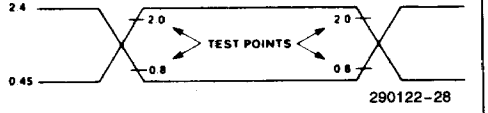
82072 C_{load} = 50 pF for all logic outputs, 100 pF for the data bus.

A. C. TESTING INPUT, OUTPUT WAVEFORM



290122-28

A.C. SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Notes
CLOCK TIMINGS					
t1	Clock Rise Time		10	ns	
	Clock Fall Time		10	ns	
t2	Clock High Time	16	26	ns	(Note 7)
t3	Clock Low Time	16	26	ns	(Note 7)
t4	Clock Period	41.66	41.66	ns	
t5	Internal Clock Period				(Note 3)
HOST READ CYCLES					
t6	Deleted Specification				
t7	Address Setup to $\overline{RD}$	5		ns	
t8	$\overline{RD}$ Pulse Width	100		ns	
t9	Address Hold From RD	0		ns	
t10	Data Valid From $\overline{RD}$		60	ns	
t11	Command Inactive	60		ns	
t12	Output Float Delay		35	ns	
t13	INT Delay From RD		t5+125	ns	
t14	Data Hold From RD	5		ns	

A.C. SPECIFICATIONS (Continued)

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Notes
HOST WRITE CYCLES					
t15	Address Setup to $\overline{WR}$	5		ns	
t16	$\overline{WR}$ Pulse Width	100		ns	
t17	Address Hold from WR	0		ns	
t18	Command Inactive	60		ns	
t19	Data Setup to WR	70		ns	
t20	Data Hold from WR	0		ns	
t21	INT Delay from WR		t5 + 125	ns	
DMA CYCLES					
t22	DRQ Cycle Period	13.0		μs	(Note 1)
t23	DACK to DRQ Inactive		75	ns	
t24	RD to DRQ Inactive		150	ns	(Note 4)
t25	DACK Setup to $\overline{RD}$, $\overline{WR}$	5		ns	
t26	DACK Hold from RD, WR	0		ns	
t27	DRQ to $\overline{RD}$, $\overline{WR}$ Active	0	12.0	μs	(Note 1)
t28	Terminal Count Width		80	ns	
t29	TC to DRQ Inactive		2.5 t5 + 100	ns	
RESET					
t30	Reset Width	170		t4	(Note 5)
t31	Reset to Control Inactive		2	μs	
WRITE DATA TIMING					
t32	Write Data Width			ns	(Note 6)
DRIVE CONTROL					
t33	DS0, 1 Setup to DIR	6	25	μs	(Note 8)
t34	DS0, 1 Hold from DIR	8		μs	
t35	DIR Setup to STEP	0.5	2	μs	
t36	DIR Hold from STEP	10		μs	
t37	STEP Active Time (High)	2.5		μs	
t38	STEP Cycle Time			μs	(Note 2)
t39	INDEX Pulse Width	5		t5	

A.C. SPECIFICATIONS (Continued)

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Notes
READ DATA TIMING					
t40	Read Data Pulse Width	40		ns	
t41	Window Setup to RDDATA	15		ns	
t42	Window Hold from RDDATA	15		ns	
t43	Window Cycle Time	2		µs	FM
	Window Cycle Time	0.5		µs	MFM
f44	PLL Data Rate		500K	bit/s	82072
t44	Data Rate Period				1/f44
tLOCK	Lockup Time		64	t44	

NOTES:
1. This timing is for FIFO threshold = 1. When FIFO threshold is N bytes, the value should be multiplied by N and subtract 1.5 µs. The value shown is for 500 Kbps, scales linearly with data rate.
2. This value can range from 1.0 ms to 16.0 ms and is dependent upon data rate and the specify command value.
3. Many timings are a function of the selected data rate. The nominal values for the internal clock period (t5) for the various data rates are:

500 Kbps	6 x oscillator period = 250 ns
300 Kbps	10 x oscillator period = 420 ns
250 Kbps	12 x oscillator period = 500 ns

4. If $\overline{DACK}$ transitions before $\overline{RD}$, then this specification is ignored. If there is no transition on $\overline{DACK}$, then this becomes the DRQ inactive delay.

5. Reset requires a stable oscillator to meet the minimum active period.
6. Based on the internal clock period (t_5). For various data rates, the Write Data Width minimum values are:

500 Kbps	360 ns
300 Kbps	615 ns
250 Kbps	740 ns

7. Test points for clock high time are 3.5V. Due to transitional times, clock high time max and clock low time max cannot be met simultaneously. Clock high time min and clock low time max cannot be met simultaneously.
8. Based on internal clock period (t_5).

DATA SEPARATOR CHARACTERISTICS

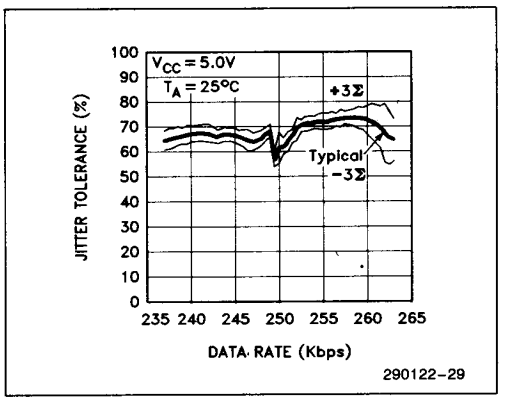


Figure 15. Jitter Tolerance vs Data Rate (F_C = 250 Kbps)

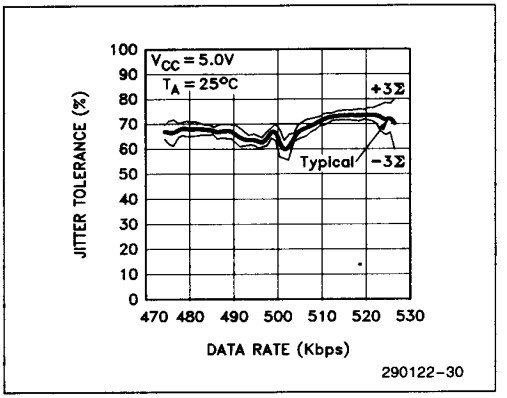


Figure 16. Jitter Tolerance vs Data Rate (F_C = 500 Kbps)

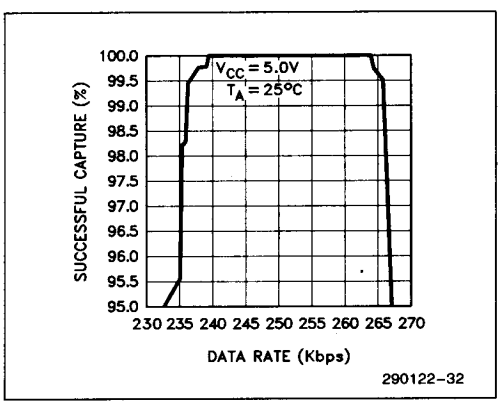


Figure 17. Typical Capture Range (F_C = 250 Kbps)

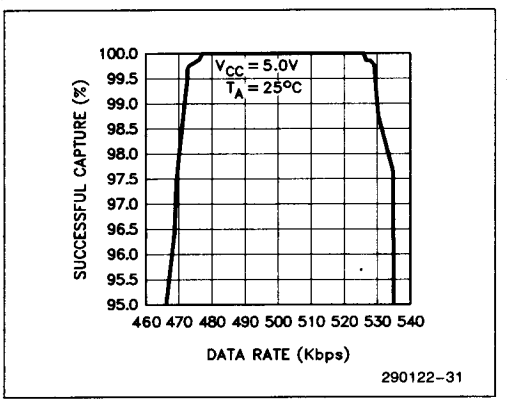


Figure 18. Typical Capture Range (F_C = 500 Kbps)

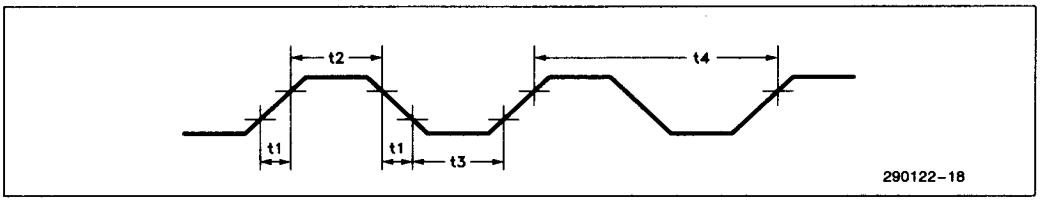
NOTES:

9. Jitter tolerance is defined as: $\frac{\text{Maximum bit shift from nominal position}}{\text{1/4 period of nominal data rate}} \times 100\%$

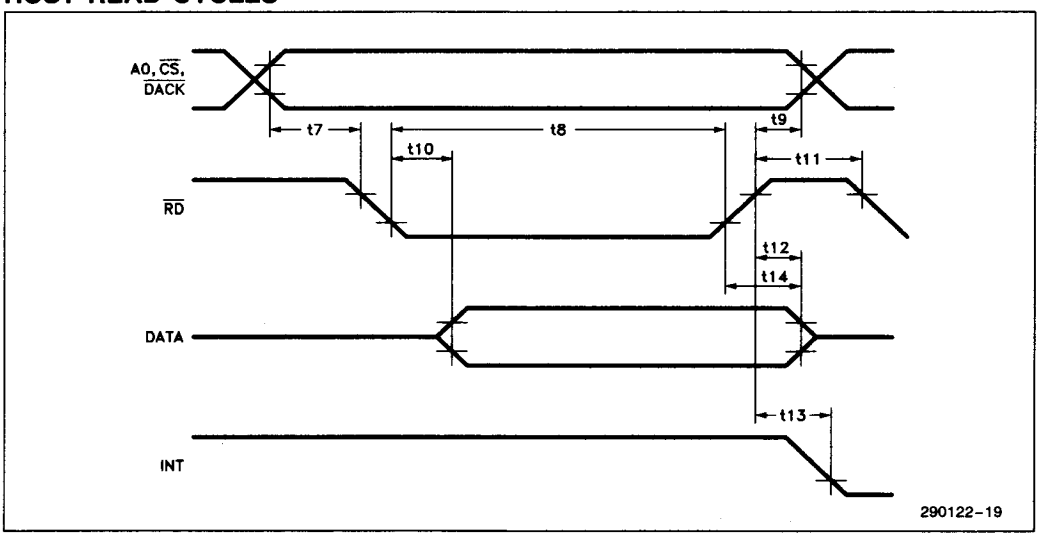
It is a measure of the allowable bit jitter that may be present and still be correctly detected. The data separator jitter tolerance is measured under dynamic conditions that jitters the bit stream according to a reverse precompensation algorithm.

10. Capture range is the frequency range over which the data separator will acquire phase lock with the incoming data stream. This measurement is performed by an iterative process that tabulates the data separator success rate in acquiring lock over a frequency range. The bit stream is jittered by 40% as defined above to reflect typical floppy disk conditions.

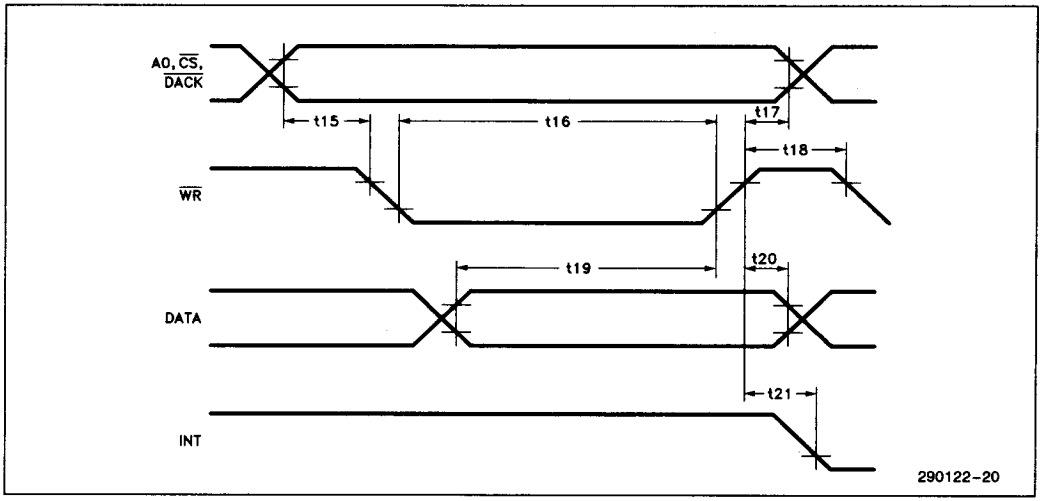
CLOCK TIMING



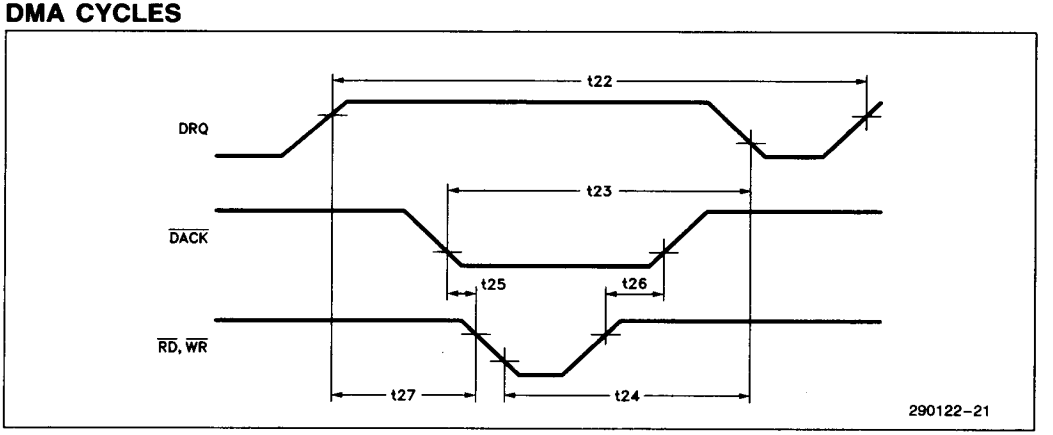
HOST READ CYCLES



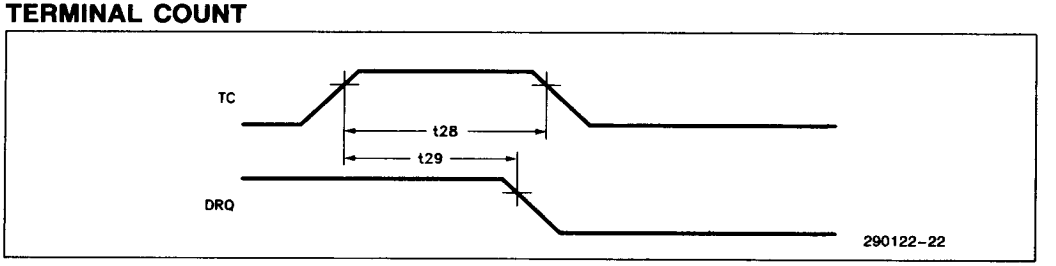
HOST WRITE CYCLES



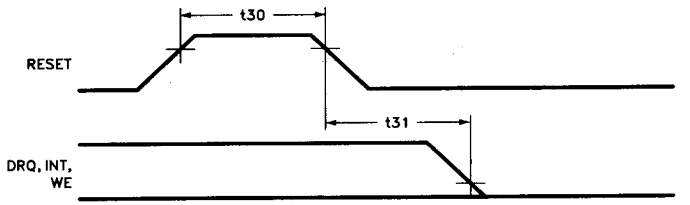
DMA CYCLES



TERMINAL COUNT

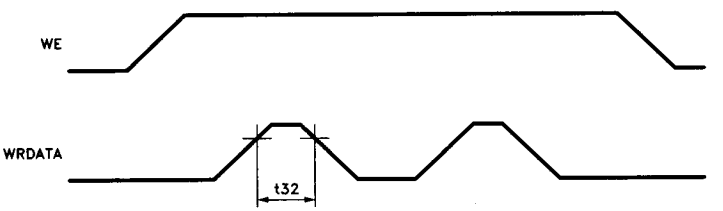


RESET



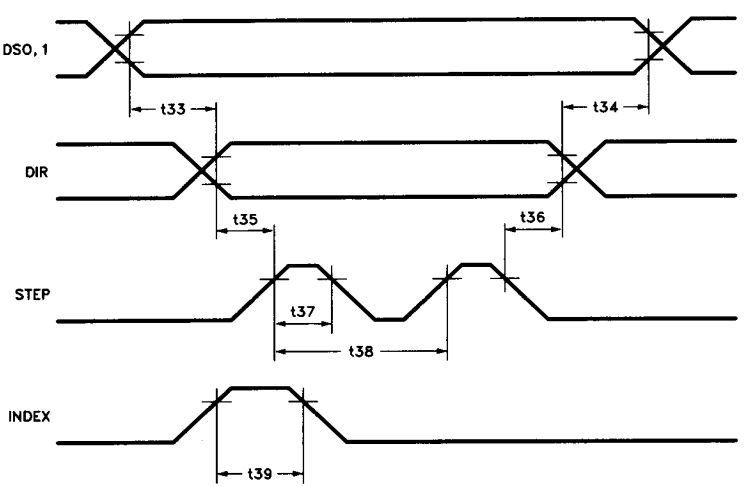
290122-23

WRITE DATA TIMING



290122-24

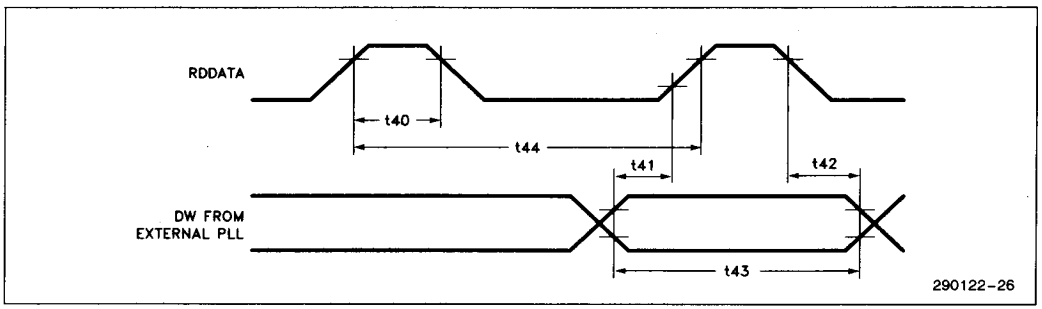
DRIVE CONTROL



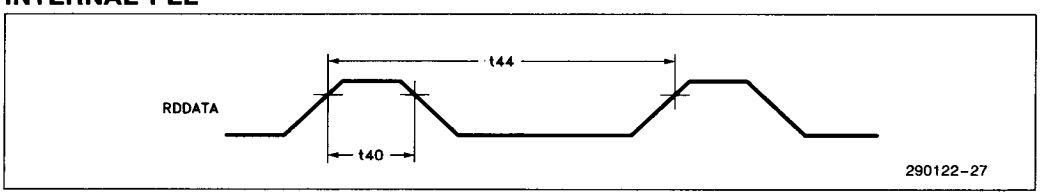
290122-25

NOTE:
For overlapped seeks, only one step pulse per drive selection is issued. Non-overlapped seeks will issue all programmed step pulses.

READ DATA TIMING-EXTERNAL PLL



INTERNAL PLL



REVISION HISTORY

Document:	82072 Preliminary Data Sheet
New Revision Number	290122-005
Previous Revision Number:	290122-004 October 1987

References to 1 Mbps data rate were removed. 1 Mbps data rate will not be supported on the 82072.

D.C. Characteristics Section; Note 7 was added to I_{CCSB} specification.

A.C. Specification Section; t22 and t27 specifications were changed to reflect values at a 500 Kbps data rate, due to 1 Mbps data rate not being supported. t28 specification was changed to reflect design changes made to the latest version of the 82072.