CS8230 386/AT CHIPSet
82C301 BUS CONTROLLER
82C302 PAGE/INTERLEAVE MEMORY CONTROLLER
82A303 HIGH ADDRESS BUFFER
82A304 LOW ADDRESS BUFFER
82B305 DATA BUFFER
82A306 CONTROL BUFFER

The CS8330-16,20,25 AT/386 CHIPSet is a seven chip VLSI implementation of most of the system logic to control an iAPX 386™ based system. The CHIPSet is designed to offer a 100% PC/AT compatible integrated solution. The flexible architecture of the CHIPSet allows it to be used in any iAPX386 based system design, such as CAD/CAE workstations, office systems, industrial and financial transaction systems.

CS8230 CHIPSet combined with CHIPS 82C206, Integrated Peripherals Controller, provides a complete PC/AT compatible system using only 40 components plus memory devices.

The CS8230 CHIPSet consists of one 82C301 Bus Controller, one 82C302 Page/ Interleave Memory Controller, one each of 82A303 and two 82A304 Address Bus Interfaces, two 82A305 or 82B305 Data Bus Interfaces, and a 82A306 Control Signal Buffer. An all CMOS CS8232-16 and CS8232-20 CHIPSet allow OEM's to reduce the form factor, size and weight of their portable and laptop machines due to the CHIPSets' reduced power cooling and buffering requirements. In particular, the all CMOS CS8232-16 and CS8232-20 CHIPSet will reduce a system's power consumption requirement by at least half that of an NMOS/BIPOLAR/CMOS based system.

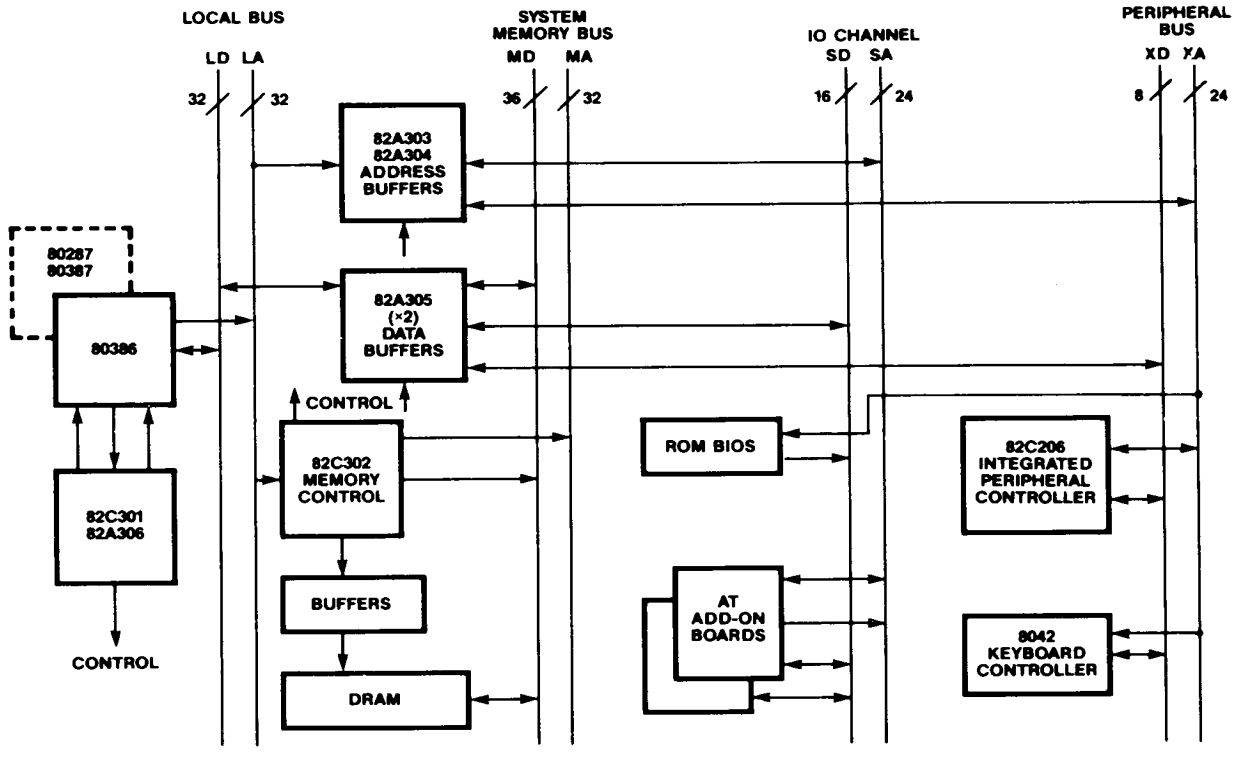

Figure 1. CS8230 AT/386 Block Diagram

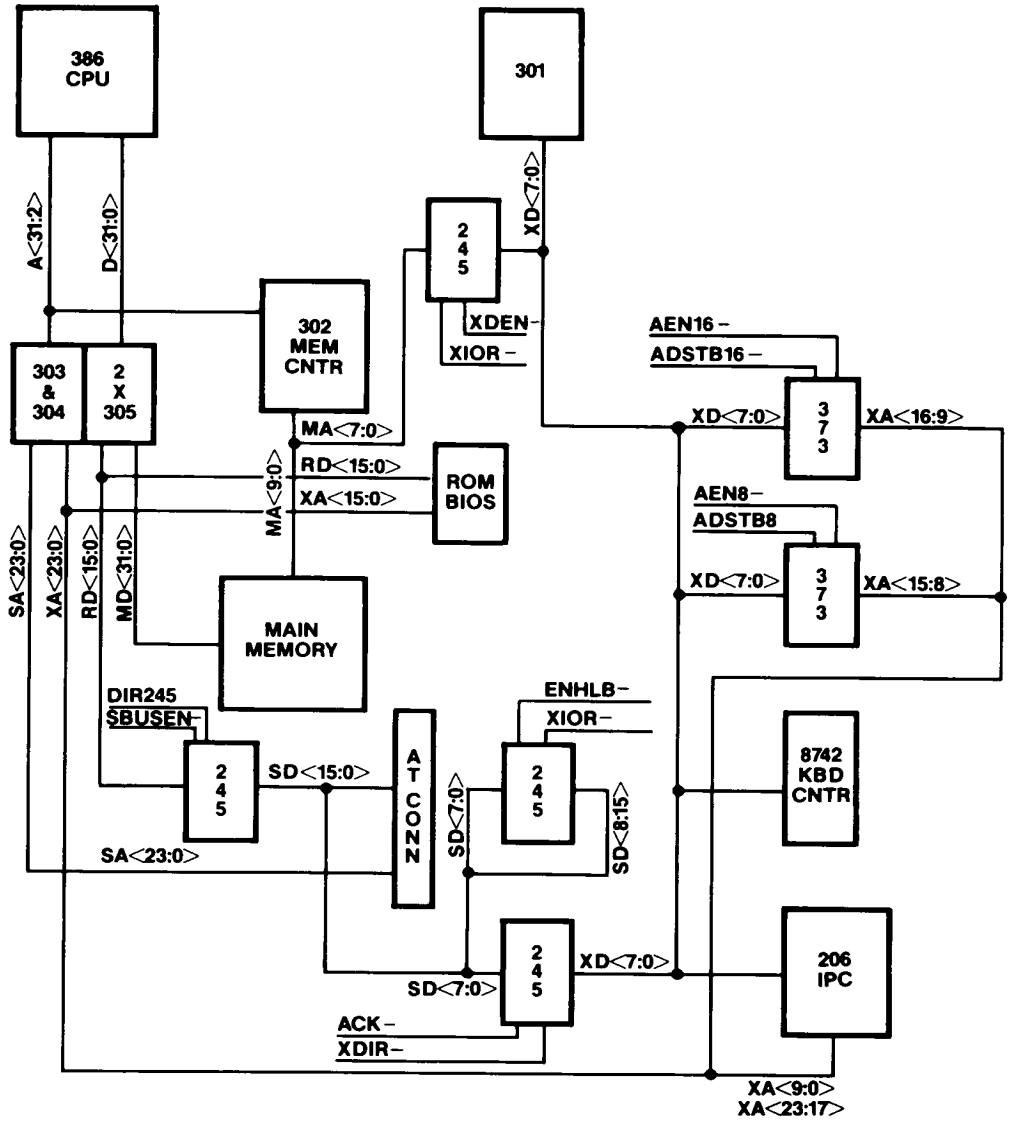

Figure 2. CS8230 AT/386 Detailed Block Diagram