82C605/82C606
CHIPSpak/CHIPSport MULTIFUNCTION CONTROLLERS

- **100% Compatible to IBM™ PC, XT and AT**
- **Fully compatible to the NS16450 Asynchronous Communications Element, and the Motorola™ 146818A Real Time Clock (82C606 only)**
- **Provides a parallel interface which can be configured for use with either a printer or a scanner**
- **Provides two UART channels which can be powered from external sources**
- **Support for a game port**
- **Provides a Real Time Clock with 100 year calendar (82C606 only)**
- **CMOS Configuration RAM with Battery Backup support permits software selection of internal register base addresses (82C606 only)**
- **114 bytes of CMOS RAM**
- **Single chip 68-pin CMOS implementation**

The 82C606 CHIPSpak Multifunction Controller incorporates two UARTs, one parallel port, one game port decoder and one Real Time Clock. The UARTs are fully compatible to the NS16450 and the Real Time Clock is fully compatible with the Motorola 146818A. The 82C606 thus offers a single chip implementation of the most commonly used IBM PC, XT or AT peripherals. While offering complete compatibility with the IBM architecture, the chip offers enhanced features. These include support for power derived from three sources (main, auxiliary and standby), an additional 64 bytes of user RAM for the Real Time Clock and a software configuration scheme which permits development of a system configuration program.

The CHIPSpak Multifunction Controller can be used on the system board to provide serial and parallel ports or on a multifunction card to create a low cost, high density peripheral for use with general purpose microcomputer systems.

The 82C605 CHIPSport is a functional sub-set of 82C606 CHIPSpak. The two products are identical, with the exception of the Real Time Clock. The 82C605 does not integrate the Real Time Clock. All references to 82C606

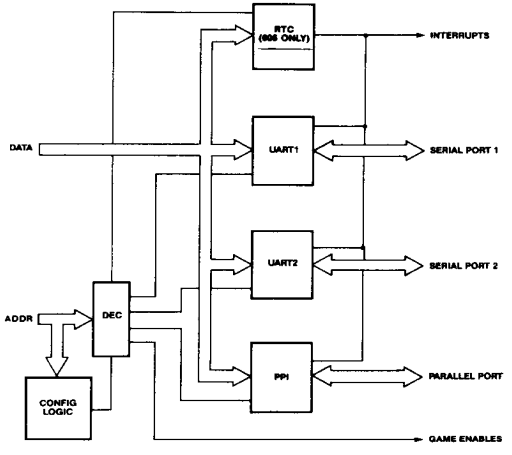


Figure 1. 82C605/606 CHIPSpak/CHIPSport Multifunction Controller Block Diagram

CHIPSpak in this data book are applicable to 82C605 CHIPSport, except where stated otherwise.

The 82C605/82C606 are implemented using advanced CMOS technology and are packaged in 68-pin PLCC packages.

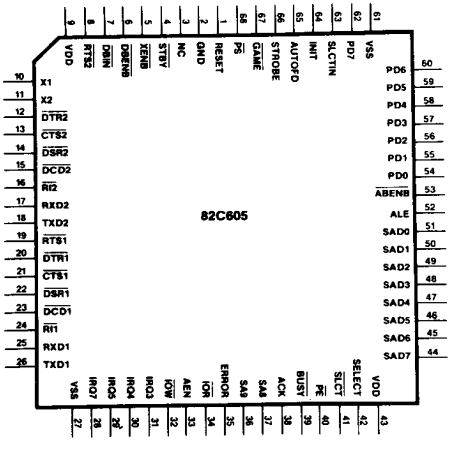


Figure 2a. 82C605 CHIPSport Multifunction Controller Pinout Diagram

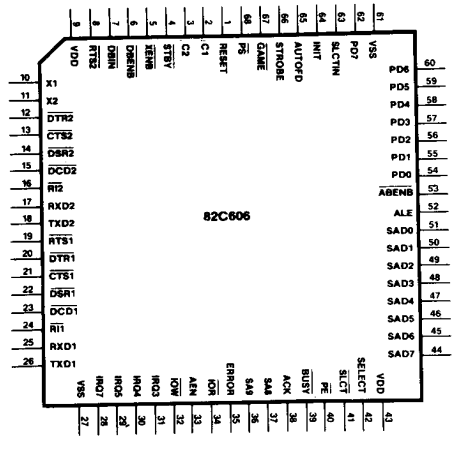


Figure 2b. 82C606 CHIPSpak Multifunction Controller Pinout Diagram

82C605/82C606 Pin Description

Pin No.	Type (Note 1)	Symbol	Pin Description
Clocks and Control			
2	I	C1 (82C606) GND (82C605)	32.768KHz Real Time Clock (RTC) crystal or oscillator input. The signal level should be CMOS compatible. This pin should be connected to ground for 82C605.
3	O	C2 (82C606) NC (82C605)	32.768KHz RTC output to crystal
4	I	$\overline{\text{STBY}}$	ACTIVE LOW. Standby Mode. This signal should be activated when the main power supply is removed. It indicates that the bus interface is invalid and that no response should be made to any bus signals. $\overline{\text{STBY}}$ immediately terminates any bus operations in progress. If the CHIPSpak is resident on a system board, $\overline{\text{STBY}}$ should be connected to POWERGOOD. If the CHIPSpak is on an add-in card, $\overline{\text{STBY}}$ should be generated from the $\overline{\text{RESETDRV}}$ signal.
68	I	$\overline{\text{PS}}$	ACTIVE LOW. Power Sense. A Schmitt trigger input that should be connected to an RC network which delays the rising edge of power (+5V supply). This signal resets the VRT bit in Register D of the RTC and the Valid Configuration bit of the Configuration Enable Register. It also disables the decode logic for the CHIPSpak which then awaits configuration by the setup software. This signal input must be provided to ensure proper operation of 82C606. When $\overline{\text{PS}}$ is asserted the configuration registers are forced to their default values. When battery back-up operation is not desired, $\overline{\text{PS}}$ should be connected to inverted RESET signal.
42	I	SELECT	ACTIVE HIGH. Unit Select. This pin should be connected to any one of SAD<07:04>. It is used to identify a particular CHIPSpak in a system having more than one CHIPSpak. Failure to connect it properly could result in inability to configure the chip. Unit 0 should connect to SAD<04>, unit 1 to SAD<05>, etc.
PC Bus Interface			
52	I	ALE	ACTIVE HIGH. Address Latch Enable.
33	I	AEN	ACTIVE HIGH. Address ENable. Used to gate $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$. When AEN is low, $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ are enabled for the CHIPSpak
34	I	$\overline{\text{IOR}}$	ACTIVE LOW. IO Read strobe.
32	I	$\overline{\text{IOW}}$	ACTIVE LOW. IO Write strobe.

82C605/82C606 Pin Description
(Continued)

Pin No.	Type (Note 1)	Symbol	Pin Description
53	O	$\overline{\text{ABENB}}$	ACTIVE LOW. Address Buffer/Mux ENable. Used to enable a buffer which separates the CHIPSpak SAD<07:00> pins from the system address lines in a system not using multiplexed Address/Data lines.
6	O	$\overline{\text{DBENB}}$	ACTIVE LOW. Data Bus Driver ENable. Used to enable an LS245 type buffer which separates the system Address/Data lines (for multiplexed Address/Data) or system Data lines (non-multiplexed) from the CHIPSpak SAD<07:00>. CHIPSpak pin $\overline{\text{DBIN}}$ controls the direction of this buffer.
5	I	$\overline{\text{XENB}}$	ACTIVE LOW. External Data Bus ENable. This input is internally ORed with the signal used to generate the $\overline{\text{DBENB}}$ output. This allows another controller sharing the board to use the same PC data bus driver without need for an external OR gate. Typically this signal would be created by an EMS or other memory controller. This pin should be tied high when not used.
7	T	$\overline{\text{DBIN}}$	ACTIVE LOW. Data Bus Driver Direction. Used to control the direction of an LS245 type buffer separating the SAD<07:00> lines from the system Data bus. High when $\overline{\text{IOW}}$ is asserted and low when $\overline{\text{IOR}}$ is asserted if a CHIPSpak function has been selected. In high impedance state at all other times to allow other logic to control the Data bus buffer.
36,37	I	SA<09:08>	Two high order bits of the Address Bus.
51-44	B	SAD<07:00>	Multiplexed Address/Data Bus.
31	T	IRQ3	ACTIVE HIGH. Interrupt Request 3. By IBM PC AT and IBM PC XT convention it is used for UART2 (COM2).
30	T	IRQ4	ACTIVE HIGH. Interrupt Request 4. By IBM PC AT and IBM PC XT convention it is used for UART1 (COM1).
29	T	IRQ5	ACTIVE HIGH. Interrupt Request 5. By IBM PC AT convention it is used for parallel port 2.
28	T	IRQ7	ACTIVE HIGH. Interrupt Request 7. By IBM PC AT and IBM PC XT convention it is used for parallel port 1.
1	I	RESET	ACTIVE HIGH. Reset input.
Serial Interface			
10	I	X1	Input pin for the clock or crystal used by the UARTs. The signal level should be CMOS compatible.
11	O	X2	Output pin for the clock or crystal used by the UARTs.

82C605/82C606 Pin Description
(Continued)

Pin No.	Type (Note 1)	Symbol	Pin Description
17	I	RXD2	Input pin for serial data stream to UART2.
25	I	RXD1	Input pin for serial data stream to UART1.
18	O	TXD2	Output pin for serial data stream from UART2.
26	O	TXD1	Output pin for serial data stream from UART1.
8,19	O	$\overline{RTS2}$, $\overline{RTS1}$	ACTIVE LOW. Request To Send. Handshake signals which notify a MODEM or data set that UART2 or UART1 (respectively) is ready to transmit data. This output can be changed by writing to bit 1 of the appropriate MODEM Control Register. High (inactive) after a hardware RESET is performed. Forced high (inactive) during loop mode operation.
13,21	I	$\overline{CTS2}$, $\overline{CTS1}$	ACTIVE LOW. Clear To Send. Handshake signals which notify UART2 or UART1 (respectively) that a MODEM is ready to receive data. The CPU can access this signal by reading bit 4 of the MODEM Status Register (MSR) of the appropriate UART. Bit 0 of the MSR flags a change of state in the corresponding $\overline{CTS}$ signal since the last read of the MSR. This signal does not affect the UART transmitter. A change in state of bit 4 of the MSR ($\overline{CTS}$) will will cause the CPU to be interrupted if bit 3 (MODEM Status) of the Interrupt Enable Register is set.
14,22	I	$\overline{DSR2}$, $\overline{DSR1}$	ACTIVE LOW. Data Set Ready. Handshake signals for UART2 and UART1 respectively. Tells the CPU that the MODEM or data set is ready to transfer characters. Can be monitored by reading bit 5 of the appropriate MODEM Status Register (MSR). A change in the state of this bit since the last read of the MSR will cause bit 1 of the MSR to go high. An interrupt will be generated when bit 5 of the MSR changes state if MODEM Status interrupts are enabled (bit 3 of the Interrupt Enable Register).
12,20	O	$\overline{DTR2}$, $\overline{DTR1}$	ACTIVE LOW. Data Terminal Ready. Notifies the MODEM or data set that UART2 or UART1 (respectively) is ready to transfer characters. Can be activated by writing a 1 to bit 0 of the MODEM Control Register. Forced high (inactive) during loop mode operation.

82C605/82C606 Pin Description
(Continued)

Pin No.	Type (Note 1)	Symbol	Pin Description
15,23	I	$\overline{DCD2}$, $\overline{DCD1}$	ACTIVE LOW. Data Carrier Detect. Notifies UART2 or UART1 (respectively) that a carrier signal has been detected by a MODEM. The CPU can monitor the value of this bit by reading bit 7 of the MODEM Status Register (MSR). A change in the state of this signal since the last read of the MSR will cause bit 3 of the MSR to go high. This signal has no affect on the UART receiver. An interrupt will be generated when bit 7 of the MSR (DCD) changes state if MODEM Status interrupts are enabled (bit 3 of the Interrupt Enable Register).
16,24	I	$\overline{RI2}$, $\overline{RI1}$	ACTIVE LOW. Ring Indicator. Notifies UART2 or UART1 (respectively) that a telephone ringing signal has been detected by a MODEM or data set. Can be monitored by the CPU by reading bit 6 of the MODEM Status Register (MSR). When this signal goes to an inactive state (from low to high), bit 2 of the MSR will be set. If MODEM Status interrupts are enabled, activation of this signal (high to low transition) will generate an interrupt.
Parallel Interface			
62,60-54	B	PD0-PD7	Parallel Port Data Bus. Printer: output only. Scanner: bidirectional.
38	I	ACK	ACTIVE HIGH, Acknowledge. Printer: handshake signal indicating that data has been received. Scanner: handshake signal indicating that data has been received.
39	I	$\overline{BUSY}$	ACTIVE LOW, Busy signal. Printer: it indicates that printer is unable to receive data. Scanner: in print mode (PR/SC is high), it indicates that scanner is unable to receive data.
40	I	$\overline{PE}$	ACTIVE LOW, Paper End signal. Printer: end of paper has been detected. Scanner: used as FAULT status indicator.
41	I	$\overline{SLCT}$	ACTIVE LOW, Select. Printer: indicates printer is selected. Scanner: indicates ready for another character.

82C605/82C606 Pin Description
(Continued)

Pin No.	Type (Note 1)	Symbol	Pin Description
35	I/O	ERROR	ACTIVE HIGH, Error. Printer: when HIGH indicates an error has occured. Scanner: busy signal from host, unable to receive.
66	O	STROBE	ACTIVE HIGH. Strobe. Printer: data strobe. Scanner: data strobe.
63	O	SLCTIN	ACTIVE HIGH. Select In. Printer: to select printer. Scanner: to select scanner and enable data buffer.
64	O	INIT	ACTIVE HIGH. Initialize. Printer: Initialize. Scanner: reset.
65	O	AUTOFD	ACTIVE HIGH. Auto Feed. Printer: causes printer to generate a line feed after each line is printed. Scanner: Print/Scan (PR/SC*), data buffer directional control signal.
Game Port			
67	O	$\overline{\text{GAME}}$	ACTIVE LOW. Game Port Enable. Active when the specified I/O address is valid and $\overline{\text{AEN}}$ is low. This signal must be externally gated with $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ to ensure proper access to a game peripheral. It can also be used as a programmable decoder for any peripheral device.
Power and Ground			
9,43		VDD	Power Supply
27,61		VSS	Ground

NOTE 1: The abbreviations used in the column labeled 'Type' are as follows:
I = Input
T = 3-state output
O = Output (always active)
D = Output (open drain)
I/O = Input and Output (depends on CHIPSpak mode)
B = Bidirectional

CHIPSport/CHIPSpak MULTIFUNCTION CONTROLLERS

The 82C606 is an LSI implementation of the most commonly used peripheral devices found in an IBM PC, XT or AT. The device contains the equivalent of two NS16450 UARTs, one Motorola 146818A Real Time Clock and one parallel port. Decoding logic and one output suitable for use with a game port, support for main, auxiliary and standby power supplies and software configurable base addresses for these devices, operational modes and interrupts are also included. Figure 1 depicts the subsystems present in the 82C606. The CHIPSport 82C605 contains all functions except the Real Time Clock.

Each of the two UARTs implements a fully functioned serial link. Programmable character length, parity generation and detection, stop-bit generation and baud rate generation are provided. Double buffering is used so that precise synchronization is unnecessary. Status information is accessible to the CPU by reading internal registers. MODEM control lines are provided, as are internal diagnostic functionality and interrupt prioritization. Support for an auxiliary power system (such as that derived from a telephone line or RS232 link) permits a CHIPSpak in a battery-powered device to consume no battery power until an incoming character is detected.

A Real Time Clock (RTC) is included in the 82C606 only for maintaining the time and date. This subsystem contains 114 bytes of RAM in additionto the Clock/Calendar. The date/time data and the additional RAM contents can be maintained without system power by using an external circuit to connect the device to a battery when system power is removed.

The parallel port can be configured for output only (printer application) or input and output (scanner application). The necessary control signals are provided for use as a Centronics-compatible (output only) parallel port. For scanner applications, a Centronics-like interface is used. Such an interface is utilized by the RICOH IS30 scanner.

The game port circuitry provides a decoded output for use by any peripheral. The base address of this peripheral is software programmable.

The configuration RAM and circuitry support programmable base addresses for all registers internal to the CHIPSpak. This permits creation of a menu-driven program for system configuration. It also permits integration of multiple CHIPSpaks in a single system, or one or more CHIPSpaks with other devices which provide overlapping functionality (for instance serial and parallel ports). Selection of sources for interrupts, enabling and configuring of on-chip subsystems (UARTs, parallel port, etc.) and control of the configuration process itself are also handled with this RAM and its associated circuitry.

The remainder of this data sheet will consider each of the aforesaid subsystems individually. Sections containing more general design data for the chip as a whole are at the end along with electrical and physical characteristics.

UARTS

The equivalent of two NS16450 UARTs is implemented on the 82C606. Since the two UARTs are identical, only one is described below. An on-chip baud rate generator divides the input clock or crystal frequency by a number from 1 to 65535. This frequency is used for both receiving and transmitting serial data. An external clock or a crystal can be used.

Serial-to-parallel conversion is performed on received data and parallel-to-serial conversion is performed on transmitted data. Status of either or both the UARTs is available at any time. To access it, the CPU reads the appropriate status register in the CHIPSpak. The current state and type of a transfer are contained in this status information as are details regarding any errors encountered. The conditions under which the processor will be interrupted and the interrupt line to be used are programmable.

Control lines are provided to permit interfacing to a MODEM. Internal diagnostics are supported. These permit simulation of break, parity, overun and framing error conditions as well as operation in loopback mode.

Using Standby or Auxiliary Power Sources

Support for use of a Standby (battery) or Auxiliary (derived from a telephone line or RS232 link) power supply is provided by the 82C606. An external circuit must be used to alter the source of current to the VDD pins.

The UART can be made to wake up the CPU upon receipt of a character. This is useful in certain applications (such as battery powered transportable computers) where power consumption must be minimized. To implement this, an Auxiliary or Standby power source must be provided. In addition, an interrupt must be generated upon receipt of a character. This interrupt initiates a power up sequence which culminates in the servicing of the interrupt. In order for this to work properly, the CHIPSpak RESET function must be programmed so that it will not alter the values of the UART control registers (see below).

Note that since the baud rate generator dissipates more power than many of the other CHIPSpak circuits, use of a battery for Standby power may prove to be infeasible. If this is the case, reducing another power source to the +5V needed by the CHIPSpak may be the solution. The 55 to 110 volts from a telephone line or the +9 to +12 volts from an RS232 link are two possible sources for input voltages.

Accessible Registers

Addressing of the accessible UART registers is shown in the table below. The base address of all registers is software programmable during the configuration sequence (see the section entitled "Configuration Sequence".) UART registers are located at sequentially increasing addresses above this base address. A CHIPSpak contains two UARTs, each of which contains one set of the registers described below.

Table 1 Addressing of UART Registers

DRAB	SAD2	SAD1	SAD0	Register Name
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Flag (read)
X	0	1	1	Byte Format
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratchpad
1	0	0	0	Divisor LSB
1	0	0	1	Divisor MSB

Where:
X = Don't Care
MSB = Most Significant byte
LSB = Least Significant byte
DRAB = Divisor Register Address Bit

BIT DEFINITIONS OF ACCESSIBLE REGISTERS

Receive Buffer (RB)

This register holds the incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Double buffering is supported by the CHIPSpak. This scheme uses an additional shift register (the Receive Shift Register; not user accessible) to assemble the incoming byte before it is loaded into the Receive Buffer.

Transmit Buffer (TB)

This register holds the data byte to be sent. Bit 0 is the least significant bit, which is transmitted and received first. Double buffering is supported by the CHIPSpak. This scheme uses a shift register (the Transmit Shift Register; not user accessible) which is loaded from the Transmit Buffer. The transmitted byte is then shifted out of the Transmit Shift Register to the TXD pin.

Interrupt Enable Register (IER)

The low order 4 bits of this register control the enabling of each of the four possible types of interrupts. Setting a bit to a logic 1 enables the corresponding interrupt. It is possible to enable all, none or some of the interrupt sources. Disabling all interrupts means that the Interrupt Flag register content is not valid and that none of the interrupt signals output by CHIPSpak can be triggered by a UART. All other portions of the UART are unaffected by the disabling of interrupts. The individual bit definitions are as follows:

Bit 0: A logic 1 here causes an interrupt when the Receive Buffer contains valid data.

Bit 1: A logic 1 here causes an interrupt when the Transmit Buffer is empty.

Bit 2: A logic 1 here causes an interrupt when an error (Overun, Parity, Framing or Break) has been encountered. The Line Status register must be read to determine the type of error.

Bit 3: A logic 1 here causes an interrupt when one of the bits in the MODEM Status register changes state.

Bits 4-7: These four bits are set to 0.

Interrupt Flag Register (IFR)

When accessed, this register reports the highest pending interrupt. By reading it, the CPU can determine the source of the interrupt and can act accordingly. The Interrupt Flag register (IFR) records the highest pending interrupt in bits 0 through 2. Other interrupts are temporarily disregarded (they are internally saved by the CHIPSpak) until the highest priority one is serviced.

Four levels of prioritized interrupts exist. In descending order of priority they are:

1. Line Status (highest priority)
2. Receive Buffer full
3. Transmit Buffer empty
4. MODEM Status (lowest priority)

Bit definitions for the IFR are as follows:

Bit 0: If this bit is a zero, an interrupt is pending and bits 1 and 2 can be read to determine the source of the interrupt. When this bit is a logic 1, no interrupts are pending. Note that this bit can be used in a polled environment to determine if an interrupt is pending. It can also be used for the same purpose with a hardwired interrupt priority scheme. In the latter case, bits 1 and 2 of this register act as a pointer to an interrupt service routine.

Bits 1 and 2: As indicated in the table below, these two bits specify the type and source of the interrupt.

Bits 3-7: These five bits are set to 0.

Table 2 UART Interrupt Specifications

Bit 2	Bit 1	Bit 0	Priority	Type	Source	The Interrupt
0	0	1	—	None	None	—
1	1	0	Highest	Line Status	Overun Error or Parity Error or Framing Error or Break Interrupt	Read Line Status Register
1	0	0	Second	Receive Buffer Full	Received Data	Rd Receive Buffer
0	1	0	Third	Transmit Buffer empty	Transmit Buffer	Read IFR or Wr Transmit Buffer
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Carrier Detect	Read MODEM Status Register

Byte Format Register (BFR)

This read/write register contains format information for the serial line. Since it can be read, a separate copy of its content need not be kept in system memory. Bit definitions are as follows:

Bits 0 and 1: These specify the word length for received and transmitted characters. Start, stop and parity bits are not included in the word length value. The word lengths are:

Bit 0	Bit 1	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: The combination of this bit and Bits 0 and 1 of this register determine the number of stop bits used with each transmitted character. The table below summarizes this information. Note that the receiver will ignore additional stop bits beyond the first regardless of the number of stop bits used when transmitting.

Bit 2	Word Length	# of Stop Bits
0	—	1
1	5 Bits	1½
1	6 Bits	2
1	7 Bits	2
1	8 Bits	2

Bit 3: A logic 1 in this bit enables parity generation (during transmission) and checking (during receipt). The parity bit is always after the last data bit but before the first stop bit. If enabled, a parity bit of the proper state (0 or 1) is generated such that the sum (carry ignored) of all data bits plus the parity bit produces either an even (even parity) or odd (odd parity) value.

Bit 4: This Even Parity bit controls parity sense. It is ignored unless Bit 3 is a logic 1. If

Bits 3 and 4 are logic 1's (even parity), an even number of logic 1's will be transmitted and a parity error will be generated each time an odd number is received. If Bit 3 is a 1 and Bit 4 is a 0 (odd parity), an odd number of logic 1's will be transmitted and a parity error will be generated each time an even number is received.

Bit 5: This is the Force Parity bit. It ensures that the parity bit and sense (even or odd) match regardless of the sum normally used to determine parity. Thus if Bits 3, 4 and 5 are all logic 1's (even parity), the parity bit transmitted will always be a 0 and a parity error will be generated if a logic 1 parity bit is received. If Bits 3 and 5 are 1 and Bit 4 is 0, the parity bit transmitted will always be a 1 and a parity error will be generated if a 0 parity bit is received.

Bit 6: This BREAK bit, when set to a logic 1, forces the transmitted data output pin (TXD2 or TXD1) to a Spacing or logic 0 condition. This BREAK condition is terminated when Bit 6 is set to a 0. The operation of the transmitter logic is unaffected by the value of this bit; only the value of the corresponding TXD pin is affected. A BREAK condition is typically used to signal a terminal or communications system. To prevent the transmission of erroneous data, follow the steps below:

1. Load a NULL character (all zeroes) into the Transmit Buffer.
2. Load Bit 6 (BREAK bit) after the next Transmit Buffer Empty (TBE) occurs.
3. Time the length of the BREAK condition by continuing to load NULL characters into the Transmit Buffer and counting the number loaded.
4. Clear the BREAK condition only after a Transmitter Empty (TEMT) condition occurs.

Bit 7: This Divisor Register Address Bit (DRAB) must be a logic 1 to permit access to the Divisor Registers. Access to all other internal UART registers requires that this bit be 0.

Modem Control Register (MCR)

This byte-wide register is used to manage the connection to an external MODEM or data set. Bit definitions are as follows:

Bit 0: This $\overline{\text{DTR}}$ bit determines the state of the corresponding $\overline{\text{DTR}}$ output pin ($\overline{\text{DTR2}}$ or $\overline{\text{DTR1}}$). Setting Bit 0 to a logic 1 forces $\overline{\text{DTR}}$ to its active state (logic 0). If Bit 0 is a logic 0, $\overline{\text{DTR}}$ will be inactive (logic 1). An external inverting buffer is typically used (to insure the proper polarity of $\overline{\text{DTR}}$) when connecting a CHIPSpak $\overline{\text{DTR}}$ output to a MODEM or data set.

Bit 1: This $\overline{\text{RTS}}$ bit determines the state of the corresponding $\overline{\text{RTS}}$ CHIPSpak output pin in a fashion identical to Bit 0 (see above).

Bit 2: This bit is internally connected to bit 6 (RI) of the MODEM Status Register (MSR) in diagnostic loopback mode (MCR bit 4 is a logic 1). A 1 in this bit will force the $\overline{\text{RI}}$ bit (bit 6 of the MSR) to be active (logic 0) when the CHIPSpak UART is in diagnostic loopback mode. A 0 will force the $\overline{\text{RI}}$ bit to be inactive.

Bit 3: This bit is internally connected to bit 7 (DCD) of the MODEM Status Register (MSR) in diagnostic loopback mode (MCR bit 4 is a logic 1). A 1 in this bit will force the $\overline{\text{DCD}}$ bit (bit 7 of the MSR) to be active (logic 0) when the CHIPSpak UART is in diagnostic loopback mode. A 0 will force the $\overline{\text{DCD}}$ bit to be inactive, and a 1 enables UART interrupts.

In the normal mode (no loopback), this bit is OUT2. When OUT2 = 0 (default), the corresponding interrupt is forced into a high impedance. When OUT2 = 1, the interrupt output is enabled.

Bit 4: This Loopback bit is used for self-diagnostic purposes. If it is a logic 1:

1. The corresponding TXD CHIPSpak output pin (TXD2 or TXD1) is set to a logic 1 (Marking state) and is disconnected from the output of the Transmit Shift Register;

2. The corresponding RXD CHIPSpak input pin (RXD2 or RXD1) is disconnected from the Receive Shift Register;

3. The input to the Receiver Shift Register is internally connected to the output of the Transmit Shift Register;

4. All MODEM control input pins ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected from the internal circuitry;

5. MODEM control output pins $\overline{DTR}$ and $\overline{RTS}$ are forced to their inactive state (logic 1);

6. MODEM control output $\overline{DTR}$ is connected internally to MODEM control input $\overline{DSR}$ MODEM control output $\overline{RTS}$ is internally connected to input $\overline{CTS}$. MODEM Control Register (MCR) bit 2 determines the state of bit 6 of the MODEM Status Register (MSR). Bit 3 of the MCR controls bit 7 of the MSR.

7. Data which is transmitted will immediately be received, permitting the CPU to verify the data paths internal to the CHIPSpak and its connection to the CPU.

While operating in diagnostic loopback mode, interrupts are disabled. Interrupts are controlled by the Interrupt Enable register. Interrupts which are due to MODEM signals operate as documented, although the source is now the lower 4 bits of the MODEM Control Register rather than the MODEM input pin signals.

Bits 5, 6 and 7: These bits are set to 0.

Line Status Register (LSR)

This byte-wide register supplies serial link status information to the CPU. A Receive Line Status interrupt is caused by one of the conditions flagged by Bits 1 through 4 of this register. It is read-only. Writes to it are used at the factory for testing purposes and are not recommended. Bit definitions are as follows:

Bit 0: This Receive Buffer Full (RBF) bit is set to a logic 1 when an incoming character has been transferred from the Receive Shift Register to the Receive Buffer. Reading the Receive Buffer resets it to a logic 0.

Bit 1: This Overun Error bit is set to a logic 1 when a new character is transferred into the Receive Buffer before the previously received character was read by the CPU. The previously received character is lost. When the CPU reads the LSR, the Overun Error bit is reset to a 0.

Bit 2: This Parity Error bit is set to a logic 1 whenever a parity error is detected (received character has a parity other than that selected). Reading the LSR resets this bit to a 0.

Bit 3: This Framing Error bit is set to a logic 1 when an incoming character has no stop bit after the last data bit or (if parity is enabled) after the parity bit. A valid stop bit is the presence of a Mark condition (logic 1) in the proper time slot after the last data bit or the parity bit. Reading the LSR resets this bit to a 0.

Bit 4: This Break Interrupt bit will be a logic 1 if a Space condition (logic 0) is present on the corresponding RXD (RXD2 or RXD1) line for an entire character time (start bit time, plus data bit times, plus parity bit time, plus stop bit time). Reading the LSR resets this bit to a 0.

Bit 5: This Transmit Buffer Empty (TBE) bit is set to a logic 1 when an outgoing character is loaded from the Transmit Buffer (TB) into the Transmit Shift Register. If the TBE interrupt is enabled, an interrupt will be generated when this bit is set. Writing a character to the TB resets this bit to a 0.

Bit 6: This Transmitter Empty (TEMT) bit will be set to a logic 1 when both the Transmit Buffer and the Transmit Shift Register are empty. When either of these two registers contains a character, this bit will be reset to a 0.

Bit 7: This bit is set to 0.

MODEM Status Register (MSR)

This byte-wide register holds the current value of the MODEM control lines. It also sets a bit (to a logic 1) each time one of these control lines changes state. Reading the MSR resets all of the Change bits to 0. A MODEM Status Interrupt is generated (if it is enabled) when Bit 0, 1, 2 or 3 is set to a 1. Bit definitions are:

Bit 0: This is the Clear To Send Changed bit. It is set to a 1 if the corresponding $\overline{CTS}$ line ($\overline{CTS2}$ or $\overline{CTS1}$) has changed state since the last time the MSR was read.

Table 3 Summary of Accessible Register Bit Definitions
Part 1 of 2

Bit #	Receive Buffer RB	Transmit Buffer TB	Interrupt Enable Register IER	Interrupt Flag Register IFR	Byte Format Register BFR	MODEM Control Register MCR
0	Data Bit 0	Data Bit 0	Enable Receive Buffer Full Interrupt	Logic 0 if Interrupt Pending	Word Length Bit 0	Data Terminal Ready (DTR)
1	Data Bit 1	Data Bit 1	Enable Transmit Buffer Empty Interrupt	Interrupt ID Bit 0	Word Length Bit 1	Request To Send (RTS)
2	Data Bit 2	Data Bit 2	Enable Receive Line Status Interrupt	Interrupt ID Bit 1	Number of Stop Bits	Drives $\overline{RI}$ internally in loopback mode
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt	0	Parity Enable	Drives $\overline{DCD}$ Internally in loopback mode OUT2 in non-loopback mode
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select	Loop
5	Data Bit 5	Data Bit 5	0	0	Force Parity	0
6	Data Bit 6	Data Bit 6	0	0	Set BREAK	0
7	Data Bit 7	Data Bit 7	0	0	Divisor Register Address Bit (DRAB)	0

Bit 1: This is the Data Set Ready Changed bit. It is set to a 1 if the corresponding $\overline{DSR}$ line ($\overline{DSR2}$ or $\overline{DSR1}$) has changed state since the last time the MSR was read.

Bit 2: This is the Rising Edge of Ring Indicator bit. It is set to a 1 if the corresponding $\overline{RI}$ line ($\overline{RI2}$ or $\overline{RI1}$) has changed from a logic 0 to a logic 1 since the last time the MSR was read.

Bit 3: This is the Data Carrier Detect Changed bit. It is set to a 1 if the corresponding $\overline{DCD}$ line ($\overline{DCD2}$ or $\overline{DCD1}$) has changed state since the last time the MSR was read.

Bit 4: This is the Clear To Send bit. It is the complement of the corresponding $\overline{CTS}$ ($\overline{CTS2}$ or $\overline{CTS1}$) pin. When in diagnostic loopback mode, this bit is identical to the RTS bit in the MODEM Control Register (MCR).

Bit 5: This is the Data Set Ready bit. It is the complement of the corresponding $\overline{DSR}$ ($\overline{DSR2}$ or $\overline{DSR1}$) pin. When in diagnostic loopback mode, this bit is identical to the DTR bit in the MCR.

Bit 6: This is the Ring Indicator bit. It is the complement of the corresponding $\overline{RI}$ ($\overline{RI2}$ or $\overline{RI1}$) pin. In diagnostic loopback mode, it is controlled by Bit 2 of the MCR.

Bit 7: This is the Data Carrier Detect bit. It is the complement of the corresponding $\overline{DCD}$

Summary of Accessible Register Bit Definitions
Part 2 of 2

Bit #	Line Status Register LSR	MODEM Status Register MSR	Scratch-pad Register SR	Divisor Register LSB DRL	Divisor Register MSB DRM
0	Receive Buffer Full (RBF)	Clear To Send Changed	Bit 0	Bit 0	Bit 8
1	Overrun Error	Data Set Ready Changed	Bit 1	Bit 1	Bit 9
2	Parity Error	Rising Edge of Ring Indicator	Bit 2	Bit 2	Bit 10
3	Framing Error	Data Carrier Detect Changed	Bit 3	Bit 3	Bit 11
4	BREAK Interrupt	Clear To Send	Bit 4	Bit 4	Bit 12
5	Transmit Buffer Empty	Data Set Ready	Bit 5	Bit 5	Bit 13
6	Transmitter Empty	Ring Indicator	Bit 6	Bit 6	Bit 14
7	0	Data Carrier Detect	Bit 7	Bit 7	Bit 15

($\overline{DCD2}$ or $\overline{DCD1}$) pin. In diagnostic loopback mode, it is controlled by Bit 3 of the MCR.

Scratchpad Register

This byte-wide register has no effect on the UART within which it is located. It can be used for any purpose by the programmer.

Summary Table of Accessible Register Bit Definitions

Table 3 summarizes the bit definitions in all of the UART accessible registers.

Effects of a Hardware Reset

The table below details the effect of a hardware RESET on each of the UARTs located in a CHIPSpak. Note that the CHIPSpak has a configuration option which permits only a part of each UART to be reset when a hardware RESET is applied. This option is useful when the CHIPSpak will monitor a serial link and wake up the CPU upon receipt of an incoming character. Bit 7 in CHIPSpak Configuration Register 1 controls this option. When Bit 7 is a 0, all registers in each UART except the Receive Buffer, Transmit Buffer

Table 4 Action of a Hardware Reset on the CHIPSpak UARTs

Register or Signal	Cause of Reset	Reset State
Interrupt Enable Register	Hardware RESET	All bits = logic 0
Interrupt Flag Register	Hardware RESET	Bit 0 = logic 1 Other bits = logic 0
Byte Format Register	Hardware RESET	All bits = logic 0
MODEM Control Register	Hardware RESET	All bits = logic 0
Line Status Register	Hardware RESET	Bits 5, 6 = logic 1 Other bits = logic 0
MODEM Status Register	Hardware RESET	Bits 0–3 = logic 0 Bits 4–7 = Input Signal
TXD2 and TXD1	Hardware RESET	logic 1 (high)
Receive Line Status Interrupt	Hardware RESET or Read LSR	logic 0 (low)
Receive Buffer Full Interrupt	Hardware RESET or Read RB	logic 0 (low)
Transmit Buffer Empty Interrupt	Hardware RESET or Read TB	logic 0 (low)
MODEM Status Interrupt	Hardware RESET or Read MSR	logic 0 (low)
$\overline{RTS2}$ and $\overline{RTS1}$	Hardware RESET	logic 1 (high)
$\overline{DTR2}$ and $\overline{DTR1}$	Hardware RESET	logic 1 (high)

and the Divisor Registers (LSB and MSB) will be reset when a hardware RESET occurs. If Bit 7 is a 1, none of the registers in the UARTS will be reset. See the section of this data sheet which covers Configuration for more details. The table below assumes that Bit 7 of the CHIPSpak Configuration register is a zero.

Baud Rate Generation

The table below details the content of the Divisor Registers for various baud rates when using either a 1.8432 MHz or a 3.072 MHz crystal. All table values are decimal. Following the table, Figure 3 depicts the use of an external oscillator for baud rate clock control and Figure 4 shows the connection of a crystal to the CHIPSpak.

PARALLEL PORT

The parallel port can be configured for either of two different modes of operation: printer (output only) and scanner (bidirectional). While there is a high degree of compatibility between these modes, there are a few differences in operation and in definition of the control registers and I/O pins. The external buffer and buffer control signals used must be changed to reconfigure the port from printer to scanner mode. This can be done either with external jumpers (requires opening of the PC case and manual intervention) or with two gates controlled by the game port decode pin (requires execution of setup software) or another decoder output. Note that this external hardware (jumpers or gates) is only required in the case where the configuration (printer or scanner) is to be software selectable.

The printer interface utilizes Centronics-compatible pin definitions. The scanner interface uses Centronics-like pin definitions which can be used to drive a RICOH IS30 scanner or equivalent.

Printer Interface

To permit the parallel port to properly drive a Centronics-compatible interface, LS05 open-collector buffers should be used with CHIPSpak control output pins to ensure sufficient drive capacity and to minimize the likelihood of electrostatic discharge (ESD) problems. The LS05 output lines should be

Table 5 Divisor Register Values for Various Baud Rates

	1.8432 MHz Crystal		3.072 MHz Crystal	
Baud Rate	Divisor Register Value	% Error Desired vs. Actual	Divisor Register Value	% Error Desired vs. Actual
50	2304	none	3840	none
75	1536	none	2560	none
110	1047	0.026	1745	0.026
134.5	857	0.058	1428	0.034
150	768	none	1280	none
300	384	none	640	none
600	192	none	320	none
1200	96	none	160	none
1800	64	none	107	0.312
2000	58	0.69	96	none
2400	48	none	80	none
3600	32	none	53	0.628
4800	24	none	40	none
7200	16	none	27	1.23
9600	12	none	20	none
19200	6	none	10	none
38400	3	none	5	none
56000	2	2.86	—	—

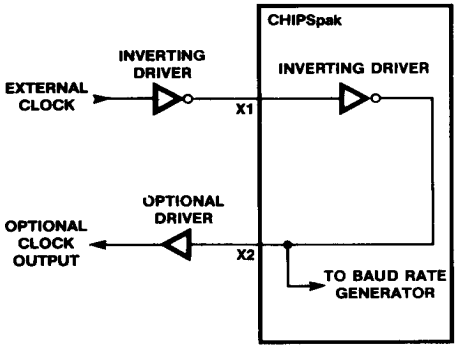


Figure 3. UART Clock Provided by an External Clock

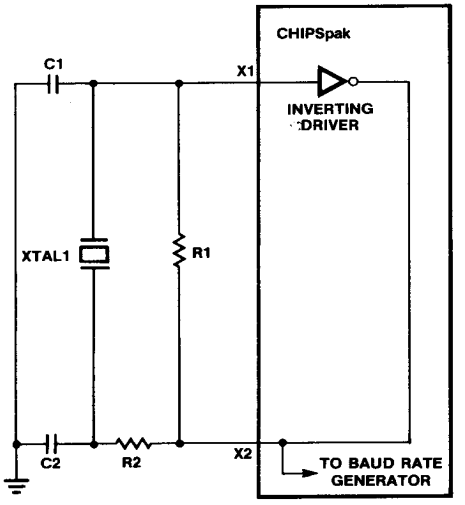


Figure 4. UART Clock Provided by a Crystal

Table 6 Resistor and Capacitor Values for Oscillator Network

Crystal Frequency	R1	R2	C1	C2
1.8 MHz	1M Ohm	1.5K Ohm	10-30 pF	40-60 pF
3.1 MHz	1M Ohm	1.5K Ohm	10-30 pF	40-60 pF

pulled up to +5V through 4.7K resistors. CHIPSpak Data outputs should be isolated with a non-inverting buffer (LS244). CHIPSpak Control inputs pins are assumed to be isolated with an inverting buffer (LS04, LS240 or Schmitt trigger LS14). A typical interface is shown in Figure 5.

Printer Interface Accessible Registers

Figure 6 depicts the registers and I/O ports which are accessible for the parallel printer port. These are compatible with the the IBM PC parallel port. Bit definitions for each of these registers are given after the diagram. All addresses are offsets from the base address for the parallel port specified during the CHIPSpak configuration process. Additional instructions regarding setup times and pulse widths are meant for use with Centronics-compatible interfaces. Bit definitions in Figure 6 labeled R are reserved.

Data Latch

This read/write register is located at an offset of 0H from the base address of the parallel port. Data written to this register is transmitted to the printer. Data read from this port is identical to that which was last written.

Printer Status Register

This read-only register is located at an offset of 1H from the base address of the parallel port. Bit definitions are as follows:

Bit 7: BS—Busy. This bit reflect the state of the CHIPSpak BUSY input pin. A 0 means that the printer is busy and cannot accept data. A 1 indicates that the printer is ready to accept data.

Bit 6: AK—Acknowledge. This bit reflects the state of the ACK input pin. A 0 means that the printer has received a character and is

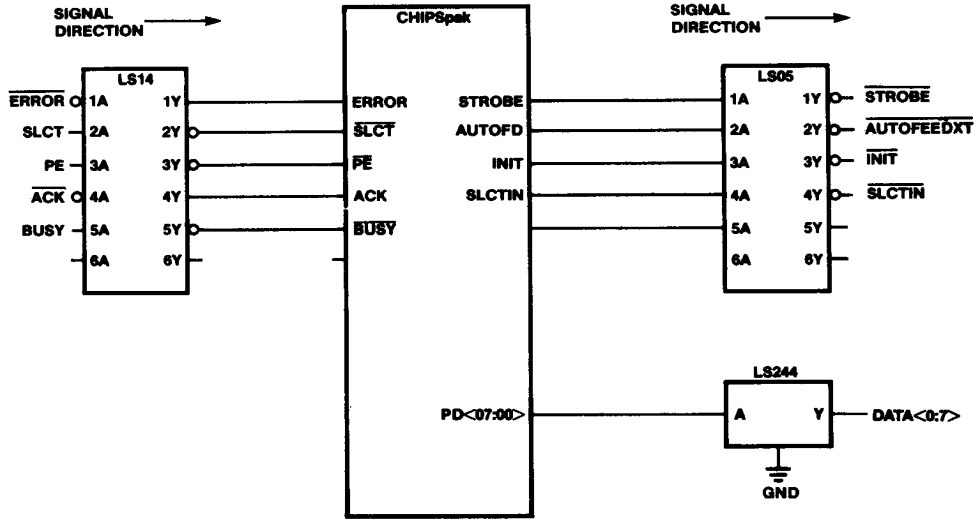


Figure 5: Printer Only Configuration.

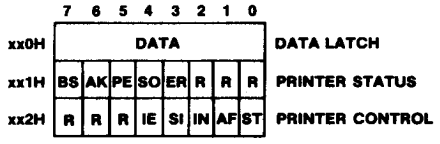


Figure 6: Parallel Port Accessible Registers

ready to accept another. A 1 means that it is still reading the last character sent.

Bit 5: PE—Paper Empty. This bit reflects the state of the CHIPSpak $\overline{PE}$ input pin. A 1 indicates a paper end condition. A 0 indicates the presence of paper.

Bit 4: SO—SLCT. This bit reflects the state of the CHIPSpak $\overline{SLCT}$ input pin. A 1 means the printer is online. A 0 means it is deselected.

Bit 3: ER—ERROR. This bit reflects the inverted state of the CHIPSpak ERROR input pin. A 0 means that an error condition has been detected. A 1 indicates no errors.

Bits 2-0: Reserved.

Printer Controls Register

This read/write register is located at an offset of 2H from the base address of the parallel port. Bit definitions are:

Bits 7-5: Reserved. Reset to 0.

Bit 4: IE—IRQ Enable. This bit is used to enable or disable interrupts resulting from the printer ACK signal. A 1 enables interrupts so that when ACK is not asserted by the printer, the CPU will be interrupted on the IRQ line specified in the CHIPSpak configuration RAM. Reset to 0.

Bit 3: SI—SLCTIN. Used to drive the CHIPSpak SLCTIN output pin. A 1 selects the printer. Reset to 0.

Bit 2: IN—Init. Used to control the CHIPSpak INIT output pin. A 0 (active low) starts the printer (50 μS pulse minimum). Reset to 0. Note that the INIT output pin is an inversion of this bit.

Bit 1: AF—Auto Feed. Used to control the CHIPSpak AUTOFD output pin. A 1 causes the printer to line feed after each line is printed. Reset to 0.

Bit 0: ST—Strobe. Used to control the CHIPSpak STROBE output pin. A 1 in this bit generates the active high pulse (0.5 μS pulse minimum) which is required to clock data into the printer. There is a 0.5 μS data setup time requirement before STROBE can be asserted. Reset to 0.

Scanner Interface

The CHIPSpak can drive the Centronics-like parallel interface used by the RICOH IS30 scanner. The parallel port is configured as a scanner interface by setting bit 6 in the CHIPSpak Configuration Register. This interface is similar to the standard Centronics interface commonly used for parallel printers. CHIPSpak control output pins should be buffered from the connector with LS05 open-collector drivers to ensure sufficient drive capacity and to minimize the likelihood of ESD problems. The LS05 output lines must be pulled up to +5V with 4.7K resistors. Bi-directional data pins should be isolated by a non-inverting buffer (LS245). Status and control inputs from the scanner are assumed to be isolated by an inverting buffer (LS04, LS240 or Schmitt trigger LS14).

The external buffers required for a typical scanner interface are shown in Figure 7.

A comparison of the signals used in a Centronics-compatible printer interface and in the Ricoh IS30 scanner interface is given in the table below. Pin numbers refer to those of the 36 pin connector normally used with a Centronics-compatible interface. The polarity of signals is that to be found at the connector (after buffering and possibly inverting the CHIPSpak input or output pins).

Scanner Interface Accessible Registers

The following registers and I/O ports are accessible when the CHIPSpak parallel port is configured for use with a scanner (see the section entitled "Configuration Sequence" for details). These are a subset of those used in the IBM PC parallel port definition. The function of the SLCTIN and AUTOFD signals has been redefined to control the operation of an external bidirectional buffer. A summary of the registers accessible when the parallel port is defined for scanner use is depicted in Figure 8. Descriptions of the use of each of the bits in these registers follows Figure 8.

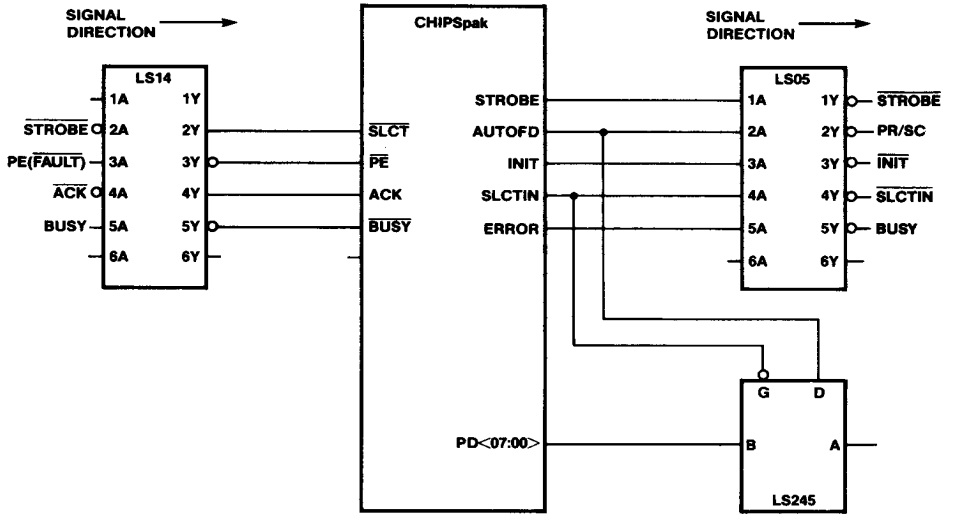


Figure 7: Scanner Only Configuration.

Table 7 Centronics-compatible Connector Pinout vs RICOH IS30 Pinout

Pin(s)	Dir	Printer	Dir	Scanner	Comments
1	O	STROBE	I/O	STROBE	
2-9	I/O	DATA<0:7>	I/O	DATA<0:7>	
10	I	ACK	I	ACK	
11	I	BUSY	I/O	BUSY	
12	I	PE	I	unused	
13	I	SLCT	—	FAULT	
14	O	AUTOFD	—	unused	generate PR/SC
15	I	unused	I	PR/SC	generated by AUTOFD
31	O	INIT	I	RESET	
32	I	ERROR	—	unused	
36	O	SLCTIN	—	unused	Buffer Enable

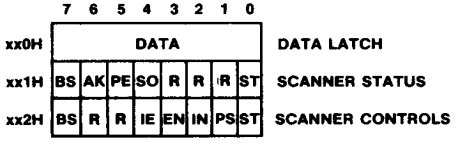


Figure 8:
Parallel Scanner Accessible Registers.

Data Latch

This read/write register is located at an offset of 0H from the base address of the parallel port. Data written to this register is transmitted to the scanner. Data read from this register is received from the scanner. CHIPSpak pins PD<07:00> are controlled by accessing this register.

Scanner Status Register

This read-only register is located at an offset of 1H from the base address of the parallel port. Bit definitions are:

Bit 7: BS—Busy. A 0 in this bit when the scanner is in print mode means the scanner is busy and cannot accept data.

Bit 6: AK—acknowledge. A 0 in this bit means that the scanner has received a character and is ready to accept another. A 1 indicates that the scanner is still reading the last character sent.

Bit 5: PE—FAULT. A 0 indicates that an error exists. This bit reflects the state of the CHIPSpak PE input pin.

Bit 4: SO—SLCT. A 1 in this bit means the scanner is selected. A 0 means it is deselected.

Bits 3-1: Reserved.

Bit 0: ST—Strobe. This bit is used to read the value of the scanner's STROBE signal which is connected to the CHIPSpak SLCT pin. It has the same polarity as the CHIPSpak SLCT pin (i.e. if the SLCT pin is a 0 this bit will be a 0). The scanner asserts STROBE (forcing this bit to a 1 state) to indicate that valid data is available.

Scanner Controls Register

This read/write register is located at an offset of 2H from the base address of the parallel port. Bit definitions are:

Bit 7: BS—Busy. This bit drives the CHIPSpak ERROR pin which is configured as an output in scanner mode. Writing a 1 to this bit sends a BUSY signal to the scanner indicating that the CPU has not yet read the last byte written by the scanner during a transfer from scanner to host.This bit should be set to 0 when not used. Reset to 0.

Bits 6-5: Reserved.

Bit 4: IE—IRQ Enable.This bit is used to enable interrupts. A 1 enables an interrupt to be generated when the scanner deasserts its ACK signal. Reset to 0.

Bit 3: EN—Enable buffer. This bit is gated to the CHIPSpak SLCTIN output pin. This output pin should be connected to the enable pin of a bidirectional LS245 type buffer. A 1 in this bit can then be used to disable the LS245 buffer before the data transfer direction (from scanner to CHIPSpak or vice versa) is changed (using the PR/$\overline{SC}$ bit). By doing so, bus contention problems will be eliminated. Reset to 0.

Bit 2: IN—Init. This bit drives the CHIPSpak INIT output pin. A 0 written here resets the scanner (100μS pulse minimum). Reset to 0.

Bit 1: PS—Print/$\overline{Scan}$. This bit is gated to the CHIPSpak AUTOFD output pin which should be connected to the direction pin of a bidirectional LS245 type buffer. In addition, AUTOFD should be buffered and transmitted to the scanner as the PR/$\overline{SC}$ signal (pin 15 of a Centronics-compatible connector). A 1 in this register causes the LS245 buffer to transmit from PC to scanner, a 0 from scanner to PC. Caution should be exercised to disable the buffer (by using the Enable buffer bit; see Bit 3 above) while the direction is being changed. Reset to 0.

Bit 0: ST—Strobe. This bit connects to the CHIPSpak STROBE output pin. A 1 in this bit is used to generate the active high pulse (1.8 μS wide minimum) which clocks data into the scanner. Data should be setup 0.3 μS before STROBE is asserted. Reset to 0.

Printer/Scanner Connections

It is possible to have a CHIPSpak drive both a printer and a scanner interface, although only one may be active at a time. External jumpers or configuration logic must be provided to change the connections in a system designed to support either a scanner or a Centronics-compatible printer. A comparison of the external buffers required for printer and/or scanner interfaces is shown in Figure 9.

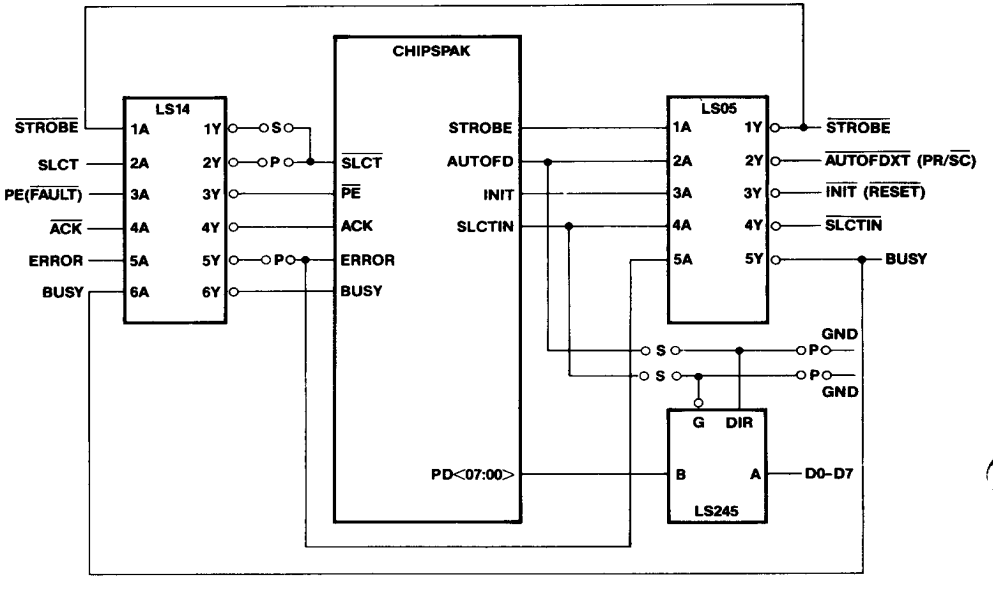


Figure 9: Printer/Scanner Configuration.

REAL TIME CLOCK (82C606 ONLY) FUNCTIONAL DESCRIPTION

This section of the 82C606 combines a complete time-of-day clock with alarm, one hundred year calendar, a programmable periodic interrupt, and 114 bytes of low power static RAM. Provisions are made to enable the device to operate in a low power (battery powered) mode and protect the contents of both the RAM and clock during system power-up and power-down.

The 82C605 does not include the Real Time Clock.

Register Access

Reading and writing to the 128 locations in the Real Time Clock is accomplished by first placing the Index Address of the location you wish to access on the data input pins XD0-XD6. The address will then be latched into the Index Address Register on the trailing edge of $\overline{IOW}$. The Index Address Register is then used as a pointer to the specific byte in the Real Time Clock, which may be read or written to by asserting $\overline{XIOR}$ or $\overline{XIOW}$ with with an address on the XA9-XA0 inputs of 2C1H.

Since AS will most likely be generated by an I/O operation which will result in the assertion of $\overline{XIOW}$, it is recommended that an address of 2C0H be applied to the XA9-XA0 inputs during this time. This will prevent the modification of other registers in the 82C606.

Address Map

Figure 10 illustrates the internal register/RAM organization of the Real Time Clock portion of the 82C606. The 128 addressable locations in the Real Time Clock are divided into 10 bytes which normally contain the time, calendar, and alarm data, four control and status bytes and 114 general purpose RAM bytes. All 128 bytes are readable by the CPU. The CPU may also write to all locations except Registers C, D, Bit 7 of Register A and Bit 7 of the Seconds Byte which is always 0.

Index	Function
00	SECONDS
01	SECONDS ALARM
02	MINUTES
03	MINUTES ALARM
04	HOURS
05	HOURS ALARM
06	DAY OF WEEK
07	DATE OF MONTH
08	MONTH
09	YEAR
0A	REGISTER A
0B	REGISTER B
0C	REGISTER C
0D	REGISTER D
0E	USER RAM
0F	USER RAM
.	
.	
.	
7E	USER RAM
7F	USER RAM

Figure 10. Address Map for Real Time Clock

Time Calendar and Alarm Bytes

The CPU can obtain the time and calendar information by reading the appropriate locations in the Real Time Clock. Initalization of the time, calendar and alarm information is accomplished by writing to these locations. Information is stored in these locations in binary-coded decimal (BCD) format.

Before initalization of the internal registers can be performed, the SET bit in Register B should be set to a "1" to prevent Real Time Clock updates from occuring. The CPU then initalizes the first 10 locations in BCD format. The SET bit should then be cleared to allow updates. Once initalized and enabled, the Real Time Clock will perform Clock/Calendar updates at a 1 Hz rate.

Index Register Address	Function	BCD Range
0	Seconds	00-59
1	Seconds Alarm	00-59
2	Minutes	00-59
3	Minutes Alarm	00-59
4	Hours (12 hour mode)	01-12 (AM) 81-92 (PM)
	Hours (24 hour mode)	00-23
5	Hours Alarm (12 hour mode)	01-12 (AM) 81-92 (PM)
	Hours Alarm (24 hour mode)	00-23
6	Day of Week Sunday = 01	01-07
7	Day of Month	01-31
8	Month	01-12
9	Year	00-99

Figure 11. Time, Calendar, Alarm Data Format

Figure 11 shows the format for the ten clock, calendar and alarm locations. The 24/12 bit in Register B determines whether the hour locations will be updated using a 1-12 or 0-23 format. After initalization the 24/12 bit cannot be changed without reinitalizing the hour locations. In 12 hour format the high order bit of the hours byte in both the time and alarm bytes will indicate PM when it is a "1".

During updates, which occur once per second, the 10 bytes of time, calendar and alarm information are unavailable to be read or written by the CPU for a period of 2ms. These 10 locations cannot be written during this time. Information read while the Real Time Clock is performing an update will be undefined. The Update Cycle section shows how to avoid Update Cycle/CPU contention problems.

The alarm bytes can be programmed to generate an interrupt at a specific time or they can be programmed to generate a periodic interrupt. To generate an interrupt at a specific time, the user need only program the time that the interrupt is to occur into the 3 alarm bytes. Alternately, a periodic interrupt can be generated by setting the high order two bits in an alarm register to a "1", which turns that byte into a "don't care". For instance, an interrupt can be generated every hour by programming a C0H into Register 5, or an interrupt can be generated once a second by programming the same value into all three alarm registers.

Static RAM

The 114 bytes of RAM from Index Address 0EH to 7FH are not affected by the Real Time Clock. These bytes are accessable during the update cycle and may be used for whatever the designer wishes. Typical applications will use this as nonvolatile storage for configuration and calibration parameters since this device is normally battery powered when the system in turned off.

Control and Status Registers

The 82C606 contains four registers used to control the operation and monitor the status of the Real Time Clock. These registers are located at Index Address 0AH-0DH and are accessable by the CPU at all times.

REGISTER A (0AH)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

(Read/Write register except UIP)

UIP—Update in progress flag is a status bit used to indicate when an update cycle is about to take place. A "1" indicates that an update cycle is taking place or is imminent. UIP will go active (High) 244us prior to the start of an update cycle and will remain active for an additional 2ms while the update is taking place. The UIP bit is read only and is not affected by Reset. Writing a "1" to the SET bit in Register B will clear the UIP status bit.

DV2-DV0—These three bits are used to control the Divider/Prescaler on the Real Time Clock. While the 82C606 can operate at frequencies higher than 32.768 Khz, this is not recommended for battery powered operation due to the increased power consumption at these higher frequencies.

DV2	DV1	DV0	OSCI Freq.	Mode
0	0	0	4.194304MHz	Operate
0	0	1	1.048576MHz	Operate
0	1	0	32.768KHz	Operate
1	1	X	Reset Divider	

Divider Options

RS3-RS0—These four bits control the Periodic Interrupt rate. The Periodic interrupt is derived from the Divider/Prescaler in the Real Time Clock and is separate from the Alarm Interrupt. Both the alarm and periodic interrupts do however, use the same interrupt channel in the Interrupt Controller. Use of the Periodic Interrupt allows the generation of interrupts at rates higher than once per second. Below are the interrupt rates for which the Real Time Clock can be programmed.

REGISTER B (0BH)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	0	BIN/$\overline{\text{BCD}}$	24/$\overline{12}$	DSE

(Read/Write Register)

SET—Writing a "0" to this bit enables the Update Cycle and allows the Real Time Clock to function normally. When set to a "1" the Update Cycle is inhibited and any cycle in progress is aborted. The SET bit is not affected by the $\overline{\text{RESET}}$ input pin.

Rate Selection				Time Base	
RS3	RS2	RS1	RS0	4.194304 MHz 1.048576 MHz	32.768 KHz
0	0	0	0	None	None
0	0	0	1	30.517 μs	3.90526 ms
0	0	1	0	61.035 μs	7.8125 ms
0	0	1	1	122.070 μs	122.070 μs
0	1	0	0	244.141 μs	244.141 μs
0	1	0	1	488.281 μs	488.281 μs
0	1	1	0	976.562 μs	976.562 μs
0	1	1	1	1.953125 ms	1.953125 ms
1	0	0	0	3.90625 ms	3.90625 ms
1	0	0	1	7.8125 ms	7.8125 ms
1	0	1	0	15.625 ms	15.625 ms
1	0	1	1	31.25 ms	31.25 ms
1	1	0	0	62.5 ms	62.5 ms
1	1	0	1	125 ms	125 ms
1	1	1	0	250 ms	250 ms
1	1	1	1	500 ms	500 ms

Periodic Interrupt Rate

PIE—The Periodic Interrupt Enable Bit controls the generation of interrupts based on the value programmed into the RS3-RS0 bits of Register A. This allows the user to disable this function without affecting the programmed rate. Writing a "1" to this bit enables the generation of periodic interrupts. This bit is cleared to a "0" by Reset.

AIE—The generation of alarm interrupts is enabled by setting this bit to a "1". Once this bit is enabled the Real Time Clock will generate an alarm whenever a match occurs between the programmed alarm and clock information. If the don't care condition is programmed into one or more of the Alarm Registers, this will enable the generation of periodic interrupts at rates of one second or greater. This bit is cleared by Reset.

UIE—Update Interrupt Enable bit enables UF (Update Flag) in Register C to assert IRQ. This bit is cleared by RESET pin going low, or SET bit (Reg. B bit-7) going high.

BIN/BCD—When this bit is high, registers 0-9 are in Binary mode. If it is low (default), registers 0-9 are in BCD mode.

24/12—The 24/12 control bit is used to establish the format of both the Hours and Hours Alarm bytes. If this bit is a "1", the Real Time Clock will interpret and update the the information in these two bytes using the 24 hour mode. This bit can be read or written by the CPU and is not affected by Reset.

DSE—The Real Time Clock can be instructed to handle daylight savings time changes by setting this bit to a "1". This enables two exceptions to the normal time keeping sequence to occur. On the last Sunday in April **AM. Setting this bit to a "0" disables the execution of these two exceptions. PSRSTB has no affect on this bit.**

REGISTER C (0CH)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

(Read only register)

IRQF—The Interrupt Request Flag bit is set to a "1" when any of the conditions which can cause an interrupt is true and the interrupt enable for that condition is true. The condition which causes this bit to be set, also generates an interrupt. The logic expression for this flag is:

IRQF = PF & PIE
+ AF & AIE
+ UF & UIE

This bit and all other active bits in this register are cleared by reading the register or by activating the PSRSTB/ input pin. Writing to this register has no affect on the contents.

PF—The Periodic Interrupt Flag is set to a "1" when a transition, which is selected by RS3-RS0, occurs in the divider chain. This bit will become active, independent of the condition of the PIE control bit. The PF bit will then generate an interrupt a nd set IRQF if PIE is a "1".

AF—A "1" appears in the AF bit whenever a match has occured between the time registers and alarm registers during an update cycle. This flag is also independent of it's enable (AIE) and will generate an interrupt if AIE is true.

REGISTER D (0DH)

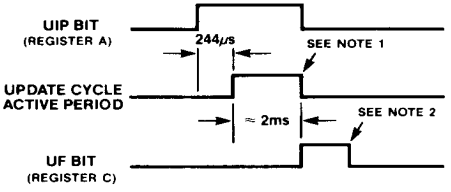
msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

(Read only register)

VRT—The Valid RAM and Time Bit indicates the condition of the contents of the Real Time Clock. This bit is cleared to a "0" whenever the PS input pin is LOW. This pin is normally derived from the power supply which supplies Vcc to the device and will allow the user to determine whether the registers have been initalized since power was applied to the device. PSRSTB has no affect on this bit and it can only be set by reading Register D.All unused register bits will be "0" when read and are not writable.

Update Cycle

During normal operation the Real Time Clock will perform an update cycle once every second. The performance of an update cycle is contingent upon the divider bits DV2-DV0 not being cleared, and the SET bit in Register B cleared. The function of the update cycle is to increment the clock/calendar registers and compare them to the Alarm Registers. If a match occurs between the two sets of registers, an alarm is issued and an interrupt will be issued if the alarm and interrupt control bits are enabled.



NOTE:
1. REGISTERS 0-9 ARE UNAVAILABLE TO BE READ OR WRITTEN DURING THIS TIME.
2. UF BIT CLEARED BY CPU READ OF REGISTER C.

Figure 12. Update Cycle

During the time that an update is taking place, the lower 10 registers are unavailable to the CPU. This is done to prevent the possible corruption of data in the registers or the reading of incorrect data. To avoid contention problems between the Real Time Clock and the CPU, a flag is provided in Register A to alert the user of an impending update cycle. This Update In Process Bit (UIP) is asserted 244μs before the actual start of the cycle and is maintained until the cycle is complete. Once the cycle is complete the UIP bit will be cleared and the Update Flag (UF) in Register C will be set. Figure 12 illustrates the update cycle. CPU access is always allowed to Registers A through D during update cycles.

Two methods for reading and writing to the Real Time Clock are recommended. Both of these methods will allow the user to avoid contention between the CPU and the Real Time Clock for access to the time and date information.

The first method is to read Register A, determine the state of the UIP bit and if it is "0", perform the read or write operation. For this method to work successfully the entire read or write operation (including any interrupt service routines which might occur) must not require longer than 244μs to complete from the beginning of the read of Register A to the completion of the last read or write operation to the Clock Calendar Registers.

The second method of accessing the lower 10 registers is to read Register C once and disregard the contents. Then subsequently continue reading this register until the UF bit is a "1". This bit will become true immediately after an update has been completed. The user then has until the start of the next update cycle to complete a read or write operation.

Power-Up/Down

Most applications will require the Real Time Clock to remain active whenever the system power is turned off. To accomplish this the user must provide an alternate source of power to the 82C606. This alternate source of of power is normally provided by connecting a battery to the Vcc supply pin of the device. A means should be provided to switch from the system power supply to the battery. A circuit such as the one shown in Figure 13 may be used to eliminate power drain on the battery when the entire 82C606 is active. The The circuit shown here will allow for reliable transitions between system and battery power without undue battery power drain.

The user should also ensure that the Vin maximum specification is never exceeded when powering the system up or down. Failure to observe this specification may result in damage to the device.

A pin is provided on the device to protect the contents of the Real Time Clock and reduce power consumption whenever the system is powered down. This pin (STBY)

should be low whenever the system power supply or on the system board. The STBY operation of the system. This signal may be generated by circuitry in either the power supply or on the system board. The STBY input will disable all unnecessary inputs during the time the system is powered down to prevent noise on the inactive pins from causing increased Icc. This pin must therefore be inactive for the remainder of the device to operate properly when system power is applied.

One pin is provided to initalize the device whenever power is applied to the 82C606. This pin ($\overline{PS}$) will not alter the RAM or Clock/Calendar contents but it will initialize the necessary control register bits. (See Pin Description for a list of the control register bits affected by $\overline{PS}$) Assertion of $\overline{PS}$ disables the generation of interrrupts and sets a flag indicating that the contents of the device may not be valid. A sample circuit for controlling the $\overline{PS}$ input is shown in Figure 13.

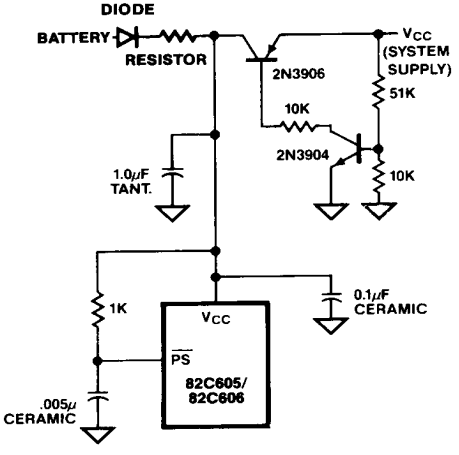


Figure 13. Power Conversion and Reset Circuitry

GAME PORT DECODER

A decoder output is provided for use with game port logic. The game port is assumed to be implemented externally using an NE558 Quad Monostable, an LS244 buffer and resistors and capacitors. Read and write enable signals must be generated with external OR gates Figure 14 shows a typical Game Port circuit.

POWER SUPPLIES

The CHIPSpak has provisions for Standby (battery) and Auxiliary (derived from an external regulated supply such as a telephone line or RS-232C link) power in addition to +5V coming from the Main power supply. An external PNP transistor or Schottky diode switch should be used for switching the CHIPSpak VDD pins from one supply source to another if either or both of these options are used. The switch should have an ON voltage drop less than a silicon diode to reduce the risk of latchup in the CHIPSpak. Latchup can occur when CHIPSpak inputs are driven with voltage levels which are greater than VDD by one silicon diode voltage drop. To prevent latchup, the VDD pin of the CHIPSpak should be no more than 0.4 volts below the VDD or VCC pins of devices whose outputs drive CHIPSpak inputs.

Power can be supplied from one of three possible sources:

Main: the normal +5V from the system power supply.

Auxiliary: an external regulated source typically derived from a phone line (reduced from the 55-110 volts available; some CMOS modems acquire their power this way) or RS-232C control signals (reduced from the +9 to +12 volts supplied; some mice use this as as a source of power).

Standby: Most commonly a NiCad or lithium battery. This is normally used to power only the Real Time Clock and to maintain the CMOS Configuration (static) RAM. The clocks to all other circuitry should be stopped to reduce power dissipation.

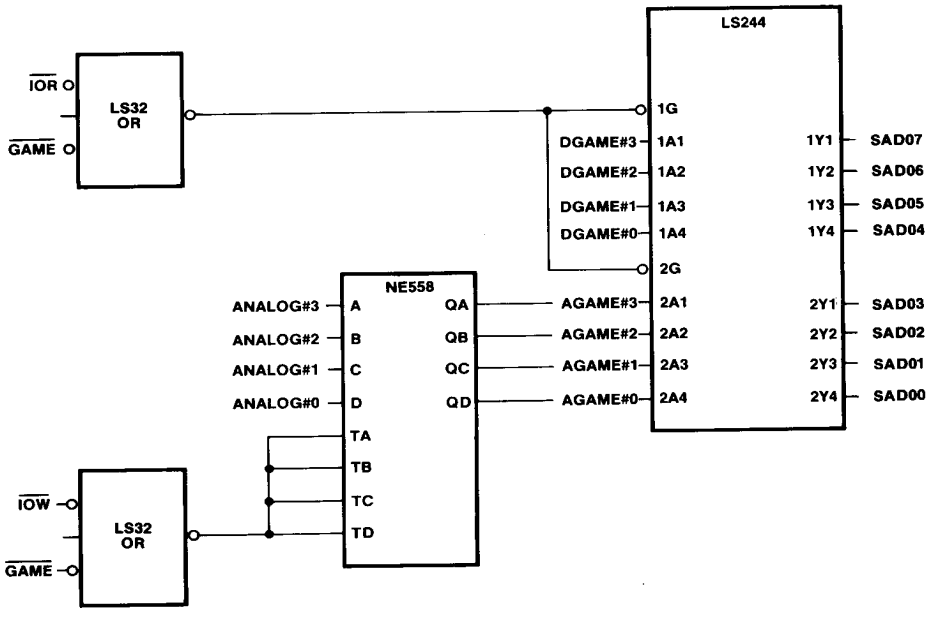


Figure 14. Typical Game Port Circuit

Note that by providing for an auxiliary supply the CHIPSpak serial ports can continue to operate while waiting for a wake-up character to be received. This wake-up character can then generate an interrupt which initiates a CPU powerup or wake-up sequence. In this manner battery-powered remote controllers can respond to requests for status or service.

So long as VDD is supplied to the CHIPSpak, the Configuration RAM will be maintained. All other CHIPSpak circuitry can be selectively enabled or disabled via bits in the Configuration RAM.

Standby Mode Operation

The 82C606 enters standby mode when $\overline{STBY}$ is asserted. In this mode of operation with VDD supplied by back-up power, some signals are forced into the default states as defined below:

1. $\overline{GAME}$, STROBE, AUTOFD, INIT, and SLCTIN are forced low,
2. $\overline{DBEN}$, and $\overline{ABENB}$ are forced into high impedance,
3. PD<07:00>, and ERROR are forced into input state,
4. IRQ3, IRQ4, IRQ5, IRQ7, TXD1, $\overline{RTS1}$, $\overline{DTR1}$, TXD2, $\overline{RTS2}$, $\overline{DTR2}$ are forced to output low if the Baud Rate Oscillator Enable field (bit 6 and bit 5) of the configuration register 00H is not set to zero, otherwise these signals are determined by the programming control of the UARTS.

CONFIGURATION REQUIREMENTS AND OVERVIEW

A significant portion of the 82C606 circuitry is used for configuration, all of which can be performed under software control. This permits user-friendly (probably menu-driven) CHIPSpak configuration using setup utilities provided with the card or system containing the CHIPSpak. DIP switches and jumpers can thus be eliminated meaning that it should no longer necessary to open the chassis to change the configuration of a peripheral.

Since the CHIPSpak is software configured, a setup program must be run any time its configuration is changed. This process entails placing the CHIPSpak in configuration mode and setting the on-chip configuration registers. The following configuration issues must be considered:

- The existence of multiple CHIPSpaks in a system.
- The existence of other peripheral adapters performing the same functions as those on the CHIPSpak (for instance providing serial or parallel ports).

When configuring a board containing a CHIPSpak, the following steps must be taken:

1. Disable all system-resident CHIPSpaks.
2. Determine the configuration of the rest of the system including the existence and I/O address locations for other serial, parallel and game port adapters and other Real Time Clocks.
3. Determine the number of CHIPSpaks in the system.
4. Establish an access port for the CHIPSpak whose address does not conflict with that of any other adapters.
5. Enable configuration mode for one of the CHIPSpaks.
6. Configure the CHIPSpak which is currently in configuration mode.
7. Disable configuration mode in the CHIPSpak just configured. Normal operation of this CHIPSpak will commence automatically.
8. Repeat steps 5 through 7 above for all other CHIPSpaks in the system.

Configuration Sequence

In order to setup or change the configuration of a CHIPSpak, two consecutive I/O addresses (one even and one odd; these should not conflict with any existing devices) are used to select and access the internal configuration registers. The configuration sequence has deliberately been made convoluted to prevent accidental changes to the CHIPSpak configuration by an errant program. Any deviation from the sequence described below will cause the configuration state machine to return to its initial idle state.

By IBM PC convention, I/O addresses 3F8-3FFH and 2F8-2FFH are reserved for COM1 and COM2 respectively. The Interrupt Flag Register (IFR), located by default at 2FAH or 3FAH in each CHIPSpak, is normally read-only. Writes to these locations are tolerated by CHIPSpaks, and they should present no problem for resident NS16450 or INS8250A UARTs. Note that there are special considerations when using more than one CHIPSpak in a single system. See below for more details.

To identify a CHIPSpak the following sequence is used:

1. Write a KEY<07:00> byte to COM2 IFR (address 2FAH)
2. Write a $\overline{\text{KEY}}$<07:00> byte to COM1 IFR (address 3FAH)
3. Write a 36H (ASCII 6; the part number) to COM1 IFR (address 3FAH)

   Where: KEY is a single byte with a value other than 00H or FFH, and $\overline{\text{KEY}}$ is the complement of KEY

   The aforesaid writes must be consecutive; no intervening writes to 2FAH or 3FAH

are allowed. Any data written other than that specified above will reset the configuration state machine and require the program to start again.

Each CHIPSpak will compare the data written to both IFR ports. If the data is complementary, the CHIPSpaks will be disabled and will not respond to any I/O addresses other than those used in configuration mode. This scheme prevents conflicts during the I/O configuration process. Only the configuration logic in the CHIPSpak will be enabled.

4. Determine whether other devices are present which conflict with with the CHIPSpak's facilities. For instance, are there other serial or parallel ports in the system? Pick a pair of consecutive, non-conflicting I/O addresses to use for the Configuration Register Index port (CRI; the EVEN and LOWER address) and the Configuration Access Port (CAP; the ODD and HIGHER address). Note that system address bit 1 (SAD <01>) must be at a logic 0 level to address the CRI and CAP. Thus 00H (for the CRI) and 01H (for the CAP port) or 04H and 05H are valid addresses, while 02H (for the CRI) and 03H (for the CAP port) are not.

5. Write the <CRI address divided by 4> to the COM1 IFR (address 3FAH).

   Where: <CRI address> is the I/O address of the CRI.

6. Write the <CRI address divided by 4 inverted> to the COM2 IFR (address 2FAH).

   Where: <CRI address inverted> is the complement of the I/O address of the CRI.

   The CHIPSpaks will compare the data written to the two IFR ports. If the two addresses written are complements of one another, configuration mode will be entered and the CRI and CAP will respond at the designated addresses.

   Bits <07:04> of the CRI are used to select the configuration registers in one of up to 4 system-resident CHIPSpaks. A 1 in bit <04> selects unit 0, a 1 in bit <05> selects unit1,etc. It is possible to select multiple units simultaneously by setting more than one bit. Enabling more than one CHIPSpak should not cause any problems when performing writes. Reading from multiple units could cause data bus contention problems. If bits<07:04> are zero or the configuration pin is not connected to one of SAD<07:04> then no CHIPSpaks will respond.

   Bits <03:00> of the CRI specify the address of the configuration register to be read or written.

7. Set the CRI to xFH and read the CAP. The correct response is the most significant 8 bits of the CRI address. This will verify the existence of a CHIPSpak at that address. Reading 8FH, 4FH, 2FH and 1FH will indicate how many CHIPSpaks are resident and must be configured.

8. Proceed to set the base addresses of all the peripherals in the CHIPSpaks. These will typically be specified by a user responding to setup program prompts. Also set the CHIPSpak options controlled by the Configuration RAM (interrupts, port configurations, etc.).

   Note that a write to the CRI port must precede every access to the CAP. Multiple CRI writes will not cause any problems; the last CRI address written will be used to access data through the CAP.

9. Set the CRI to xFH and write any value to the CAP to terminate configuration mode of the specified CHIPSpak and cause it to commence normal operation.

Configuration Registers

There are 10 configuration registers in the 82C606 which must be initialized. Settings are retained as long as standby power is maintained. These registers are not affected by the RESET signal and are set to their default state only when the PS pin becomes

active. Standby power is assumed to be in use when the STBY pin becomes active. Figure 15 below depicts the configuration registers in the 82C606. After Figure 11 are the definitions for each of the bits in the 82C606 configuration registers.

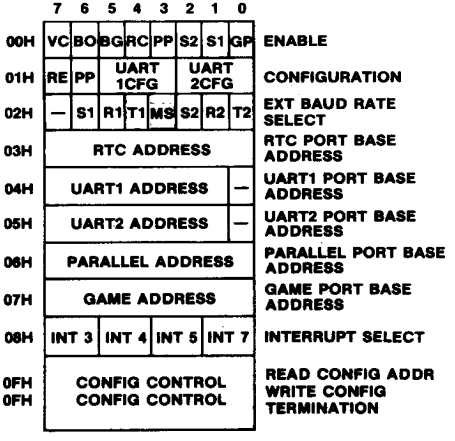


Figure 15. Configuration Registers

Enable Register

This read/write register is located at CRI offset 0H. Bit definitions are as follows:

Bit 7: Valid Configuration. This bit indicates that a valid configuration cycle has taken place. The configuration software should set this bit to 1 after it has initialized the required configuration registers.

Value	Definition
0	Invalid Configuration indicates that power has been applied to the CHIPSpak but the configuration registers have not yet been fully initialized. Asserting PS causes this bit to be set to 0. A reset from the RESET pin has no effect on this bit.
1	Valid Configuration indicates that the configuration software has initialized all necessary configuration registers since the last time power was applied to the CHIPSpak.

Bit 6-5: BO—Enable Baud Rate Oscillator; Read/Write. The default value is 0.

Value	Function
0	Oscillator ON, BR Generator Clock ENABLED In this state the oscillator and baud rate generator clock are always enabled and are not shut off due to removal of the main power supply (STBY pin became active). The presence of a power supply other than a (low capacity) battery (needed for the RTC) is assumed. This is due to the fact that serial port operation (in particular the oscillator) consumes more power than many of the other CHIPSpak circuits.
1	Oscillator ON, BR Generator Clock ENABLED In this state, the oscillator and BR Generator clock are ON and ENABLED respectively as long as the STBY pin is inactive. When STBY becomes active, these two are shut down.
2	Oscillator ON, BR Generator Clock DISABLED In this state the oscillator is ON as long as the STBY pin is inactive. When STBY becomes active, the oscillator is shut off. The BR generator clock is always disabled.
3	Oscillator OFF, BR Generator Clock DISABLED

Bit 4: RC—Enable Real Time Clock (RTC); Read/Write. A 1 in this bit enables the RTC.

For the 82C605 CHIPSpak, this bit must be programmed to 0, which is also the default value on RESET.

Bit 3: PP—Enable Parallel Port; Read/Write. A 1 in this bit enables the Parallel Port. The default is disabled.

Bit 2: S2—Enable UART2; Read/Write. A 1 in this bit enables UART2. The default is disabled.

Bit 1: S1—Enable UART1; Read/Write. A 1 in this bit enables UART1. The default is disabled.

Bit 0: GP—Enable Game Port; Read/Write. A 1 in this bit enables the Game Port. The default is disabled.

Configuration Register

This read/write register is located at CRI offset 01H. Bit definitions are as follows:

Bit 7: Reset Control. This bit determines the manner in which the RESET pin affects the serial ports and RTC. Default is normal RESET.

Value	Function
0	Normal RESET. The CHIPSpak RESET input will cause a reset of all registers in the serial ports excluding the Receive Buffer, Transmit Buffer and Divisor Registers.
1	Restricted RESET. The RESET input will not reset the serial ports. This is used in applications where the CHIPSpak remains powered from an external supply while power to the remainder of the system is shut off. When the system power is restored, (most likely due to an interrupt when a character is received) it is desirable to have the state of the serial ports be unchanged.

Bit 6: Printer Port Operation. This bit defaults to 0.

Value	Definition
0	Normal, for printer only. Only data written to the CHIPSpak output data latch can be read back from the parallel port data output pins. An external LS244 buffer with its output always enabled should be connected to the PD<07:00> pins. The parallel port data register is defined for printer use. The ERROR pin is used as an input signal.
1	Bidirectional. Setting this bit to a logic 1 allows data to be read back through an external LS245 bidirectional buffer connected to the CHIPSpak PD<07:00> pins. The LS245 direction control should be driven by the AUTOFD pin. The LS245 enable control line should be driven from the CHIPSpak SLCTIN pin. The parallel port data register is defined for scanner use. The ERROR pin is used as an output signal.

Bit 5: Force UART1 $\overline{\text{CTS}}$ active. A 1 in this bit forces the CHIPSpak internal $\overline{\text{CTS1}}$ signal low. Default is disabled.

Bit 4: Force UART1 $\overline{\text{DSR}}$ active. A 1 in this bit forces the CHIPSpak internal $\overline{\text{DSR1}}$ signal low. Default is disabled.

Bit 3: Force UART1 $\overline{\text{DCD}}$ active. A 1 in this bit forces the CHIPSpak internal $\overline{\text{DCD1}}$ signal low. Default is disabled.

Bit 2: Force UART2 $\overline{\text{CTS}}$ active. A 1 in this bit forces the CHIPSpak internal $\overline{\text{CTS2}}$ signal low. Default is disabled.

Bit 1: Force UART2 $\overline{\text{DSR}}$ active. A 1 in this bit forces the CHIPSpak internal $\overline{\text{DSR2}}$ signal low. Default is disabled.

Bit 0: Force UART2 $\overline{\text{DCD}}$ active. A 1 in this bit forces the CHIPSpak internal $\overline{\text{DCD2}}$ signal low. Default is disabled.

External Baud Rate Select Register

This read/write register is located at CRI offset 2H. Bit definitions are as follows:

Bit 7: Reserved.

Bit 6: UART1 Divider. Divide external clock fed to CHIPSpak X1 pin by 2 or 4.

Value	Function
0	Divide by 2 (default)
1	Divide by 4

Bit 5: UART1 RX Clock Select.

Value	Function
0	Use baud rate generator output (default)
1	Use divider output

Bit 4: UART1 TX Clock Select.

Value	Function
0	Use baud rate generator output (default)
1	Use divider output

Bit 3: MS is the Mode Select option. When MS = 0 (default) the Interrupt signal corresponds to the 8250 interrupt mode. When MS = 1, the interrupt signal emulates the 16450A interrupt. The 8250 type interrupt is reset on reading the status-register (MSR or LSR), and is activated immediately if another interrupt is pending. In the 16450 emulation mode, the interrupt output remains active continuously until all pending interrupts are serviced.

Bit 2: UART2 Divider. Divide external clock fed to CHIPSpak X1 pin by 2 or 4.

Value	Function
0	Divide by 2 (default)
1	Divide by 4

Bit 1: UART2 RX Clock Select.

Value	Function
0	Use baud rate generator output (default)
1	Use divider output

Bit 0: UART2 TX Clock Select.

Value	Function
0	Use baud rate generator output (default)
1	Use divider output

Real Time Clock (RTC)
Port Base Address Register

This read/write register holds the base address of the RTC. It is located at CRI offset 3H. The eight bits in this register are compared with SAD<09:02> when the CHIPSpak is in normal operating mode to determine if the RTC Port is being addressed. To access the RTC, SAD<01> must be 0 and SAD<00> is used to select either the RTC address (index) or data port. The data port is selected when SAD<00> is a logic 0 while the address (index) port is selected when SAD<01> is a logic 1. Default setting of 2C0H.

UART1 Port Base Address Register

This read/write register holds the base address of UART1. It is located at CRI offset 4H. The high order seven bits in this one byte register are compared with SAD<09:03> when the CHIPSpak is in normal operating mode to determine if UART1 is being addressed. Nominal settings are 2F8H (COM2) or 3F8H (COM1). Default is 3F8H.

UART2 Port Base Address Register

This read/write register holds the base address of UART2. It is located at CRI offset 5H. The high order seven bits in this one byte register are compared with SAD<09:03> when the CHIPSpak is in normal operating mode to determine if UART 2 is being addressed. Nominal settings are 2F8H (COM2) or 3F8H (COM1). Default is 2F8H.

Parallel Port Base Address Register

This read/write register holds the base address of the parallel port. It is located at CRI offset 6H. The eight bits in it are compared with SAD<09:02> when the CHIPSpak is in normal operating mode to determine if the Parallel Port is being addressed. Nominal settings are 278H (LPT2) or 378H (LPT1). Default is 278H. (LPT1 is assumed to be on the monochrome adapter).

Game Port Base Address Register

This read/write register holds the base address of the game port. It is located at CRI offset 7H. The eight bits in it are compared with SAD<09:02> when the CHIPSpak is in normal operating mode to determine if the Game Port is being addressed. Nominal range of odd addresses in 201-207H. Default is 201H. SA<01> must be 0 and SA<00> must be 1 during the address comparison process.

Interrupt Source Register

This read/write register controls the source of each of the four CHIPSpak interrupt request lines. It is located at CRI offset 8H. Bit definitions are as follows:

Bits 7-6: Source for IRQ3. Default is 3 (UART 2—COM2)

Value	Interrupt Source
0	None
1	RTC
2	UART 1
3	UART 2

Bits 5-4: Source for IRQ4. Default is 2 (UART 1—COM1)

Value	Interrupt Source
0	None
1	RTC
2	UART 1
3	UART 2

Bits 3-2: Source for IRQ5. Default is 3 (Parallel—LPT2)

Value	Interrupt Source
0	None
1	RTC
2	UART 1
3	Parallel

Bits 1-0: Source for IRQ7. Default is 0 (disabled)

Value	Interrupt Source
0	None
1	RTC
2	UART 2
3	Parallel

Note:

1. It is possible to configure the CHIPSpak so that one source can cause interrupts on multiple lines.

Configuration Address Verification and Process Termination Register

This register is located at CRI offset FH. Reads perform one function while writes perform another. By reading this register, the configuration register address being used can be verified. Writing any data to this register terminates configuration mode for the CHIPSpak being addressed. The selected CHIPSpak will commence normal operation after the configuration process is terminated.

DESIGN CONSIDERATIONS

Reset

Due to support for standby battery power operation, a hardware RESET from the system bus does not reset the entire CHIPSpak. A hardware RESET will initialize the following functions:

1. RTC interrupts.
2. UART control registers except the Receive Buffer, Transmit Buffer and Divisor Registers if this option is selected at configuration time. The UARTs can also be configured so that none of their internal registers are initialized during a hardware RESET.

Normally a hardware RESET does not re-initialize anything except certain bus-related logic. The configuration of the parallel port and the RTC are not affected. The initialization of the UARTs after a hardware RESET depends on the option selected at CHIPSpak configuration time. This option is used to prevent the loss of serial port data when the processor in a remote controller (which was woken up by an incoming character) resumes operation.

A flag bit is maintained which indicates whether power has been removed from the CHIPSpak. This is used to determine when reconfiguration is required. It is maintained so long as VDD is applied to the device. If the flag bit is reset (during a power-up), the operation of the CHIPSpak is disabled while it awaits the commencement of a configuration sequence.

Multiplexed Address/Data Port

A single multiplexed Address/Data port is provided to minimize pin count. This port must be externally buffered from an XT or AT bus using TTL buffers to minimize the likelihood of ESD problems. In systems which do not have a multiplexed Address/Data bus, an external multiplexor must be used with the CHIPSpak. The selection pin of this multiplexor should be driven by ALE. When ALE is true, the Address should be gated to the CHIPSpak SAD<07:00> pins. When ALE is false, Data should be gated to CHIPSpak pins SAD<07:00>. In a computer which uses a multiplexed Address/Data bus internally, it is not necessary to externally gate either the Address or Data bus to the CHIPSpak SAD<07:00> pins.

Two CHIPSpak output control signals ($\overline{\text{ABENB}}$ and $\overline{\text{DBENB}}$) are generated from ALE, AEN, $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$. $\overline{\text{ABENB}}$ is used to enable the address bus LS244-type buffer. $\overline{\text{DBIN}}$ is used to control the direction of the external Data bus LS245-type buffers. The $\overline{\text{DBENB}}$ pin is used to enable the LS245 Data bus buffer. An additional input ($\overline{\text{XENB}}$)is provided to minimize chip count when sharing the Data bus buffer (LS245). Figure 16 below shows the

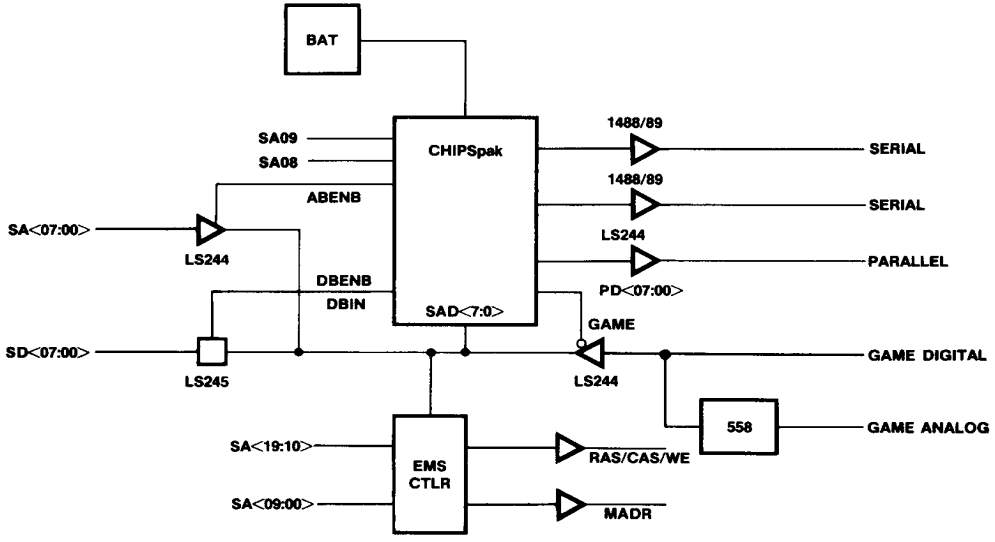


Figure 16. Multifunction Card Using CHIPSpak and an EMS Controller.
The LS244 which buffers the CHIPSpak SAD<07:00> pins from SA<07:00> is not required in a system with a multiplexed Address/Data bus.

CHIPSpak in a typical application with an EMS memory controller.

By default $\overline{DBENB}$ is high and $\overline{DBIN}$ is in high impedance state unless 82C606 recognizes the address for one of its devices.

For all IOR access to 82C606 devices, $\overline{DBENB}$ and $\overline{DBIN}$ are both low. For IOW access to 82C606 devices other than the game port $\overline{DBENB}$ is low and $\overline{DBIN}$ is high. For IOW accesses to the game port $\overline{DBENB}$ is high and $\overline{DBIN}$ is in high impedance state.

Interrupts

There are three sources for interrupts on the 82C605: the two UARTs and the parallel port. The 82C606 has an additional interrupt from the Real Time Clock. To permit software configuration, four 3-state interrupt request outputs are named: IRQ3, IRQ4, IRQ5 and IRQ7. These may be externally connected to any interrupt pins by the user. The outputs have sufficient drive to connect directly to the I/O channel.

PC Defaults and Conventions

The default I/O port addresses used by the IBM PC, PC/XT and PC/AT are as follows:

Device	IO Address	Interrupt	Note
LPT1	378-37FH	IRQ7	AT, XT
LPT2	278-27FH	IRQ5	AT only
COM1	3F8-3FFH	IRQ4	AT, XT
COM2	2F8-2FFH	IRQ3	AT, XT

The CHIPSpak will default to COM1 (UART1), COM2 (UART2) and LPT2 (the parallel port) when powered for the first time. These can be overridden by the setup/configuration program. The RTC will default to 2C0-2C1H as normally defined in an XT environment.

Multiple Usage Configuration

The SELECT pin is designed for use in applications where two to four CHIPSpaks are present. The CHIPSpaks are identified as units 0-3. The SELECT pin should be connected to one of the four lines SAD<07:04>. Connection of the SELECT pin to SAD<04> indicates unit 0, SAD<05> unit 1, etc. If the SELECT pin is not connected, the CHIPSpak will not respond. To ensure that a unique SAD line can be dedicated to each CHIPSpak (even if an add-on card containing one is installed), it is necessary to use external switches or jumpers.

If the CHIPSpak is located on an add-on multifunction card it should be configured as unit 0. If the CHIPSpak is located on the system board, it should probably be configured as unit 3. This will reduce the chance of confusion if the end user installs a multifunction card with another CHIPSpak (the most likely default configuration of the add-on CHIPSpak is unit 0). As mentioned above, an external jumper or switch is normally required to permit connection of the SELECT line to any of SAD<07:04> to ensure the use of non-conflicting addresses.

Table 8 Default Values of Configuration Registers

Offset	Default	Description
00H	00H	Invalid configuration, Oscillator on, Baud Rate Generator Clock enabled. RTC, UART1, UART2, Parallel, and Game port disabled.
01H	00H	Normal reset, Printer only, CTSs, DSRs and DCDs not enforced.
02H	00H	Divide by 2, and use Baud Rate Generator.
03H	B0H	RTC address 2C0H
04H	FEH	UART1 address 3F8H
05H	BEH	UART2 address 2F8H
06H	9EH	Parallel port address 278H
07H	80H	Game port address 200H
08H	ECH	IRQ3 = UART2, IRQ4 = UART1, IRQ5 = Parallel, IRQ7 = none.
0FH	na	

82C605/82C606 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device may occur of Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C605/82C606 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

DC Characteristics (T_A = 0-70°C, V_{CC} = 5 ± 5%)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.0 mA I_{OL} = 12mA (note 1)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -2.0 mA I_{OH} = -6.0mA (note 1)
I_{IL}	Input Current	-10	10	μA	V_{IN} = V_{CC} to 0V
I_{OL}	Output Leakage Current	-10	10	μA	V_{OU} = V_{CC} to 0.45
I_{CC}	V_{CC} Supply Current		20	mA	CLK Freq = 4 MHz
I_{CCSB}	V_{CC} Standby Supply Current (82C606 only)		10	μA	CLK Freq = DC without Oscillator Crystal

Capacitance (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance		10	pF	FC = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins
C_{OUT}	Output Capacitance		20	pF	Returned to V_{SS}

NOTE 1: for signal pins IRQ3, IRQ4, IRQ5, IRQ7

82C605/82C606 AC Characteristics

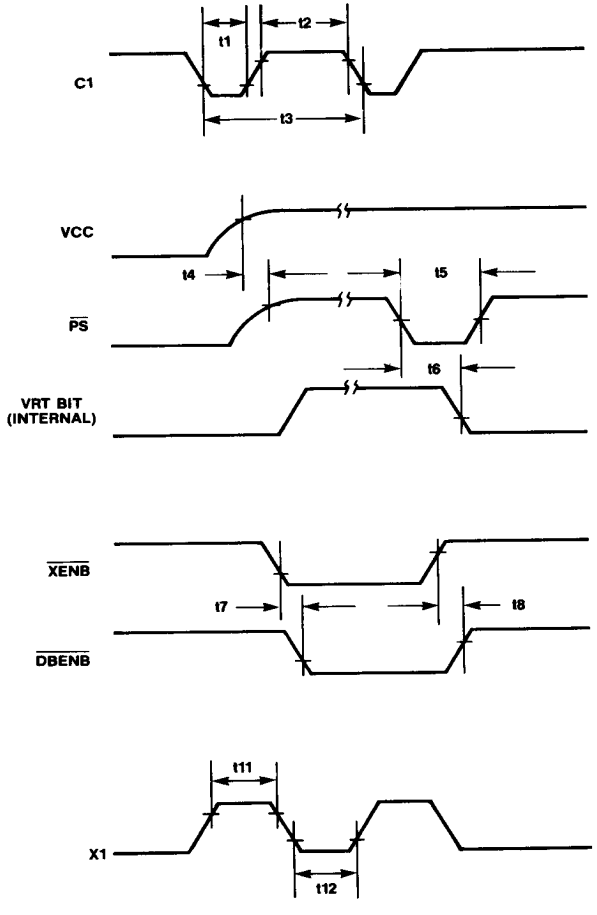
Description	Symbol	Min	Max	Units
t1	CI Low Time	200		ns
t2	CI High Rime	200		ns
t3	CI Period	500		ns
t4	$\overline{PS}$ High Delay from V_{CC}	5		μs
t5	$\overline{PS}$ Low Pulse Width	5		μs
t6	VRT Bit Valid Delay		2	μs
t7	$\overline{DBENB}$ Delay from $\overline{XENB}$		40	ns
t8	$\overline{DBENB}$ Delay from $\overline{XENB}$		40	ns
t11	Clock High Pulse at 3.1MHz	140		ns
t12	Clock Low Pulse at 3.1MHz	140		ns
t13	Delay of DBIN and $\overline{DENB}$ from $\overline{IOR}$, $\overline{IOW}$	40		ns
t14	Delay of DBIN and $\overline{DENB}$ from $\overline{IOR}$, $\overline{IOW}$	40		ns
t15	Delay of DBIN and $\overline{DENB}$ from $\overline{IOR}$, $\overline{IOW}$	40		ns
t16	Delay of DBIN and $\overline{DENB}$ from $\overline{IOR}$, $\overline{IOW}$	40		ns
t17	Delay from $\overline{IOR}$ (RD RBR or LSR) to Reset Interrupt		1	μs
t18	Delay from IOW↓ to Transmit Buffer to Reset Interrupt		175	ns
t19	Delay from Initial IOW↑ to Transmit Buffer to Interrupt (note 1)	16	32	TCLK cycles
t20	Delay from Initial INTR Reset to Transmit Start (note 1)	8	24	TCLK cycles
t21	Delay from Stop to Interrupt (note 1)	8	8	TCLK cycles
t22	Delay from RD IIR to Reset Interrupt		250	ns
t23	Delay from IOW↑ (to Modem Control Register) to Output		200	ns
t24	Delay from IOW↑ (MCR) to Control High Impedance of Interrupt		200	ns
t25	Delay to Set Interrupt from MODEM Input		250	ns
t26	Delay to Reset Interrupt from RD MSR		250	ns
t31	ALE High Width	45		ns
t32	Address Setup Time to ALE↓	35		ns
t33	Address Hold Time to ALE↓	10		ns
t34	ALE↓ to Command Active	25		ns

82C605/82C606 AC Characteristics
(Continued)

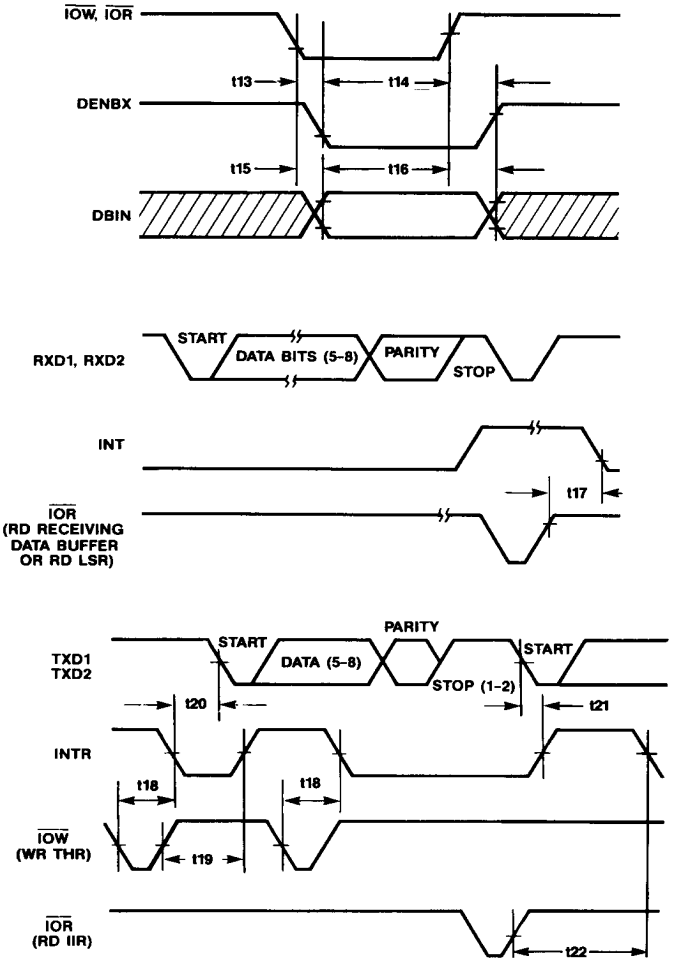
Description	Symbol	Min	Max	Units
t35	Command Width	300		ns
t36	AEN Setup Time to $\overline{IOR}$, $\overline{IOW}$	30		ns
t37	AEN Hold Time to $\overline{IOR}$, $\overline{IOW}$	4		ns
t38	Data Setup to IOW↑	100		ns
t39	Data Hold from IOW↑	10		ns
t40	Data Valid from IOR↓		200	ns
t41	Data Hold Read from IOR↑	10		ns
t42	Delay from Valid Data of Parallel Port Data Register & Control Register		200	ns
t43	Delay from Interrupt to ACK Input		250	ns
t50	$\overline{ABENB}$ delay from ALE↑	40		ns
t51	Valid address setup time to IOR↓ or IOW↓	60		ns

NOTE 1: TCLK is programmed by the user.

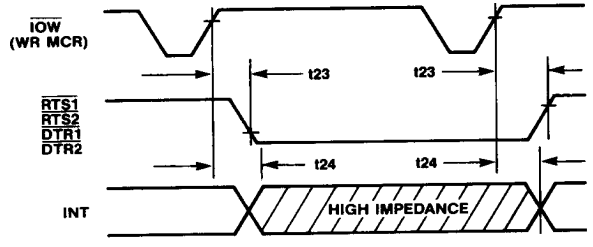
82C605/82C606 TIMING DIAGRAMS

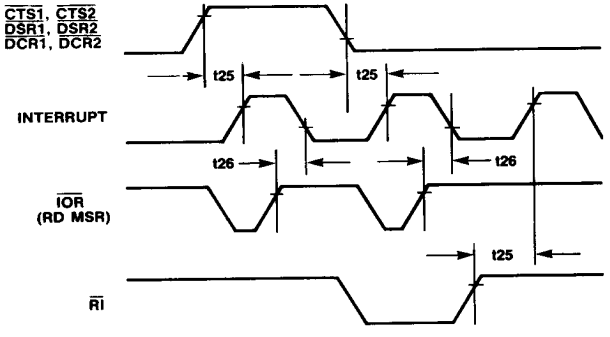


82C605/82C606 TIMING DIAGRAMS

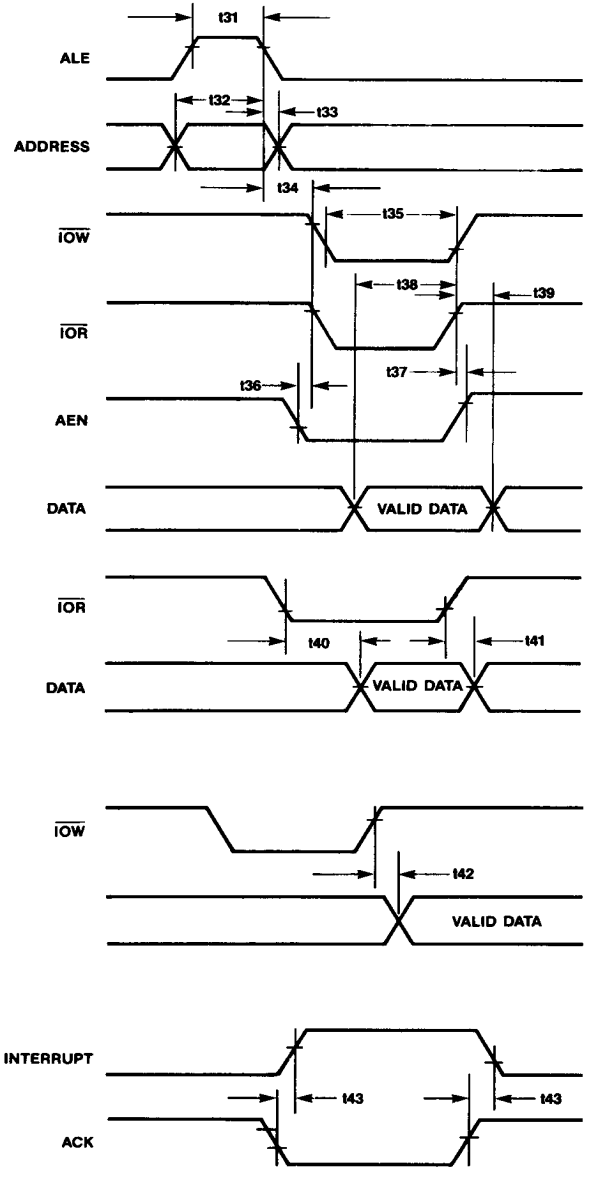


82C605/82C606 TIMING DIAGRAMS

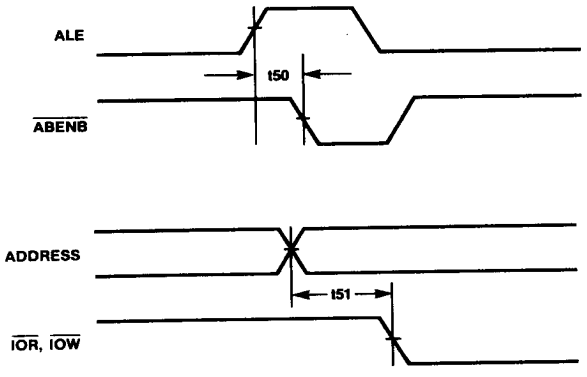




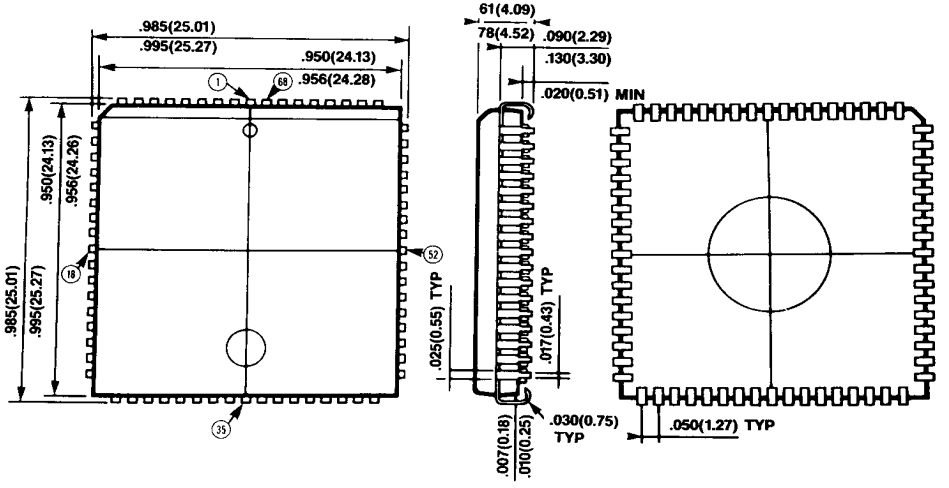
82C605/82C606 TIMING DIAGRAMS



82C605/82C606 TIMING DIAGRAMS



68-PIN PLASTIC LEADED CHIP CARRIER

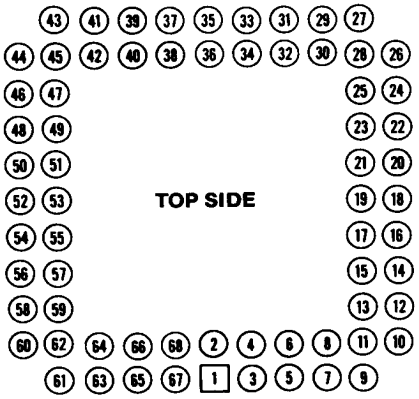


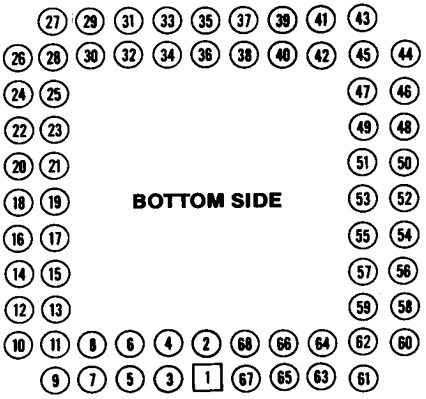
Ordering Information

Order Number	Package Type
P82C605	PLCC-68 pins
P82C606	PLCC-68 pins

Note:
1. PLCC = Plastic Leaded Chip Carrier

68-PIN PLCC SOCKET





RECEIVED 7-13-88

PAGE REF

RESEARCHED 7-25-88 MC

CHIPS

Chips and Technologies, Incorporated
521 Cottonwood Drive, Milpitas, CA 95035 408-434-0600 Telex 272929 CHIPS UR