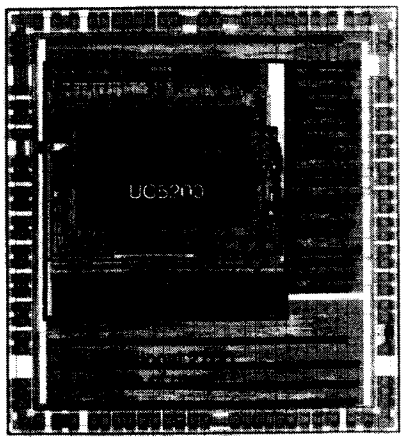
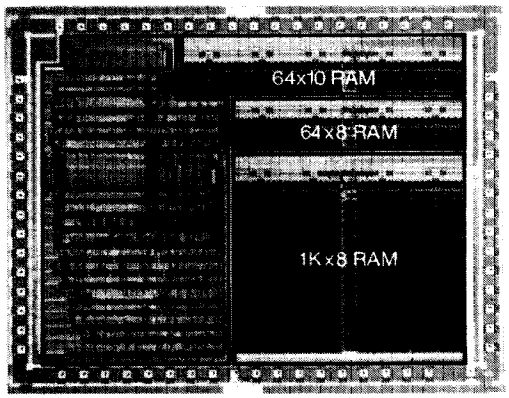
1.5 MICRON CHMOS III CELL LIBRARY

- 1.5 Micron CMOS
- User Configurable N-Bit Counters, Registers, Adders, and Magnitude Comparators Built from "Telescoping" Cells Achieve High Performance and Silicon Efficiency for Repetitive Functions
- RAM Configurations up to 8K bits
- All VLSI Cells are Tested and Verified Using the Equivalent Standard Product Test Program, Guaranteeing 0.1% AQL or Better.
- VLSiCEL™ Elements, Cell Versions of Popular Intel Standard Microprocessors, Microcontrollers, and Microprocessor Support Peripherals, Offer the Highest Level of Micro-Computer Based System Integration. The Current Library Includes:
  - 80C51BH 8-Bit Microcontroller
  - 82C37A Programmable DMA Controller
  - 82C54 Programmable Interval Timer
  - 82C59A Programmable Interrupt Controller
  - 82C84 8086/8088 Clock Generator
  - 82C284 80286 Clock Generator
  - 82C88 8086/8088 Bus Controller
  - 82288 80286 Bus Controller



240051-1

The Cell-Based IC Shown here Contains the 80C51BH ASIC Core. This Design also Integrates Approximately 2700 Gates of User Control Logic



240051-2

The Cell-Based IC Shown above Depicts a Standard Cell Design with 3000 Gates of User Logic and 3 RAM Configurations

*Daisy is a registered trademark of Daisy Systems Corporation.
*Mentor Graphics is a registered trademark of Mentor Graphics Corporation.

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DESCRIPTION

Intel's advanced cell-based family of integrated circuits is based on a comprehensive set of pre-designed, fully-characterized functions for the integration of system logic into high-performance, cost effective semicustom devices. The basic cell library contains over 150 logic, I/O and special function cells. Also available are VLSiCEL™ elements such as the 80C51BH 8-bit microcontroller, and cell equivalents of Intel microprocessor support peripheral functions. Intel libraries run on several industry standard CAE platforms, including Daisy Systems* and Mentor Graphics* workstations. Customers may receive expert technical support via Intel's fully equipped technology centers. Once a design has been completed to the customer's satisfaction, Intel produces its cell-based IC using a 1.5 micron double layer metal CMOS process. This process is also used on standard components such as the 80C51BH, thus ensuring manufacturability and high quality and reliability.

FEATURES/BENEFITS

Logic Cells

- Over 150 SSI/MSI/LSI logic functions to obtain high performance and high density.
- CMOS, TTL, and Schmitt Trigger compatible I/O cells available with a variety of drive levels and ESD protection to 2000V.

Special Function Cells

- Fixed configuration RAM to 8K bits.
- User configurable n-bit counters, shift registers, adders and magnitude comparators built from "Telescoping" cells achieve high performance and silicon efficiency for repetitive functions.

ASIC Emulators

- ASIC emulators support code development and "breadboard" simulation of 80C51BH-based ASICs.

Packaging

- A complete set of packaging options with lead counts to 208.

VLSiCEL™ ELEMENTS

- Cell versions of popular Intel standard microprocessors, microcontrollers and microprocessor support peripherals are available in the library. These "VLSiCEL" elements offer the highest level of microcomputer based system integration.

80C51BH	8-bit Microcontroller
82C37A	Programmable DMA Controller
82C54	Programmable Interval Timer
82C59A	Programmable Interrupt Controller
82C84A	8086 Clock Generator
82C284	80286 Clock Generator
82C88	8086 Bus Controller
82288	80286 Bus Controller

- UCS Family is based on the 80C51BH standard product and includes both the microcontroller core and peripheral functions. This family makes the internal communications bus (SFR Bus) available to the designer.
- The 12.5 MHz microprocessor support peripheral family includes 82CXX peripheral cells compatible with 86/186/286 environments.
- All VLSI cells are tested and verified using the equivalent standard product test program, guaranteeing 0.1% AQL or better.
- Functional relationships identical to the standard product, including standard product code compatibility.

Design Environment

- Libraries compatible with workstations from Daisy Systems and Mentor Graphics.
- Mainframe interface accessible to customers via Intel technology centers or dial-up from customer site. Supports high complexity designs.
- All design environments include Intel developed utilities for back annotation of actual delays from layout database for post layout simulations.
- Software utilities provided by Intel automatically converts your simulation stimulus to Intel tester compatible vectors.
- For those designs incorporating the 80C51-based VLSI cell and which are designed in the Daisy environment, customers may also simulate the core using Daisy's Physical Modeling Extension (PMX) board. The PMX is a hardware add-on chassis and control software that allows the user to perform software modeling using an actual physical component in the Daisy environment.

CHMOS III: 1.5 Micron CMOS

- Intel's cell based products are produced using CHMOS III—an advanced 1.5 micron, double-layer metal CMOS process technology providing high performance, high density, and low power consumption semi-custom integrated circuits with proven manufacturability.
- Intel's 80C51BH standard product also manufactured in CHMOS III.

Manufacturing Reliability

- 0.1% Average Quality Level (AQL) against submitted test vectors.
- < 200 Failures In Time (FITs).

LSI and VLSI Functions

UCS51 FAMILY: UCS51XX and UCS52XX cells listed below are fully compatible with the 80C51BH standard product. In addition, these cells make the internal bus (Special Function Register Bus) of the 80C51BH accessible to the designer. A series of SFR peripheral cells have been designed to interface to this bus. These peripherals are also listed below. Peripheral communications are optimized (less code required) and the designer can also define his own peripherals and connect them directly to the bus.

Name	Cell Description
UCS5100	80C51BH Microcontroller Core with No ROM, 128 Bytes RAM
UCS5104	80C51BH Microcontroller Core with 4K Bytes ROM, 128 Bytes RAM
UCS5108	80C51BH Microcontroller Core with 8K Bytes ROM, 128 Bytes RAM
UCS5116	80C51BH Microcontroller Core with 16K Bytes ROM, 128 Bytes RAM
UCS5200	80C51BH Microcontroller Core with No ROM, 256 Bytes RAM
UCS5204	80C51BH Microcontroller Core with 4K Bytes ROM, 256 Bytes RAM
UCS5208	80C51BH Microcontroller Core with 8K Bytes ROM, 256 Bytes RAM
UCS5216	80C51BH Microcontroller Core with 16K Bytes ROM, 256 Bytes RAM
UCS51BRG	Baud Rate Generator
UCS51SIO	Serial I/O
UCS51T2	Timer 2
UCS51BIU	SFR Bus Interface Unit
UCS51AD	8-Bit Analog to Digital Converter with Sample and Hold
UCS51IEU	Interrupt Expansion Unit

NOTE:
All specifications within tables are subject to change.

UC51 FAMILY: UC51XX cells listed below are fully compatible with the 80C51BH standard product and are available in a variety of ROM configurations. In addition, the signals from the standard product "CORE" have been demultiplexed, making all 116 signals available for use.

Name	Cell Description
UC5100	80C51BH Microcontroller Core with No ROM, 128 Bytes RAM
UC5104	80C51BH Microcontroller Core with 4K Bytes ROM, 128 Bytes RAM
UC5108	80C51BH Microcontroller Core with 8K Bytes ROM, 128 Bytes RAM
UC5116	80C51BH Microcontroller Core with 16K Bytes ROM, 128 Bytes RAM
UC5200	80C51BH Microcontroller Core with No ROM, 256 Bytes RAM
UC5204	80C51BH Microcontroller Core with 4K Bytes ROM, 256 Bytes RAM
UC5208	80C51BH Microcontroller Core with 8K Bytes ROM, 256 Bytes RAM
UC5216	80C51BH Microcontroller Core with 16K Bytes ROM, 256 Bytes RAM

80C51 Based Core Companion Cells: The following cells are used in conjunction with the UC51XX cells noted above.

Name	Cell Description
POSC	Oscillator
PWOSC	Oscillator with Power Down
PADB	Address/Data Bus I/O Buffer
PRESET	Reset Input Buffer
PTNQB	Quasi-Bidirectional I/O Buffer
PRGPIN	UC51 Programmable I/O Buffer
PRGUCS	UCS Programmable I/O Buffer

MICROPROCESSOR SUPPORT PERIPHERAL COMPANION CELLS: The following cells are used in conjunction with the microprocessor support peripheral cells noted above:

For use with SP8284/SP82284	
POSC2	Oscillator, frequency range to 37.5 MHz
PCNO4	Non-inverting CMOS Output Buffer, High Drive
For use with SP8288/SP82288	
PCO2	Inverting CMOS Output Buffer, High Drive
PCOT6	3-State Inverting CMOS Output Buffer with Enable, High Drive

MICROPROCESSOR SUPPORT PERIPHERAL FAMILY: These cells are equivalent in functionality to the corresponding Intel standard products.

Name	Cell Description
SP8237	Programmable DMA Controller
SP8254	Programmable Interval Timer
SP8259	Programmable Interrupt Controller
SP8284	8086/8088 Clock Generator and Driver
SP82284	80286 Clock Generator and Ready Interface
SP8288	8086/8088 Bus Controller
SP82288	80286 Bus Controller

Fixed Configuration Memory

Name	Cell Description
RAM64	64 x 8 Static Random Access Memory
RAM128	128 x 8 Static Random Access Memory
RAM256	256 x 8 Static Random Access Memory
RAM512	512 x 8 Static Random Access Memory
RAM1K	1024 x 8 Static Random Access Memory

NOTE:
All specifications within tables are subject to change.

Telescoping Cells

Telescoping cells are building blocks from which certain multi-stage logic functions can be implemented. They are the preferred method of construction for multi-stage logic functions because they allow the designer to implement the exact function width required by the design. Silicon utilization is optimized. Front end work station tools make the creation of telescoping blocks transparent to the user.

Name	Cell Description
REGC	Telescoping Register Control
REGB	Telescoping Register Body
REGCT	Telescoping 3-State Register Control
REGBT	Telescoping 3-State Register Body
SHRC	Telescoping Shift Register Control
SHRB	Telescoping Shift Register Body
SHLC	Telescoping Shift Register with Load, Control
SHLB	Telescoping Shift Register with Load, Body
CULC	Telescoping Up Counter Control
CULB	Telescoping Up Counter Body
CULP	Telescoping Up Counter Carry Out Driver
CUPC	Telescoping Up/Down Counter Control
CUPB	Telescoping Up/Down Counter Body
CUPP	Telescoping Up/Down Counter End Count Driver
CUPP2	Telescoping Up/Down Counter End Count/Carry/Borrow Driver
ADDC	Telescoping Adder Control
ADDB	Telescoping Adder Body
ADDP	Telescoping Adder Carry Out Driver
CMPC	Telescoping Magnitude Comparator Control
CMPB	Telescoping Magnitude Comparator Body
CMPP	Telescoping Magnitude Comparator Equal/Greater Than/Less Than Driver

NOTICE: All specifications within tables are subject to change.

Inverters, Buffers and Gates

Name	Cell Description
INVN	Inverter, Normal Drive
INVNH	Inverter, High Drive
INVTE	3-State Inverter with Active Low Output Enable, Normal Drive
INVTD	3-State Inverter with Active High Output Enable, Normal Drive
BUF	Buffer, Normal Drive
BUFH	Buffer, High Drive
BUF2	Buffer with Dual Output, Normal Drive
BUFTD	3-State Buffer with Active High Output Enable, Normal Drive
BUFTE	3-State Buffer with Active Low Output Enable, Normal Drive
NAN2	2 Input NAND, Normal Drive
NAN3	3 Input NAND, Normal Drive
NAN4	4 Input NAND, Normal Drive
NAN5	5 Input NAND, Normal Drive
NAN6	6 Input NAND, Normal Drive
NAN7	7 Input NAND, Normal Drive
NAN8	8 Input NAND, Normal Drive
NOR2	2 Input NOR, Normal Drive
NOR3	3 Input NOR, Normal Drive
NOR4	4 Input NOR, Normal Drive
NOR5	5 Input NOR, Normal Drive
NOR6	6 Input NOR, Normal Drive
NOR7	7 Input NOR, Normal Drive
NOR8	8 Input NOR, Normal Drive
AND2	2 Input AND, Normal Drive
AND3	3 Input AND, Normal Drive
AND4	4 Input AND, Normal Drive
AND5	5 Input AND, Normal Drive
AND6	6 Input AND, Normal Drive
AND7	7 Input AND, Normal Drive
AND8	8 Input AND, Normal Drive
OR2	2 Input OR, Normal Drive
OR3	3 Input OR, Normal Drive
OR4	4 Input OR, Normal Drive
OR5	5 Input OR, Normal Drive
OR6	6 Input OR, Normal Drive
OR7	7 Input OR, Normal Drive
OR8	8 Input OR, Normal Drive
AOR22	2 AND2 into OR2, Normal Drive
AOI22	2 AND2 into NOR2, Normal Drive
EXR2	2 Input EXCLUSIVE OR, Normal Drive
EXN2	2 Input EXCLUSIVE NOR, Normal Drive

NOTICE: All specifications within tables are subject to change.

Flip-Flops and Latches

Name	Cell Description
FFT	Toggle Flip-Flop with Master Reset
FFTE	Toggle Flip-Flop with Enable and Master Reset
FFJK	JK Flip-Flop with Master Reset
FLJK	JK Flip-Flop with Master Set and Master Reset
FLJKT	3-State JK Flip-Flop with Master Set and Master Reset
FFD	D Flip-Flop with Master Reset
FFDE	D Flip-Flop with Enable and Master Reset
FLDE	D Flip-Flop with Enable, Master Set and Master Reset
FLDET	3-State D Flip-Flop with Enable, Master Set and Master Reset
FFDM2	D Flip-Flop with 2 to 1 Data Multiplexer and Master Reset
FLDM2	D Flip-Flop with 2 to 1 Data Multiplexer, Master Set and Master Reset
FFDHI	Positive Edge Event Trigger with Master Reset
LAD	Transparent D Latch with Master Reset
LSR	S-R Latch with Master Reset
LASR	S-R Latch with Enable and Master Reset
LNSR	$\overline{S}$-$\overline{R}$ Latch with Master Reset
LANSR	$\overline{S}$-$\overline{R}$ Latch with Enable and Master Reset

Multiplexers, Decoders and Arithmetic Functions

Name	Cell Description
MUX21	2-Line to 1-Line Multiplexer
MUX41	4-Line to 1-Line Multiplexer
DMX2	2-Line to 4-Line Demultiplexer/Decoder with 2 Enables
DMX3	3-Line to 8-Line Demultiplexer/Decoder
CPR	8/9-Bit Parity Checker/Generator

NOTICE: All specifications within tables are subject to change.

Input/Output Functions

Name	Cell Description
PCI	Non-Inverting CMOS Input Buffer, Normal Drive
PCIH	Non-Inverting CMOS Input Buffer, High Drive
PTI	Non-Inverting TTL Input Buffer, Normal Drive
PTIH	Non-Inverting TTL Input Buffer, High Drive
PTIRH	Non-Inverting TTL Input Buffer with Pull-Up Resistor, High Drive
PISH	Non-Inverting TTL Schmitt Trigger Input Buffer, High Drive
PISRH	Non-Inverting TTL Schmitt Trigger Input Buffer with Pull-Up Resistor, High Drive
PCO	Inverting CMOS Output Buffer, Low Drive
PCNO	Non-Inverting CMOS Output Buffer, Low Drive
PCOT	3-State Inverting CMOS Output Buffer, Low Drive
PTO	Inverting TTL Output Buffer, Low Drive
PTNO	Non-Inverting TTL Output Buffer, Low Drive
PTNO3	Non-Inverting TTL Output Buffer, Medium Drive
PTNO5	Non-Inverting TTL Output Buffer, High Drive
PTOT	3-State Inverting TTL Output Buffer, Low Drive
PTOT3	3-State Inverting TTL Output Buffer, Medium Drive
PTOT5	3-State Inverting TTL Output Buffer, High Drive
PTND	Non-Inverting TTL Open-Drain Output Buffer, Low Drive
PTND3	Non-Inverting TTL Open-Drain Output Buffer, Medium Drive
PTND5	Non-Inverting TTL Open-Drain Output Buffer, High Drive
PCIO	CMOS I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, Low Drive
PTIO	TTL I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, Low Drive
PTIO3	TTL I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, Medium Drive
PTIO5	TTL I/O Buffer; Latched Non-Inverting Input, 3-State Inverting Output, High Drive

NOTICE: All specifications within tables are subject to change.

INTEL DESIGN ENVIRONMENT

Intel's design environment includes the software tools necessary to assist customers with their Intel cell-based design. Intel provides workstation library models and utilities to support schematic capture, netlist generation, and functional and timing simulation in the Daisy Systems or Mentor Graphics environments. For complex designs requiring simulation capability exceeding the capabilities of the workstation, Intel provides mainframe simulation. Automatic test vector generation software is provided to assist the customer in the development of input test stimuli. The table below shows the typical flow of Intel cell-based design activities.

Task	Intel Feature	Responsibility
System Design		Customer
Schematic Capture, User Logic and Test Logic Design	Customer Maintains Control of the Design Specification.	Customer
Netlist Generation	Electrical Rules Check. Flags Illegal use of Cells.	Customer
Simulation	Built in Timing Verifier.	Customer
Test Vector Generation	Automatic Conversion of User's Simulation Vectors to Intel-tester Compatible Format. 100% Explainable Toggle Node Count Required.	Customer
Design Review		Customer
Auto Place and Route	Proprietary Tools for Automatic Place and Route, Mask design.	Intel
Back Annotation/ Post-Layout Simulation	Resistance and Capacitance Values Extracted from Layout Database.	Intel/Customer
Design Review		Intel/Customer
Fab, Assembly, Test		Intel
Prototype Delivery	On-Time Delivery; Conformance to Specifications.	Intel

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias
- Plastic ..... −40°C to +85°C
- Ceramic ..... −55°C to +125°C

Storage Temperature ..... −65°C to +150°C

DC Supply Voltage (V_{DD}) ..... 0V to 7.0V

Voltage to Any Pin with Respect to Ground ..... −0.5V to V_{DD} + 0.5V

Power Dissipation 1.0W

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage, V_{DD} ..... +4.5V to 5.5V

Case Temperature ..... 0°C to +70°C

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

PACKAGING

Intel's cell-based ICs are available in a wide variety of both through-board and surface-mount packages. DIP, chip carrier, pin grid array and flatpack configurations are offered. Special packages are available by request.

Intel ASIC Components Packaging Alternatives

Package Type	Leadcount	Ceramic	Plastic
Dual-In-Line(1)	16		X
	18		X
	20	X	X
	24	X	X
	28	X	X
	40	X	X
	48	X	X
Leaded Chip Carrier	20		X
	28		X
	32		X
	44	X(2)	X
	52		X
	68	X(2)	X
	84	X(2)	X
Leadless Chip Carrier	68	X	
	84	X(2)	
Quad Flat Pack	84	X(2)	X
	100	X(2)	X
	132	X(2)	X
	164	X(2)	X
Pin Grid Array	68	X	
	72	X	
	84	X	
	88	X	
	100	X	
	132	X	
	144	X	
	180	X	
	208	X	

NOTES:
1. Hermetic DIPs may be side-brazed or CERDIP.
2. Prototype only.

D.C. CHARACTERISTICS/I-O CELLS 0°C–70°C, 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Low Level Input Voltage				
	TTL Inputs		0.8	V	
	CMOS Inputs		1.2	V	
V_{IH}	High Level Input Voltage				
	TTL Inputs	2.0		V	
	CMOS Inputs	3.5		V	
I_{IL}	Low Level Input Current				
	TTL Inputs		−10	μA	$V_{IL} = V_{SS}$
	CMOS Inputs		−10	μA	$V_{IL} = V_{SS}$
I_{IH}	High Level Input Current				
	TTL Inputs		10	μA	$V_{IH} = V_{DD}$
	CMOS Inputs		10	μA	$V_{IH} = V_{DD}$
V_{OL}	Low Level Output Voltage				
	TTL Inputs		0.45	V	
	CMOS Inputs		0.4	V	
V_{OH}	High Level Output Voltage				
	TTL Inputs	2.4		V	
	CMOS Inputs	3.6		V	
I_{OL}	Low Level Output Current				
	TTL Outputs		3.2	mA	Low Drive
	TTL Outputs		7	mA	Medium Drive
	TTL Outputs		12	mA	High Drive
	CMOS Outputs		3.2	mA	
I_{OH}	High Level Output Current				
	TTL Outputs		−0.08	mA	All Drives
	CMOS Outputs		−2.4	mA	

NOTICE: All specifications within tables are subject to change.

DESIGN SUPPORT AND INTERFACE

Intel's design environment provides customers with expert technical support, either locally or in dedicated ASIC Technology Centers. Intel training and field application engineers offer training classes, design consultation, and technical support for semicustom chip design, cell-based design libraries, and engineering workstation (CAE) tools. ASIC Technology Centers are equipped with Daisy and Mentor workstations. These design centers also provide customers with access to factory mainframes for efficient simulation of complex designs.

ORDERING INFORMATION

Contact your local Intel sales office.

RELATED LITERATURE

Item	Order Number
Introduction to Intel Cell-Based Design	231816