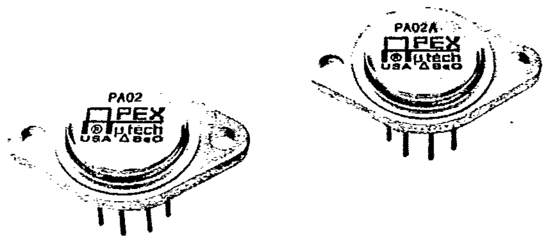
PA02 • PA02A

POWER OPERATIONAL AMPLIFIERS

T-79-23



FEATURES

- HIGH POWER BANDWIDTH - 350KHz
- HIGH SLEW RATE - 20V/μs
- FAST SETTLING TIME - 600ns
- LOW CROSSOVER DISTORTION - Class A/B
- LOW INTERNAL LOSSES - 1.2V at 2A
- HIGH OUTPUT CURRENT - ±5A Peak
- LOW INPUT BIAS CURRENT - FET Input
- ISOLATED CASE - 300 VDC

APPLICATIONS

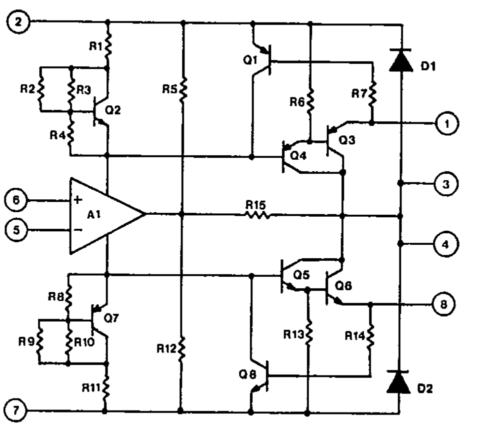
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 5A
- POWER TRANSDUCERS UP TO 350 KHz
- AUDIO AMPLIFIERS UP TO 30W RMS

DESCRIPTION

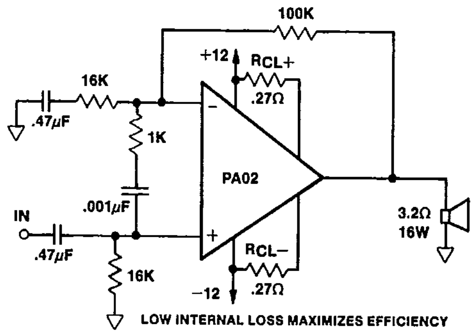
The PA02 and PA02A are wideband, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary "collector output" stage can swing close to the supply rails and is protected against inductive kickback. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors (down to 10mA). Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is hermetically sealed and electrically isolated. Isolation washers are not recommended. The use of compressible isolation washers may void the warranty.

SCHEMATIC



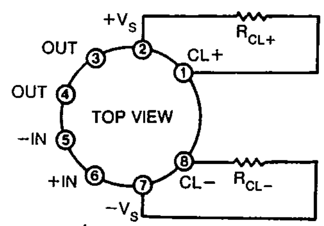
TYPICAL APPLICATION



Vehicular Sound System Power Stage

When system voltages are low and power is at a premium, the PA02 is a natural choice. The circuit above utilizes not only the feature of low internal loss of the PA02, but also its very low distortion level to implement a crystal clear audio amplifier suitable even for airborne applications. This circuit uses AC coupling of both the input signal and the gain circuit to render DC voltage across the speaker insignificant. The resistor and capacitor across the inputs form a stability enhancement network (refer to Application Note 1). The 0.27 ohm current limit resistors provide protection in the event of an output short circuit.

EXTERNAL CONNECTIONS



PA02 ABSOLUTE MAXIMUM RATINGS

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SUPPLY VOLTAGE, $+V_S$ to $-V_S$	38V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	48W
INPUT VOLTAGE, differential	$\pm V_S$ −5V
INPUT VOLTAGE, common-mode	$\pm V_S$ −2V
TEMPERATURE, pin solder-10s	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE RANGE, storage	−65 to +150°C
OPERATING TEMPERATURE RANGE, case	−55 to +125°C

SPECIFICATIONS

		PA02			PA02A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±5	±10		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±50		*	±25	μV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±10			*		μV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±6			*		μV/W
BIAS CURRENT, initial	T_C = 25°C		50	200		25	100	pA
BIAS CURRENT, vs. temperature	T_C = 85°C			60			*	nA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		25	100		15	50	pA
OFFSET CURRENT, vs. temperature	T_C = 85°C			15			*	nA/°C
INPUT IMPEDANCE, dc	T_C = 25°C		1000			*		GΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON-MODE VOLT. RANGE,[5] Pos.	Full temperature range	$+V_S$ −6	$+V_S$ −3		*	*		V
COMMON-MODE VOLT. RANGE,[5] Neg.	Full temperature range	$-V_S$ +6	$-V_S$ +5		*	*		V
COMMON-MODE REJECTION, dc	Full temperature range	70	100		*	*		db
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1kΩ load		103			*		db
OPEN LOOP GAIN at 10Hz	Full temp. range, 10kΩ load	86	100		*	*		db
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, 10Ω load		4.5			*		MHz
POWER BANDWIDTH	T_C = 25°C, 10Ω load		350			*		kHz
PHASE MARGIN	Full temp. range, 10Ω load		45			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A, R_{CL} = .08Ω	$\pm V_S$ −4	$\pm V_S$ −3		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 2A	$\pm V_S$ −2	$\pm V_S$−1.2		*	*		V
CURRENT, peak	T_C = 25°C	5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		.6			*		μs
SLEW RATE	T_C = 25°C	13	20		*	*		V/μs
CAPACITIVE LOAD	Full temp. range, G >10		SOA			*		
HARMONIC DISTORTION	P_O = .5W, F = 1kHz, R_L = 10Ω		.004			*		%
SMALL SIGNAL rise/fall time	R_L = 10Ω, G = 1		100			*		ns
SMALL SIGNAL overshoot	R_L = 10Ω, G = 1		10			*		%
POWER SUPPLY								
VOLTAGE	Full temperature range	±7	±15	±19	*	*	*	V
CURRENT, quiescent	T_C = 25°C		27	37		*	*	mA
THERMAL								
RESISTANCE, ac[4] junction to case	F>60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, dc junction to case	F<60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meet full range specification	−25		+85	−55		+125	°C

NOTES:
- * The specification of PA02A is identical to the specification for PA02 in applicable column to the left.

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Exceeding CMV range can cause the output to latch.

CAUTION: The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

PA02 TYPICAL PERFORMANCE GRAPHS

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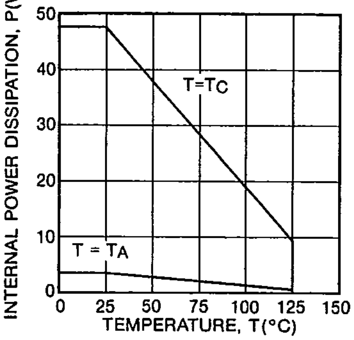
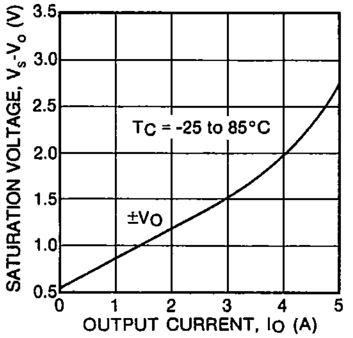
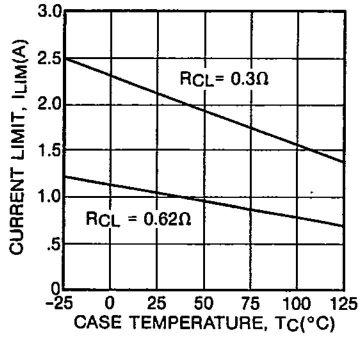
POWER DERATING



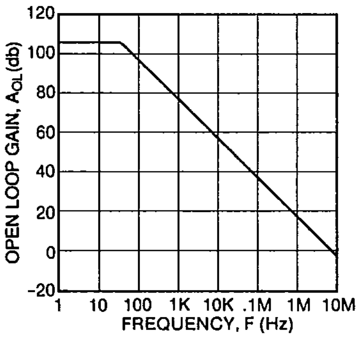
OUTPUT VOLTAGE SWING



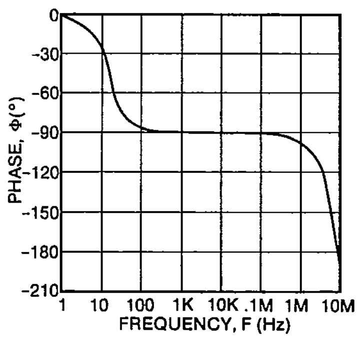
CURRENT LIMIT



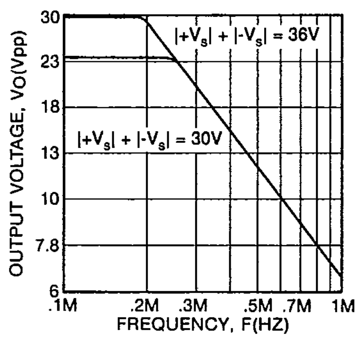
SMALL SIGNAL RESPONSE



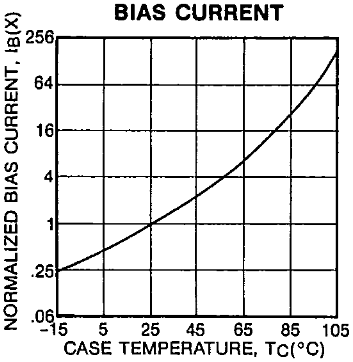
PHASE RESPONSE



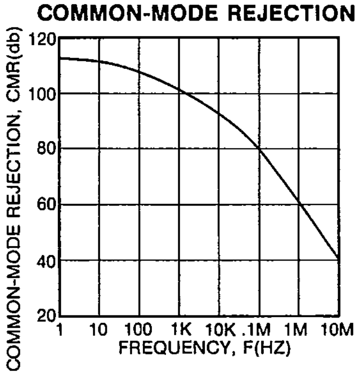
POWER RESPONSE



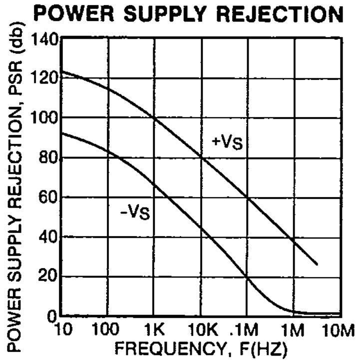
BIAS CURRENT



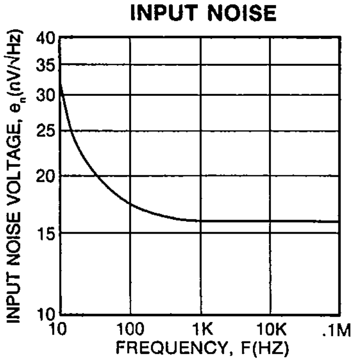
COMMON-MODE REJECTION



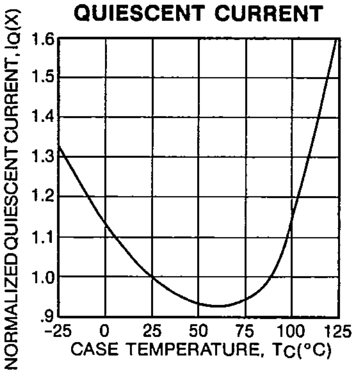
POWER SUPPLY REJECTION



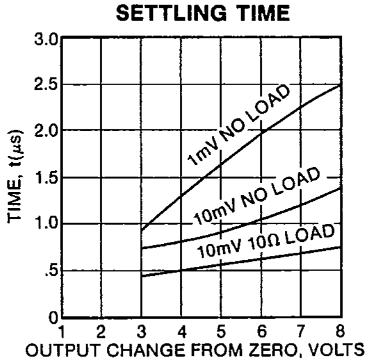
INPUT NOISE



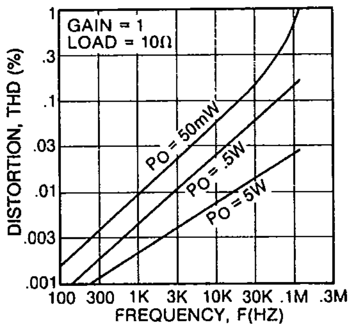
QUIESCENT CURRENT



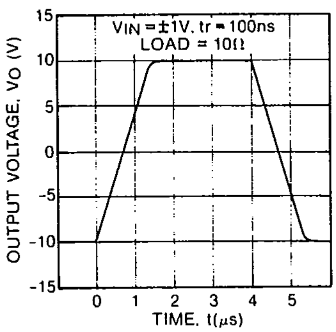
SETTLING TIME



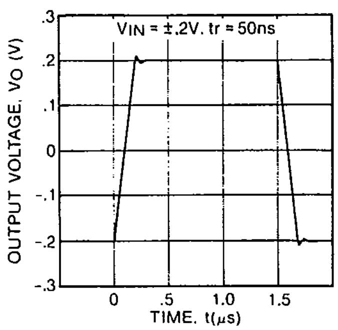
HARMONIC DISTORTION



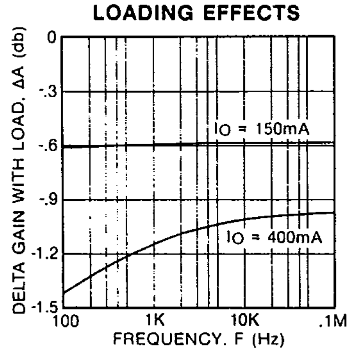
PULSE RESPONSE



PULSE RESPONSE



LOADING EFFECTS



PA02 OPERATING CONSIDERATIONS

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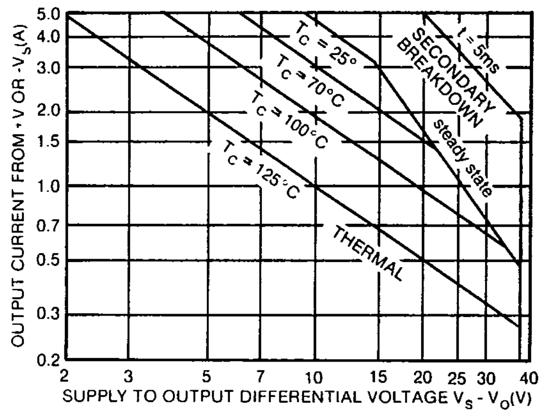
GENERAL

Please read the "General Operating Considerations" section which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the applications notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)



The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximums are safe:

±V_S	CAPACITIVE LOAD I_{LIM} = 2A	CAPACITIVE LOAD I_{LIM} = 5A	INDUCTIVE LOAD I_{LIM} = 2A	INDUCTIVE LOAD I_{LIM} = 5A
18V	2mF	0.7mF	.2H	10mH
15V	10mF	2.2mF	.7H	25mH
10V	25mF	10mF	5H	50mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 5A, or 17V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifer can handle any EMF generating or reactive load and short circuits to the supply rails or shorts to common if the current limits are set as follows at T_C = 85°C.

±V_S	SHORT TO ±V_S, C, L OR EMF LOAD	SHORT TO COMMON
18V	.5A	1.7A
15V	.7A	2.8A
10V	1.6A	4.2A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is 0.12 ohm, however for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

DEVICE MOUNTING

The case (mounting flange) is electrically-isolated and should be mounted directly to a heatsink with thermal compound. Screws with Belville spring washers are recommended to maintain positive clamping pressure on heatsink mounting surfaces. Long periods of thermal cycling can loosen mounting screws and increase thermal resistance.

Since the case is electrically isolated (floating) with respect to the internal circuits it is recommended to connect it to common or other convenient AC ground potential.

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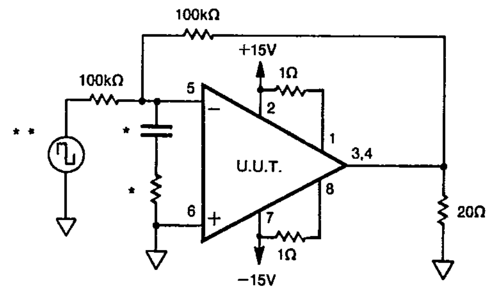
PA02M

TABLE 4 — GROUP A INSPECTION

SG	PARAMETER	SYMBOL	TEMP	PWR	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±15V	V_{IN} = 0, G = 100, R_{CL} = .2Ω†		40	mA
1	Input Offset Voltage	V_{OS}	25°C	±15V	V_{IN} = 0, G = 100		10	mV
1	Input Offset Voltage	V_{OS}	25°C	±7V	V_{IN} = 0, G = 100		11.6	mV
1	Input Offset Voltage	V_{OS}	25°C	±19V	V_{IN} = 0, G = 100		10.8	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±15V	V_{IN} = 0, G = 100		200	pA
1	Input Bias Current, −IN	$-I_B$	25°C	±15V	V_{IN} = 0, G = 100		200	pA
1	Input Offset Current	I_{OS}	25°C	±15V	V_{IN} = 0, G = 100		100	pA
3	Quiescent Current	I_Q	−55°C	±15V	V_{IN} = 0, G = 100, R_{CL} = .2Ω†		60	mA
3	Input Offset Voltage	V_{OS}	−55°C	±15V	V_{IN} = 0, G = 100		14	mV
3	Input Offset Voltage	V_{OS}	−55°C	±7V	V_{IN} = 0, G = 100		15.6	mV
3	Input Offset Voltage	V_{OS}	−55°C	±19V	V_{IN} = 0, G = 100		14.8	mV
3	Input Bias Current, +IN	$+I_B$	−55°C	±15V	V_{IN} = 0, G = 100		200	pA
3	Input Bias Current, −IN	$-I_B$	−55°C	±15V	V_{IN} = 0, G = 100		200	pA
3	Input Offset Current	I_{OS}	−55°C	±15V	V_{IN} = 0, G = 100		100	pA
2	Quiescent Current	I_Q	125°C	±15V	V_{IN} = 0, G = 100, R_{CL} = .2Ω†		60	mA
2	Input Offset Voltage	V_{OS}	125°C	±15V	V_{IN} = 0, G = 100		15	mV
2	Input Offset Voltage	V_{OS}	125°C	±7V	V_{IN} = 0, G = 100		16.6	mV
2	Input Offset Voltage	V_{OS}	125°C	±19V	V_{IN} = 0, G = 100		15.8	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±15V	V_{IN} = 0, G = 100		10	nA
2	Input Bias Current, −IN	$-I_B$	125°C	±15V	V_{IN} = 0, G = 100		10	nA
2	Input Offset Current	I_{OS}	125°C	±15V	V_{IN} = 0, G = 100		10	nA
4	Output Voltage, I_O = 5A	V_O	25°C	±9V	R_L = 1Ω, R_{CL} = 0Ω	5		V
4	Output Voltage, I_O = 36mA	V_O	25°C	±19V	R_L = 500Ω	18		V
4	Output Voltage, I_O = 2A	V_O	25°C	±12V	R_L = 5Ω, R_{CL} = 0Ω	10		V
4	Current Limits	I_{CL}	25°C	±9V	R_L = 1Ω, R_{CL} = .2Ω	2.6	3.9	A
4	Stability/Noise	E_N	25°C	±15V	R_L = 500Ω, G = 1, C_L = 1.5nF		1	mV
4	Slew Rate	SR	25°C	±18V	R_L = 500Ω	13	100	V/μs
4	Open Loop Gain	A_{OL}	25°C	±15V	R_L = 500Ω, f = 10Hz	86		db
4	Common-mode Rejection	CMR	25°C	±8.25V	R_L = 500Ω, f = DC, V_{CM} = ±2.25V	70		db
6	Output Voltage, I_O = 5A	V_O	−55°C	±9V	R_L = 1Ω, R_{CL} = 0Ω	5		V
6	Output Voltage, I_O = 36mA	V_O	−55°C	±19V	R_L = 500Ω	18		V
6	Output Voltage, I_O = 2A	V_O	−55°C	±12V	R_L = 5Ω, R_{CL} = 0Ω	10		V
6	Stability/Noise	E_N	−55°C	±15V	R_L = 500Ω, G = 1, C_L = 1.5nF		1	mV
6	Slew Rate	SR	−55°C	±18V	R_L = 500Ω	13	100	V/μs
6	Open Loop Gain	A_{OL}	−55°C	±15V	R_L = 500Ω, f = 10Hz	86		db
6	Common-mode Rejection	CMR	−55°C	±8.25V	R_L = 500Ω, f = DC, V_{CM} = ±2.25V	70		db
5	Output Voltage, I_O = 3A	V_O	125°C	±7V	R_L = 1Ω, R_{CL} = 0Ω	3		V
5	Output Voltage, I_O = 36mA	V_O	125°C	±19V	R_L = 500Ω	18		V
5	Output Voltage, I_O = 2A	V_O	125°C	±12V	R_L = 5Ω, R_{CL} = 0Ω	10		V
5	Stability/Noise	E_N	125°C	±15V	R_L = 500Ω, G = 1, C_L = 1.5nF		1	mV
5	Slew Rate	SR	125°C	±18V	R_L = 500Ω	8.5	100	V/μs
5	Open Loop Gain	A_{OL}	125°C	±15V	R_L = 500Ω, f = 10Hz	86		db
5	Common-mode Rejection	CMR	125°C	±8.25V	R_L = 500Ω, f = DC, V_{CM} = ±2.25V	70		db

†30 secoonds after power applied.

BURN IN CIRCUIT:



*These components are used to stabilize device due to poor high frequency characteristics of burn in board.
**Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA02MU REV. C SEPTEMBER 1989

APEX μtech

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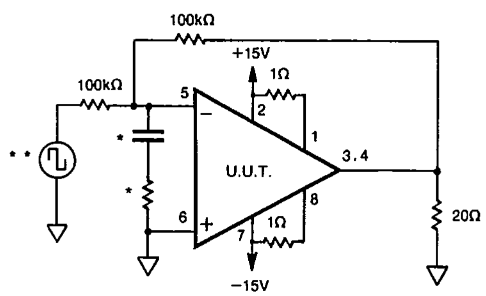
PA02Q

100% TEST TABLE

SG	PARAMETER	SYMBOL	TEMP	PWR	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±15V	$V_{IN}=0$, G = 100		40	mA
1	Input Offset Voltage	V_{OS}	25°C	±15V	$V_{IN}=0$, G = 100		10	mV
1	Input Offset Voltage	V_{OS}	25°C	±7V	$V_{IN}=0$, G = 100		11.6	mV
1	Input Offset Voltage	V_{OS}	25°C	±19V	$V_{IN}=0$, G = 100		10.8	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±15V	$V_{IN}=0$, G = 100		200	pA
1	Input Bias Current, −IN	$-I_B$	25°C	±15V	$V_{IN}=0$, G = 100		200	pA
1	Input Offset Current	I_{OS}	25°C	±15V	$V_{IN}=0$, G = 100		100	pA
3	Quiescent Current	I_Q	−25°C	±15V	$V_{IN}=0$, G = 100		60	mA
3	Input Offset Voltage	V_{OS}	−25°C	±15V	$V_{IN}=0$, G = 100		12.5	mV
3	Input Offset Voltage	V_{OS}	−25°C	±7V	$V_{IN}=0$, G = 100		14.1	mV
3	Input Offset Voltage	V_{OS}	−25°C	±19V	$V_{IN}=0$, G = 100		13.3	mV
3	Input Bias Current, +IN	$+I_B$	−25°C	±15V	$V_{IN}=0$, G = 100		200	pA
3	Input Bias Current, −IN	$-I_B$	−25°C	±15V	$V_{IN}=0$, G = 100		200	pA
3	Input Offset Current	I_{OS}	−25°C	±15V	$V_{IN}=0$, G = 100		100	pA
2	Quiescent Current	I_Q	85°C	±15V	$V_{IN}=0$, G = 100		60	mA
2	Input Offset Voltage	V_{OS}	85°C	±15V	$V_{IN}=0$, G = 100		13	mV
2	Input Offset Voltage	V_{OS}	85°C	±7V	$V_{IN}=0$, G = 100		14.6	mV
2	Input Offset Voltage	V_{OS}	85°C	±19V	$V_{IN}=0$, G = 100		13.8	mV
2	Input Bias Current, +IN	$+I_B$	85°C	±15V	$V_{IN}=0$, G = 100		10	nA
2	Input Bias Current, −IN	$-I_B$	85°C	±15V	$V_{IN}=0$, G = 100		10	nA
2	Input Offset Current	I_{OS}	85°C	±15V	$V_{IN}=0$, G = 100		6.4	nA
4	Output Voltage, $I_O=5A$	V_O	25°C	±9V	$R_L=1\Omega$	5		V
4	Output Voltage, $I_O=36mA$	V_O	25°C	±19V	$R_L=500\Omega$	18		V
4	Output Voltage, $I_O=2A$	V_O	25°C	±12V	$R_L=5\Omega$	10		V
4	Current Limits	I_{CL}	25°C	±9V	$R_L=1\Omega$, $R_{CL}=.2\Omega$	2.6	3.9	A
4	Stability/Noise	E_N	25°C	±15V	$R_L=500\Omega$, G = 1, $C_L=1.5nF$		1	mV
4	Slew Rate	SR	25°C	±15V	$R_L=500\Omega$	13	100	V/μs
4	Open Loop Gain	A_{OL}	25°C	±15V	$R_L=500\Omega$, f = 10Hz	86		db
4	Common-mode Rejection	CMR	25°C	±8.25V	$R_L=500\Omega$, f = DC, $V_{CM}=\pm2.25V$	70		db
6	Output Voltage, $I_O=5A$	V_O	−25°C	±9V	$R_L=1\Omega$	5		V
6	Output Voltage, $I_O=36mA$	V_O	−25°C	±19V	$R_L=500\Omega$	18		V
6	Output Voltage, $I_O=2A$	V_O	−25°C	±12V	$R_L=5\Omega$	10		V
6	Stability/Noise	E_N	−25°C	±15V	$R_L=500\Omega$, G = 1, $C_L=1.5nF$		1	mV
6	Slew Rate	SR	−25°C	±15V	$R_L=500\Omega$	13	100	V/μs
6	Open Loop Gain	A_{OL}	−25°C	±15V	$R_L=500\Omega$, f = 10Hz	86		db
6	Common-mode Rejection	CMR	−25°C	±8.25V	$R_L=500\Omega$, f = DC, $V_{CM}=\pm2.25V$	70		db
5	Output Voltage, $I_O=3A$	V_O	85°C	±7V	$R_L=1\Omega$	3		V
5	Output Voltage, $I_O=36mA$	V_O	85°C	±19V	$R_L=500\Omega$	18		V
5	Output Voltage, $I_O=2A$	V_O	85°C	±12V	$R_L=5\Omega$	10		V
5	Stability/Noise	E_N	85°C	±15V	$R_L=500\Omega$, G = 1, $C_L=1.5nF$		1	mV
5	Slew Rate	SR	85°C	±15V	$R_L=500\Omega$	8.5	100	V/μs
5	Open Loop Gain	A_{OL}	85°C	±15V	$R_L=500\Omega$, f = 10Hz	86		db
5	Common-mode Rejection	CMR	85°C	±8.25V	$R_L=500\Omega$, f = DC, $V_{CM}=\pm2.25V$	70		db

BURN IN CIRCUIT:



*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

**Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

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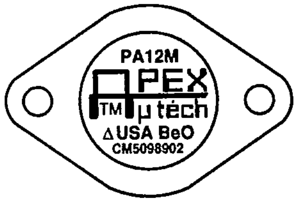
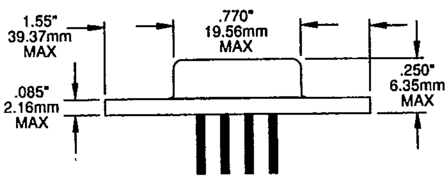
PACKAGE OUTLINE DIMENSIONS

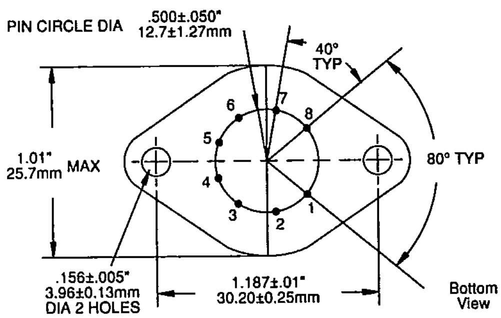
T-90-20

STANDARD 8 PIN TO-3



NOTE: ESD triangle (Δ) on top of package denotes pin 1 location.



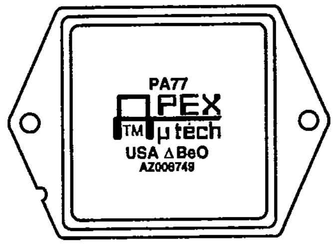


PIN DIAMETER:	.967/1.07mm or .038/.042"
PIN LENGTH:	11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated alloy 52, solderable
PIN MATERIAL, MIL:	Gold plated alloy 52, solderable
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	15 grams or .53 ounces
ISOLATION:	500VDC any pin to case
SOCKETS:	APEX PN: MS03
CAGE JACKS:	APEX PN: MS02 (Set of 8)
HEATSINKS:	APEX PN: HS01 thru HS05

CAUTION

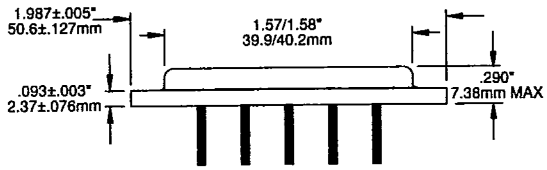
Recommended mounting torque is 4 – 7 in•lbs (.45 – .79 N•m)

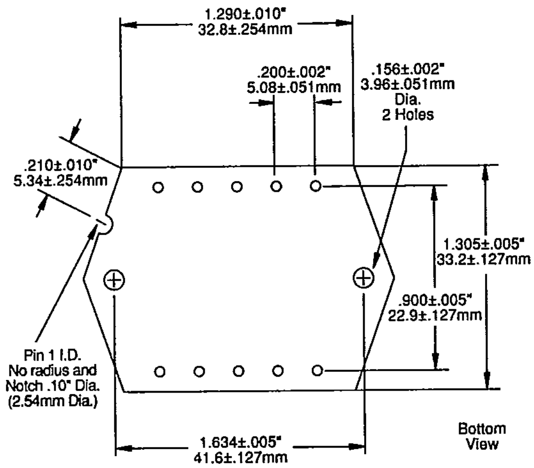
POWER PD10



NOTE: Notch on package base denotes pin 1 location.

PD10/60S





PIN DIAMETER:	1.47/1.58mm or .058/.062"
PIN LENGTH:	11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	36 grams or 1.27 ounces
ISOLATION:	500VDC any pin to case
CAGE JACKS:	MS04 (Set of 12)

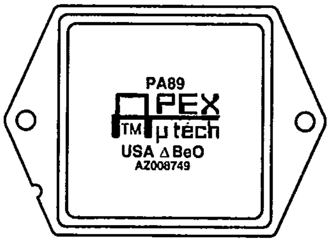
CAUTION

Recommended mounting torque is 8 – 10 in•lbs (.90 – 1.13 N•m)

PACKAGE OUTLINE DIMENSIONS

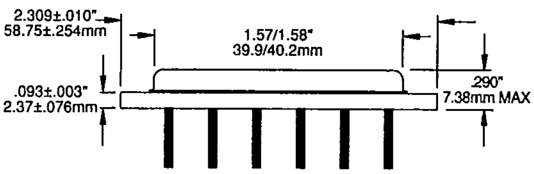
T-90-20

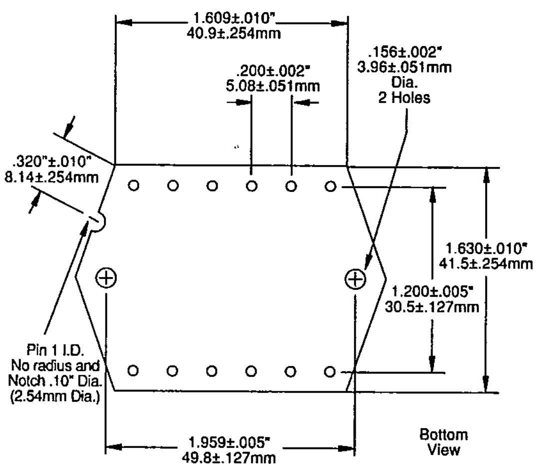
HIGH VOLTAGE PD12



NOTE: Notch on package base denotes pin 1 location.

PD12/25S



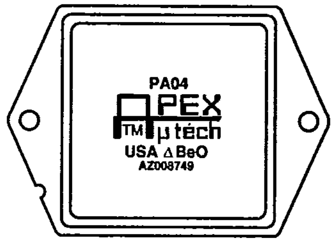


PIN DIAMETER:	.585/.687mm or .023/.027"
PIN LENGTH:	11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	53 grams or 1.87 ounces
ISOLATION:	1200VDC any pin to case

CAUTION

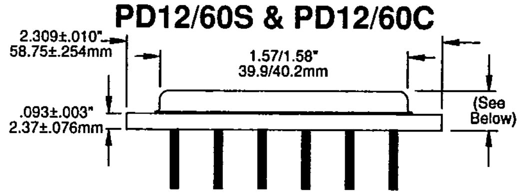
Recommended mounting torque is 8 – 10 in•lbs (.90 – 1.13 N•m)

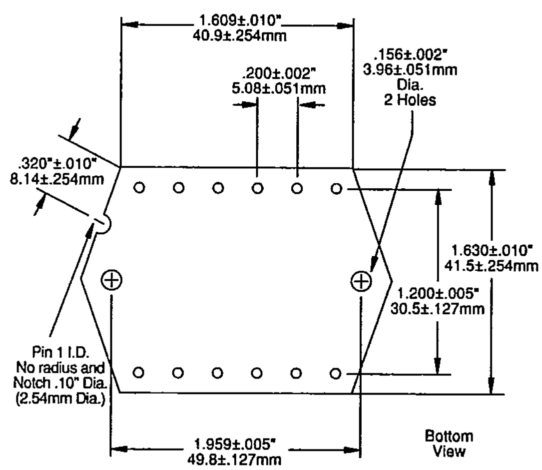
HIGH POWER PD12



NOTE: Notch on package base denotes pin 1 location.

PD12/60S & PD12/60C





PIN DIAMETER:		1.47/1.58mm or .058/.062"
PIN LENGTH:		11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:		Nickel plated steel
ISOLATION:	PD12/60S:	500VDC any pin to case
	PD12/60C:	300VDC any pin to case
HEIGHT:	PD12/60S:	7.38mm or .290" MAX
	PD12/60C:	8.90mm or .350" MAX
PACKAGE:	PD12/60S:	Hermetic, nickel plated steel
	PD12/60C:	Base: Nickel plated copper
	PD12/60C:	Cap: Hermetic, nickel plated steel
WEIGHT:	PD12/60S:	53 grams or 1.87 ounces
	PD12/60C:	58 grams or 2.05 ounces
CAGE JACKS:	Apex PN:	MS04 (Set of 12)
HEAT SINKS:	Apex PN:	HS06
MATING SOCKET:	Apex PN:	MS05

CAUTION Recommended mounting torque is 8–10 in•lbs (.90–1.13 N•m)