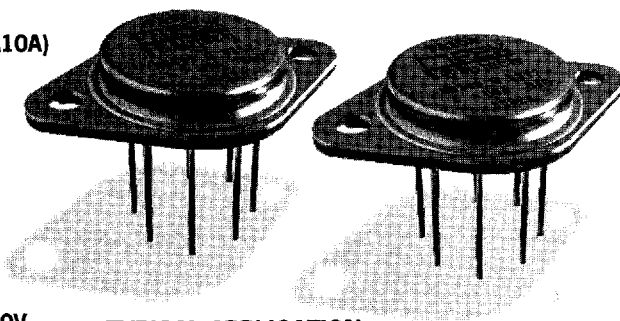# POWER OPERATIONAL AMPLIFIERS
PA10 • PA10A

APEX MICROTECHNOLOGY CORPORATION • APPLICATIONS HOTLINE 800 546-APEX (800-546-2739)

FEATURES

- **GAIN BANDWIDTH PRODUCT — 4MHz**
- **TEMPERATURE RANGE — –55 to +125°C (PA10A)**
- **EXCELLENT LINEARITY — Class A/B Output**
- **WIDE SUPPLY RANGE — ±10V to ±50V**
- **HIGH OUTPUT CURRENT — ±5A Peak**

APPLICATIONS

- **MOTOR, VALVE AND ACTUATOR CONTROL**
- **MAGNETIC DEFLECTION CIRCUITS UP TO 4A**
- **POWER TRANSDUCERS UP TO 100kHz**
- **TEMPERATURE CONTROL UP TO 180W**
- **PROGRAMMABLE POWER SUPPLIES UP TO 90V**
- **AUDIO AMPLIFIERS UP TO 60W RMS**

DESCRIPTION

The PA10 and PA10A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary darlington emitter follower output stages are protected against transient inductive kickback. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

EQUIVALENT SCHEMATIC
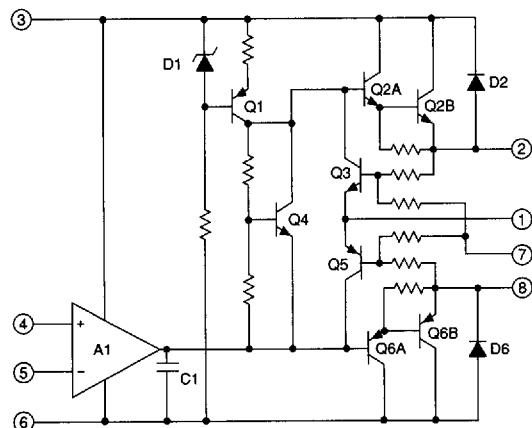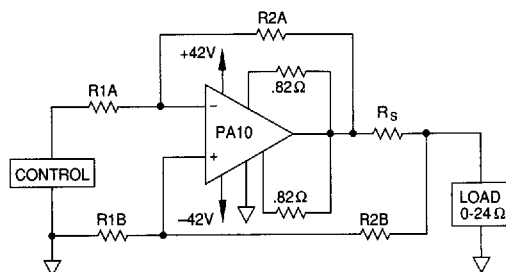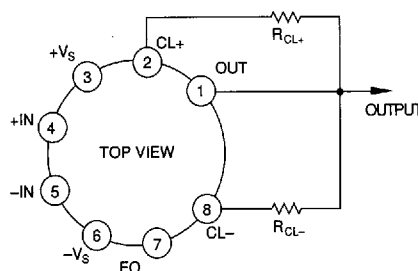

TYPICAL APPLICATION

FIGURE 1. VOLTAGE-TO-CURRENT CONVERSION

DC and low distortion AC current waveforms are delivered to a grounded load by using matched resistors (A and B sections) and taking advantage of the high common mode rejection of the PA10.

Foldover current limit is used to modify current limits based on output voltage. When load resistance drops to 0, the current is limited based on output voltage. When load resistance drops to 0, the current limit is 0.79A resulting in an internal dissipation of 33.3 W. When output voltage increases to 36V, the current limit is 1.69A. Refer to Application Note 9 on foldover limiting for details.

EXTERNAL CONNECTIONS

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PA10 • PA10A

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_s$ to $-V_s$	100V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal	67W
INPUT VOLTAGE, differential	$\pm V_s -3V$
INPUT VOLTAGE, common mode	$\pm V_s$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	−65 to +150°C
OPERATING TEMPERATURE RANGE, case	−55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA10 MIN	PA10 TYP	PA10 MAX	PA10A MIN	PA10A TYP	PA10A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	$T_C = 25°C$		±2	±6	±1		±3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65	*		±40	µV/°C
OFFSET VOLTAGE, vs. supply	$T_C = 25°C$		±30	±200	*		*	µV/V
OFFSET VOLTAGE, vs. power	$T_C = 25°C$		±20		*			µVW
BIAS CURRENT, initial	$T_C = 25°C$		12	30	10		20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±50	±500	*		*	pA/°C
BIAS CURRENT, vs. supply	$T_C = 25°C$		±10		*			pA/V
OFFSET CURRENT, initial	$T_C = 25°C$		±12	±30	±5		±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±50		*			pA/°C
INPUT IMPEDANCE, DC	$T_C = 25°C$		200		*			MΩ
INPUT CAPACITANCE	$T_C = 25°C$		3		*			pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_s -5$	$\pm V_s -3$		*	*		V
COMMON MODE REJECTION, DC[3]	Full temp. range, $V_{CM} = \pm V_s -6V$	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	$T_C = 25°C$, 1KΩ load		110			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 15Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	$T_C = 25°C$, 15Ω load		4			*		MHz
POWER BANDWIDTH	$T_C = 25°C$, 15Ω load	10	15		*	*		kHz
PHASE MARGIN	Full temp. range, 15Ω load		20			*		°
OUTPUT								
VOLTAGE SWING[3]	$T_C = 25°C$, $I_O = 5A$	$\pm V_s -8$	$\pm V_s -5$		$\pm V_s -6$	*		V
VOLTAGE SWING[3]	Full temp. range, $I_O = 2A$	$\pm V_s -6$			*			V
VOLTAGE SWING[3]	Full temp. range, $I_O = 80mA$	$\pm V_s -5$			*			V
CURRENT, peak	$T_C = 25°C$	5			*			A
SETTLING TIME to .1%	$T_C = 25°C$, 2V step		2			*		µs
SLEW RATE	$T_C = 25°C$	2	3		*	*		V/µs
CAPACITIVE LOAD	Full temperature range, $A_V = 1$			.68			*	nF
CAPACITIVE LOAD	Full temperature range, $A_V = 2.5$			10			*	nF
CAPACITIVE LOAD	Full temperature range, $A_V > 10$			SOA			*	nF
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±40	±45	*	*	±50	V
CURRENT, quiescent	$T_C = 25°C$	8	15	30	*	*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	$T_C = -55$ to $+125°C$, F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	$T_C = -55$ to $+125°C$		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air	$T_C = -55$ to $+125°C$		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	−25		+85	−55		+125	°C

NOTES:
* The specification of PA10A is identical to the specification for PA10 in applicable column to the left.
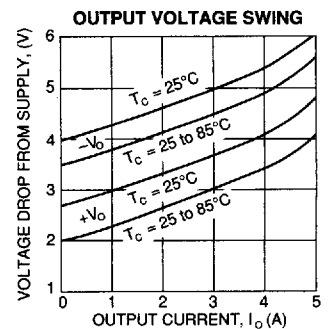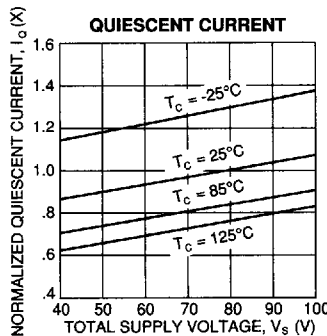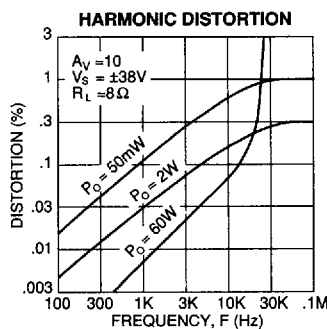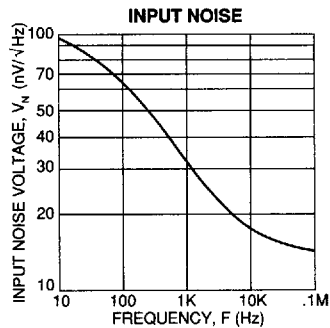1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

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TYPICAL PERFORMANCE
GRAPHS

PA10 • PA10A

POWER DERATING

BIAS CURRENT

CURRENT LIMIT

SMALL SIGNAL RESPONSE

PHASE RESPONSE

POWER RESPONSE

COMMON MODE REJECTION

PULSE RESPONSE

INPUT NOISE

HARMONIC DISTORTION

QUIESCENT CURRENT

OUTPUT VOLTAGE SWING

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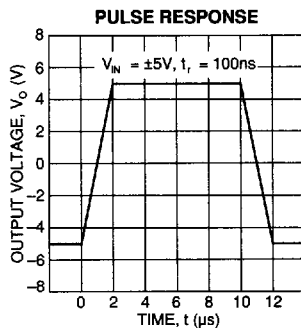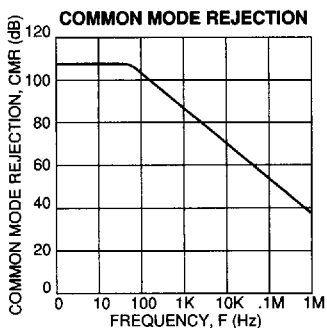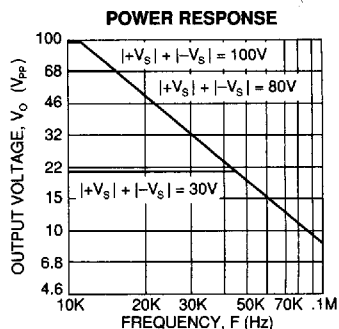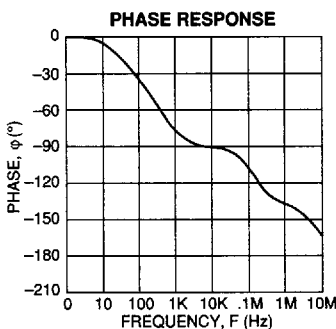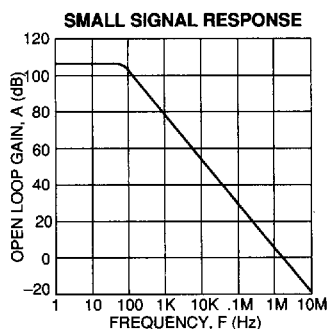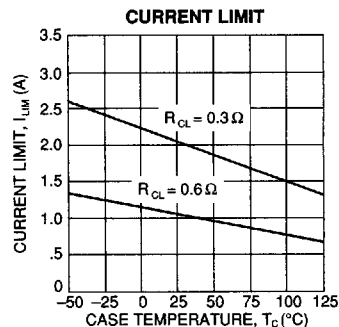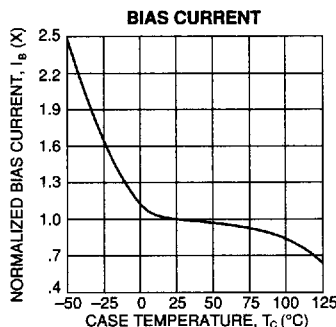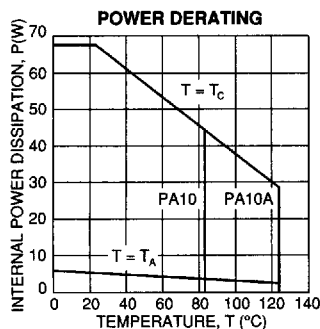
PA10 • PA10A

GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:
1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.
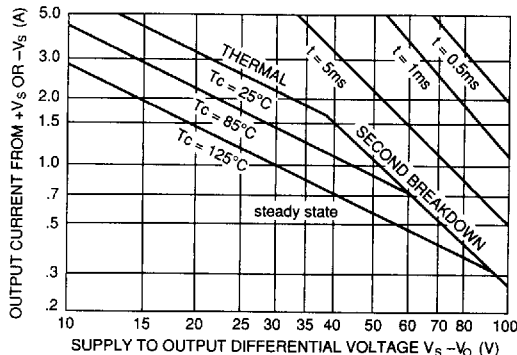
The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified.

±V_S	CAPACITIVE LOAD		INDUCTIVE LOAD	
	I_{LIM} = 2A	I_{LIM} = 5A	I_{LIM} = 2A	I_{LIM} = 5A
50V	80μF	75μF	55mH	7.5mH
40V	250μF	150μF	150mH	11mH
35V	500μF	250μF	200mH	15mH
30V	1,200μF	500μF	250mH	24mH
25V	4,000μF	1,600μF	400mH	38mH
20V	20,000μF	5,000μF	1,500mH	75mH
15V	**	25,000μF	**	100mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 5A or 20V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

**Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C = 85°C:

±V_S	SHORT TO ±V_S C, L, OR EMF LOAD	SHORT TO COMMON
50V	.26A	.84A
40V	.38A	1.1A
35V	.49A	1.2A
30V	.65A	1.4A
25V	.84A	1.7A
20V	1.1A	2.2A
15V	1.4A	2.9A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

CURRENT LIMITING

To use standard current limiting, leave pin 7 open and proceed per "General Operating Considerations" section of the handbook, where initial setting and variation with temperature are described. Foldover action is described in detail in Application Note 9.

For certain applications, foldover protection allows for increased output current as the output of the Power Op Amp swings close to the supply rail. This function can be achieved by connecting pin 7 directly or through a resistor to ground, and controlled by the following equation:

$$I_{LIM} = \frac{.65 + \dfrac{.28V_o}{20 + R_{FO}}}{R_{CL} + .01} \tag{1}$$

Where:
I_{LIM} is the current limit, in Amps, at a given output voltage V_o.
R_{FO} is the current foldover resistor pin 7 to ground in KΩ.
R_{CL} is the current limit resistor in Ω.
V_o is the instantaneous output voltage in V.*

*The basic equation assumes V_o and the current carrying supply are of the same polarity. If these polarities differ, assign V_o a negative value.
**.01Ω = wire bond and pin resistance to R_{CL} connections.

PROCEDURE

1. Select R_{CL} to provide a safe current limit at V_o = 0:

$$R_{CL} (\Omega) = (.65/I_{LIM}) - .01 \tag{2}$$

2. Find the current limit for the maximum output voltage swing and pin 7 connected to ground/common:

$$I_{LIM} = \frac{.65 + \dfrac{.28V_O}{20}}{R_{CL} + .01} \tag{3}$$

This is the highest current limit possible at maximum output. It may be decreased without affecting the short circuit current limit by putting a resistor in series with pin 7 to ground.

The following equation can be used to calculate R_{FD} (KΩ) using a lower current limit:

$$R_{FD} = \frac{.28V_O}{I_{LIM} (R_{CL} + .01) - .65} - 20 \tag{4}$$

3. To calculate the current limit at any output voltage (V_o), use equation "one". If V_o is of opposite polarity to the current carrying supply, assign V_o a negative value and check the calculated current against the SOA graph.

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TABLE 4 GROUP A INSPECTION
PA10M/SMD 5962-9082801HXX

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SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		30	mA
1	Input offset voltage	V_{OS}	25°C	±40V	V_{IN} = 0, A_V = 100		±6	mV
1	Input offset voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±12	mV
1	Input offset voltage	V_{OS}	25°C	±45V	V_{IN} = 0, A_V = 100		±7	mV
1	Input bias current, +IN	$+I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Input bias current, −IN	$-I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Input offset current	I_{OS}	25°C	±40V	V_{IN} = 0		±30	nA
3	Quiescent current	I_Q	−55°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		75	mA
3	Input offset voltage	V_{OS}	−55°C	±40V	V_{IN} = 0, A_V = 100		±11.2	mV
3	Input offset voltage	V_{OS}	−55°C	±10V	V_{IN} = 0, A_V = 100		±17.2	mV
3	Input offset voltage	V_{OS}	−55°C	±45V	V_{IN} = 0, A_V = 100		±12.2	mV
3	Input bias current, +IN	$+I_B$	−55°C	±40V	V_{IN} = 0		±115	nA
3	Input bias current, −IN	$-I_B$	−55°C	±40V	V_{IN} = 0		±115	nA
3	Input offset current	I_{OS}	−55°C	±40V	V_{IN} = 0		±115	nA
2	Quiescent current	I_Q	125°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		30	mA
2	Input offset voltage	V_{OS}	125°C	±40V	V_{IN} = 0, A_V = 100		±12.5	mV
2	Input offset voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±18.5	mV
2	Input offset voltage	V_{OS}	125°C	±45V	V_{IN} = 0, A_V = 100		±13.5	mV
2	Input bias current, +IN	$+I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input bias current, −IN	$-I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input offset current	I_{OS}	125°C	±40V	V_{IN} = 0		±70	nA
4	Output voltage, I_O = 5A	V_O	25°C	±18V	R_L = 2.07Ω	10		V
4	Output voltage, I_O = 80mA	V_O	25°C	±45V	R_L = 500Ω	40		V
4	Output voltage, I_O = 2A	V_O	25°C	±30V	R_L = 12Ω	24		V
4	Current limits	I_{CL}	25°C	±16.5V	R_L = 2.07Ω, R_{CL} = .2Ω	2.6	3.9	A
4	Stability/noise	E_N	25°C	±40V	R_L = 500Ω, A_V = 1, C_L = .68nF		1	mV
4	Slew rate	SR	25°C	±40V	R_L = 500Ω	2	10	V/μs
4	Open loop gain	A_{OL}	25°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
4	Common mode rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
6	Output voltage, I_O = 5A	V_O	−55°C	±18V	R_L = 2.07Ω	10		V
6	Output voltage, I_O = 80mA	V_O	−55°C	±45V	R_L = 500Ω	40		V
6	Output voltage, I_O = 2A	V_O	−55°C	±30V	R_L = 12Ω	24		V
6	Stability/noise	E_N	−55°C	±40V	R_L = 500Ω, A_V = 1, C_L = .68nF		1	mV
6	Slew rate	SR	−55°C	±40V	R_L = 500Ω	2	10	V/μs
6	Open loop gain	A_{OL}	−55°C	±40V	R_L = 500Ω, F = 10Hz	96		db
6	Common mode rejection	CMR	−55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
5	Output voltage, I_O = 3A	V_O	125°C	±14.3V	R_L = 2.07Ω	6.3		V
5	Output voltage, I_O = 80mA	V_O	125°C	±45V	R_L = 500Ω	40		V
5	Output voltage, I_O = 2A	V_C	125°C	±30V	R_L = 12Ω	24		V
5	Stability/noise	E_N	125°C	±40V	R_L = 500Ω, A_V = 1, C_L = .68nF		1	mV
5	Slew rate	SR	125°C	±40V	R_L = 500Ω	2	10	V/μs
5	Open loop gain	A_{OL}	125°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
5	Common mode rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB

BURN IN CIRCUIT
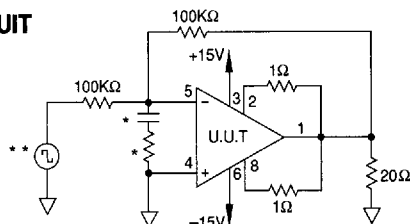
*   These components are used to stabilize device due to poor high frequency characteristics of burn in board.

**   Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.