PA50000 Series

T-42-11-09

These data sheets are provided for technical guidance only. The final device performance may vary depending upon the final device design and configuration.

Silicon-Gate CMOS Logic Arrays

Features:

- *Silicon-gate 3-micron CMOS technology*
- *Schottky TTL speeds - 2.5 ns through 2-input NAND gate and interconnection, T_A = 25° C, fanout = 2, V_{DD} = 5 V*
- *Optimal block structure of 2N and 2P transistors*
- *Complexities ranging from 880 to 6000 blocks*
- *Pin counts ranging up to 180*
- *Extensive macrocell and macrofunction libraries*
- *All non-power pads configurable as inputs, outputs or bidirectional*
- *TTL/CMOS I/O compatibility*
- *Configurable output drive up to 6 mA*
- *All inputs and outputs protected from overvoltage and latch-up*
- *Full military capability*
- *Ceramic packages*
- *Alternately sourced*
- *PA52200Q evaluation device available*

The industry-standard PA50000 series of silicon-gate CMOS logic arrays from GE/RCA are a high-density, high-performance family, with speeds that match fast bipolar technologies such as Schottky TTL. At the same time, they offer the low power consumption, high noise margins, and ease of design of CMOS technology. The PA50000 series is implemented in 3-micron drawn gate length, two-layer metal interconnection technology. A range of complexities from 880 to 6000 blocks is offered. Each block is equivalent to a 2-input NAND or NOR gate. Maximum pin counts range from 74 to 180.

The speeds and densities of the PA50000 series make it suitable for LSI implementation of complete, high-performance functions such as special processors, dedicated peripheral controllers and intelligent support chips. It is also ideal for replacement of LS/S TTL logic in medium-and high-speed systems. IC count can be reduced by factors of tens to hundreds depending on the density of the array used. Power requirements can be reduced by several orders of magnitude, reliability significantly enhanced and the total size and cost of the system similarly reduced.

SERIES OUTLINE

Device Number	Gate Complexity	Max[3] I/O	V_{DD} Pads	V_{SS} Pads	Max Pads	Gate Speed (ns)[1]	
						Typ.	Max.[2]
PA50800	880	66	2	6	74	2.5	4.5
PA51400	1404	84	2	6	92	2.5	4.5
PA52200	2224	106	2	6	114	2.5	4.5
PA53200	3192	130	2	6	138	2.5	4.5
PA54200	4202	144	4	8	156	2.5	4.5
PA56000	6000	168	4	8	180	2.5	4.5

Notes: 1. 2-input NAND gate, fanout = 2, and typical interconnection
2. T_A = -55 to +125° C, V_{DD} = 5 V ±5%
3. It may be necessary to configure additional I/O pads for V_{DD} and V_{SS}, depending on the number and drive of the outputs buffers. See section on V_{DD} and V_{SS} Requirements."

MAXIMUM RATINGS, *Absolute-Maximum Values:*
(Voltages referenced to V_{SS} Terminal)

DC SUPPLY-VOLTAGE (V_{DD}) ..... -0.5 to +7 V
DC SUPPLY OPERATING VOLTAGE RANGE (V_{DD}) ..... 2 to 6 V
DC INPUT VOLTAGE RANGE, ALL INPUTS (V_{IN}) ..... -0.5 to V_{DD} +0.5 V
DC OUTPUT VOLTAGE RANGE, ALL OUTPUTS (V_{OUT}) ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±1 mA
POWER DISSIPATION PER PACKAGE (P_D):
For External Temperature Range -55 to +125° C
For T_A = -55 to +100° C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/° C to 200 mW
POWER DISSIPATION PER OUTPUT ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D (CERAMIC) ..... -55 to +125° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265° C

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STATIC ELECTRICAL CHARACTERISTICS

Specified at V_{DD} = 5V ± 5% ambient temperature over the specified temperature range(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage					
	TTL Inputs		—	—	0.8	V
	CMOS Levels.		—	—	1.5	V
V_{IH}	High Level Input Voltage					
	TTL Inputs, Commercial Temperature Range		2.0	1.7	—	V
	TTL Inputs, Military and Industrial Temperature Range		2.25	1.7	—	V
	CMOS Levels		3.5	3.0	—	V
V_{T+}	Schmitt-Trigger, Positive-going Threshold		—	3.0	4.0	V
V_{T-}	Schmitt-Trigger, Negative-going Threshold		1.0	1.5	—	V
Π	Hysteresis, Schmitt Trigger	V_{IL} to V_{IH} V_{IH} to V_{IL}	1.0	1.5	—	V V
I_{IN}	Input Current, CMOS, TTL Inputs	$V_{IN} = V_{DD}$	-10	±1	10	µA
	Inputs with pull-down resistors	$V_{IN} = V_{DD}$	—	5	20	µA
	CMOS inputs	$V_{IN} = V_{SS}$	-10	±1	10	µA
	TTL Inputs & Inputs with Pull-up Resistors	$V_{IN} = V_{SS}$	-20	-5		µA
V_{OH}	High Level Output Voltage					
	Type B14	I_{OH} = -0.3mA				
	Type B18	I_{OH} = -0.6mA	2.4	4.5	—	V
	Type B1	I_{OH} = -1.5mA				
	Type B2 (2)	I_{OH} = -3.0mA				
	Type B3 (3)	I_{OH} = -4.5mA				
V_{OL}	Low Level Output Voltage					
	Type B14	I_{OL} = 0.5mA				
	Type B18	I_{OL} = 1.0mA		0.2	0.4	V
	Type B1	I_{OL} = 2.0mA	—			
	Type B2 (2)	I_{OL} = 4.0mA				
	Type B3 (3)	I_{OL} = 6.0mA				
I_{OZ}	Three-State Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DD}	-10	±1	10	µA
I_{OS}	Output Short Circuit Current (4)	V_{DD} = Max $V_O = V_{DD}$ V_{DD} = Max, V_O = 0V	25 -7	— —	90 -28	mA mA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}	User-Design Dependent			
C_{IN}	Input Capacitance	Any Input (5)	5			pF
C_{OUT}	Output Capacitance	Any Output (6)	7			pF

Notes:
1. Military temperature range is -55°C to +125°C (ceramic packages only).
2. Requires two output pads.
3. Requires three output pads.
4. Type B1 output. Output short circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.
5. Not applicable to assigned bi-directional buffer (excluding package).
6. Output using single buffer structure (excluding package).

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DYNAMIC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, T_A = 25° C

Note: Delays through interconnect are included. Interconnect wirelengths are assumed from statistical distributions for given fanouts.

Macrocell	Input Transition	Propagation Delays					Equivalent Gate Count
		Output Load Capacitance					
		15pF	50pF	85pF	100pF		
UNIDIRECTIONAL BUFFERS							
3-state Output Buffer with 0.5mA Drive (BTS14)	t_{PHL} t_{PLH}	10.2 4.7	28.3 12.7	46.3 20.8	54.0 24.2		5
3-state Output Buffer with 6.0mA Drive (BTS3)	t_{PHL} t_{PLH}	6.3 6.8	7.7 7.9	9.1 9.0	9.7 9.5		5
THREE-STATE BIDIRECTIONAL BUFFERS							
3-state I/O Buffers with 2.0mA Drive (BTS7)	t_{PHL} t_{PLH}	5.0 5.5	9.1 8.7	13.2 11.9	14.9 13.3		7
3-state I/O Buffers with Pull-up (BTS7U)/Pull-down (BTS7D)	t_{PHL} t_{PLH}	5.0 5.5	9.1 8.7	13.2 11.9	14.9 13.3		7
OUTPUT BUFFERS							
Output Buffer with 0.5mA Drive (B14)	t_{PHL} t_{PLH}	10.2 4.7	28.3 12.7	46.3 20.3	54.0 24.2		1
Output Buffer with 6.0mA Drive (B3)	t_{PHL} t_{PLH}	4.2 5.2	5.5 6.2	6.9 7.3	7.5 7.8		2
		Fanout					
		1	2	3	4	8	
INPUT RECEIVERS							
Input Buffer with CMOS Inputs (IBUF)	t_{PHL} t_{PLH}	0.9 0.9	1.0 1.0	1.1 1.1	1.2 1.2	1.4 1.5	0
Input Buffer with Schmitt Trigger (SCHMIT1)	t_{PHL} t_{PLH}	7.8 4.4	8.0 4.8	8.1 5.2	8.3 5.5	8.7 6.5	3
Input Buffer with TTL Inputs (TLCHT)	t_{PHL} t_{PLH}	3.8 1.6	4.0 2.0	4.1 2.4	4.1 2.7	4.5 3.7	0
INTERNAL BUFFERS							
Single Inverter (IV)	t_{PHL} t_{PLH}	1.3 2.2	1.7 3.1	1.9 3.7	2.2 4.3	3.2 6.5	1
Power Inverter (IVP)	t_{PHL} t_{PLH}	1.2 1.9	1.5 2.5	1.9 3.6	2.7 5.4	5.2 10.9	1-2
Internal Pull-up (PUI)	t_{PLH}	1.7	2.4	3.1	3.7	6.5	1
Internal Pull-down (PDI)	t_{PHL}	1.7	2.1	2.4	2.7	3.6	1
LOGIC GATES							
2-input NAND (ND2)	t_{PHL} t_{PLH}	1.7 2.4	2.4 3.3	2.9 3.9	3.4 4.5	5.0 6.7	1
2-input NOR (NR2)	t_{PHL} t_{PLH}	1.4 3.8	1.8 5.5	2.0 6.8	2.3 7.9	3.3 11.9	1
2-input Exclusive OR(EO)	t_{PHL} t_{PLH}	4.8 5.3	5.4 7.0	5.9 8.2	6.4 9.4	8.0 13.4	3
3-input NAND (ND3)	t_{PHL} t_{PLH}	3.0 3.0	3.9 3.9	4.6 4.6	5.2 5.2	7.5 7.4	2
3-input NOR (NR3)	t_{PHL} t_{PLH}	1.6 6.9	2.0 9.4	2.3 11.2	2.6 12.8	3.5 18.9	2

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DYNAMIC ELECTRICAL CHARACTERISTICS (Cont'd)

V_{DD} = 5V, T_A = 25°C

Macrocell	Input Transition	Propagation Delays (Fanout 1)	Fanout 2	Fanout 3	Fanout 4	Fanout 8	Equivalent Gate Count
LOGIC GATES							
4-input NAND (ND4)	t_{PHL}	3.9	5.2	6.1	7.0	10.0	2
	t_{PLH}	3.4	4.2	4.9	5.5	7.7	
4-input NOR (NR4)	t_{PHL}	1.6	2.0	2.3	2.5	3.5	2
	t_{PLH}	9.5	12.7	15.2	17.4	25.3	
8-input NAND/2 4-input NANDs into 2-input NOR into Inverter (ND8)	t_{PHL}	7.2	7.4	7.5	7.7	8.1	6
	t_{PLH}	4.8	5.3	5.6	5.9	7.0	
8-input NOR/2 4-input NANDs into 2-input NAND into Inverter (NR8)	t_{PHL}	4.3	4.5	4.6	4.8	5.2	6
	t_{PLH}	9.1	9.6	9.9	10.2	11.2	
FLIP-FLOPS							
D Flip-flop (FD1)	t_{PHL}	4.8	5.2	5.5	5.8	6.7	5
	t_{PLH}	6.5	7.3	8.0	8.6	10.7	
	t_S	0.5	0.5	0.5	0.5	0.5	
	t_H	0.5	0.5	0.5	0.5	0.5	
D Flip-flop with Scan Test Inputs (FD1S)	t_{PHL}	7.2	7.6	7.9	8.1	9.1	7
	t_{PLH}	6.7	7.6	8.2	8.8	10.9	
	t_S	6.0	6.0	6.0	6.0	6.0	
	t_H	-0.5	-0.5	-0.5	-0.5	-0.5	
D Flip-flop with Set Direct, Clear Direct (FD3)	t_{PHL}	5.7	6.4	6.9	7.3	8.9	7
	t_{PLH}	6.7	7.5	8.2	8.8	10.9	
	t_S	0.5	0.5	0.5	0.5	0.5	
	t_H	0.5	0.5	0.5	0.5	0.5	
D Flip-flop with Set Direct, Clear Direct, and Scan Test Inputs (FD3S)	t_{PHL}	8.1	8.8	9.3	9.8	11.3	9
	t_{PLH}	7.4	8.2	8.9	9.5	11.6	
	t_S	6.0	6.0	6.0	6.0	6.0	
	t_H	-0.5	-0.5	-0.5	-0.5	-0.5	
J-K Flip-flop (FJK1)	t_{PHL}	4.8	5.2	5.5	5.8	6.7	8
	t_{PLH}	6.5	7.3	8.1	8.6	19.7	
	t_S	4.5	4.5	4.5	4.5	4.5	
	t_H	-3.0	-3.0	-3.0	-3.0	-3.0	
J-K Flip-flop with Scan Test Inputs (FJK1S)	t_{PHL}	5.1	7.4	7.8	8.1	8.4	10
	t_{PLH}	7.0	7.2	8.1	8.8	9.4	
	t_S	9.0	9.0	9.0	9.0	9.0	
	t_H	-4.5	-4.5	-4.5	-4.5	-4.5	
LATCHES							
Gated D Latch (LD1)	t_{PHL}	6.2	6.6	6.9	7.1	8.1	3
	t_{PLH}	7.6	8.4	9.1	9.7	11.8	
	t_S	0.0	0.0	0.0	0.0	0.0	
	t_H	2.0	2.0	2.0	2.0	2.0	
S-R Latch with Separate Input Gates, Set Direct and Reset Direct (LSR1)	t_{PHL}	3.9	4.6	5.2	5.8	8.0	4
	t_{PLH}	6.1	7.3	8.5	9.5	13.4	
D Latch with Scan Test Inputs (LS1)	t_{PHL}	5.1	5.5	5.8	6.1	7.0	6
	t_{PLH}	6.0	6.8	7.5	8.1	10.2	
	t_S	2.0	2.0	2.0	2.0	2.0	
	t_H	0.5	0.5	0.5	0.5	0.5	
MISCELLANEOUS							
8-to-1 Multiplexer (MUX8)	t_{PHL}	8.7	9.3	9.8	10.2	11.9	13
	t_{PLH}	11.4	13.1	14.4	15.5	19.6	

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Package Options
See "Packages for High-Reliability ASICs" where indicated by the section outline of this section.

PA52200Q Evaluation Device
A potential user of the PA50000 series can, prior to design commencement, measure its performance under his unique system and environmental conditions. The PA52200Q contains a variety of logic functions such as 2-, 3-, or 4-input NAND gates, 2- or 4-input NOR gates, output buffers with different drive capability, a variety of different flip-flops, inverters, and TTL-to-CMOS level-shifters. These functions are implemented in several different test circuits. Technology parameters such as propagation delays, power consumption, and input/output characteristics can be measured under different conditions of parameters such as loading, supply voltage, and ambient temperature. See the PA52200Q data sheet for more details.

Product Description
The PA50000 series of arrays are manufactured using a proven 3-micron, oxide-isolated silicon-gate CMOS fabrication process. The low parasitic capacitance of the oxide-isolated devices and their small channel geometries provide high performance. Propagation delays through a 2-input NAND gate average 2.5 ns. Two layers of metal are used for interconnection, allowing high utilization, ease of wireability and high performance.

Macrocells
The arrays consist of columns of blocks in the core region, I/O buffers around the periphery, and wiring channels in between. The typical organization is shown in Fig. 1. Each block consists of 2N and 2P transistors. Thus, a block can implement complete basic functions such as a 2-input NAND or 2-input NOR gate. Array complexities are stated in terms of the number of blocks or, equivalently, 2-input NAND gates. The individual N and P transistors in a block are not pre-connected. They can be configured into a variety of logic elements such as exclusive-OR gates or flip-flops using unique metal interconnections. These elements are called macrocells. The PA50000-series macrocell library contains approximately 150 macrocells with new elements being defined regularly. The Dynamic Electrical Characteristics chart lists some of the commonly used macrocells, their propagation delays, and their complexity measured in blocks.

Macrocells for Level-Sensitive Scan Design
The PA50000-series macrocell libraries also contain macrocells needed to support scan testing. Scan testing simply involves the capability to serially shift the contents of all internal flip-flops off-chip in a test mode.

All that is required to select scan-testable storage logic elements is to add an 'S' suffix to each applicable macrocell reference, and two input entries, Test Enable and Test Source, in the netlist. See Fig. 2.

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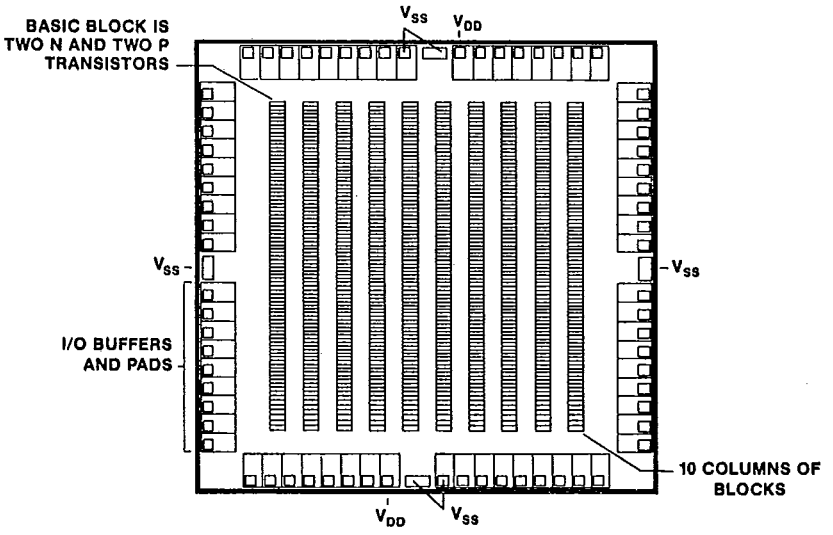

Fig. 1 - The PA50800 array organization shown is typical of the PA50000 series.

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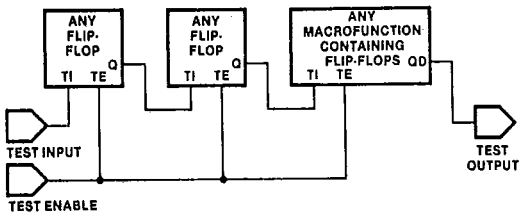

Fig. 2 - Scan testing may be added easily to any macrofunction.

Macrofunctions
Macrocells are the basic building blocks available to the user. To specify his logic, the user builds elements of greater complexity from macrocells. These more complex elements are called macrofunctions. Simple macrofunctions are in turn used to hierarchically build higher-level macrofunctions until the logic is completely specified.

For user convenience, a selection of macrofunctions composed of macrocells is also available in the PA50000-series library. These macrofunctions implement generic functions such as counters, decoders, and shift registers, and are optimized for gate usage and performance characteristics. Under some circumstances, such as for upgrading existing products using 7400/4000-series MSI/SSI functions, or because of previous familiarity, designers may prefer to use 7400/4000-series functions as building blocks. GE/RCA also provides a selection of these elements. Overall, over 200 macrofunctions are available in the PA50000-series library, and new ones are added regularly. Table II lists some representative macrofunctions. Detailed information on available macrocells and macrofunctions is provided in other GE/RCA publications.

I/O Buffers
Each I/O buffer around the perimeter of the array consists of an input protection circuit and large N- and P-channel transistors for driving off-chip loads. 2-4 dedicated power pads and 6-8 dedicated ground pads are provided. All the remaining peripheral cells can be used as input, output, bi-directional tri-state, power, or ground pads. If necessary, they can even be used to buffer heavily loaded internal signals.

Further flexibility is available in the use of pull-ups/pull-downs and choice of input levels and current drive:
- All I/O pads have pull-up and pull-down resistors available (typically 1 megohm).
- Output drive may be tailored to 0.5 mA, 1 mA or 2 mA. Additional drive capability may be obtained by paralleling two (4 mA) or three (6 mA) drivers.
- Three-input voltage level options are available on any input/output pin. CMOS input buffers provide standard 1.5- and 3.5-volt input levels. TTL input buffers provide standard 0.8 and 2-volt (2.25-volt on industrial and military devices) input levels. Schmitt trigger inputs provide 1.5 volts of hysteresis. See the Static Electrical Characteristics chart for more details.
- All I/O's are protected against latch-up and static discharge.

Propagation Delays
Propagation delays of the PA50000 series logic elements are a function of several factors:
- fanout
- interconnection routing
- junction temperature
- supply voltage
- processing tolerance
- input transition time
- input signal polarity

The GE/RCA design verifier program generates the propagation delays for all networks automatically once the network has been entered into the development system. Prior to layout, these values are based on the estimated interconnections. After layout, the program is rerun and final delay values based on actual interconnections are obtained.

Prior to availability of the network in computer format, approximate delay calculations may be used. This may be done as follows:

Propagation delays for some popular macrocells are shown in the Dynamic Electrical Characteristics chart for nominal processing, 5-V operation, 25°C temperature and for various fanouts, with statistically estimated wire-lengths.

The effect of temperature may be estimated from Fig. 3.

Table II - Representative Macrofunctions Available in the PA50000 Series

ADDERS
Full adder
2-bit binary full adder similar to 7482

COMPARATORS
4-bit magnitude comparator similar to 7485
8-bit equality comparator

PARITY GENERATORS
8-bit odd parity detector

REGISTERS
8-bit data latch
8-bit data register, clear direct
4-bit shift register, sync parallel load and clear
4-bit shift register, async parallel load

COUNTERS
Binary, BCD, Gray and Johnson counters in a variety of configurations
Large modulo counters

CLOCK GENERATORS
Two-phase clock generator, buffered

DECODERS
2-to-4 decoders
3-to-8 decoders
4-to-10 decoders

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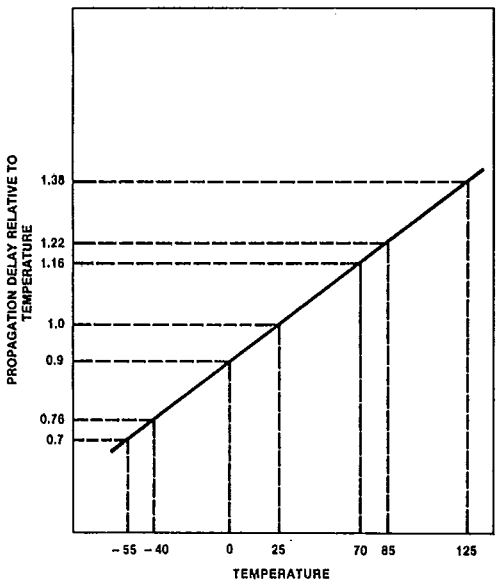

Fig. 3 - CMOS propagation delays as a function of temperature.

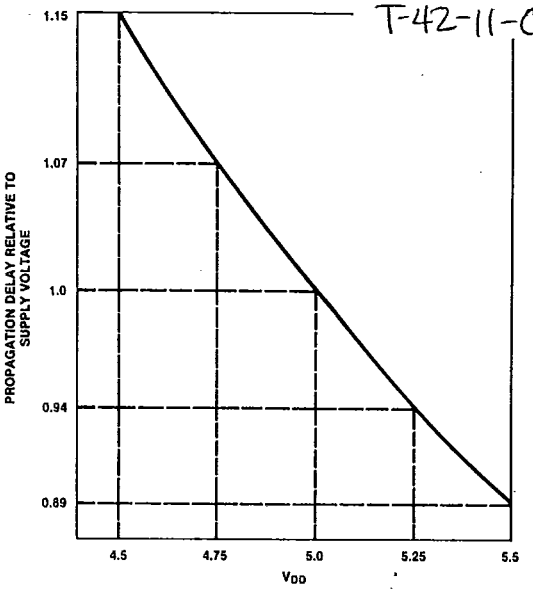

Fig. 4 - CMOS propagation delays as a function of supply voltage

The maximum junction temperature will determine a temperature multiplier (K_T). In CMOS technology, the junction temperature is usually close to the ambient temperature. Similarly, Fig. 4 shows the effect of supply voltage (K_V). GE/RCA assumes a maximum 40% variability resulting from all other factors including processing, or in other words, a factor of 1.4 for the worst-case multiplier for all other factors (K_O).

The maximum propagation delay is:

$T_{MAX} = K_O \bullet K_T \bullet K_V \bullet T_{TYP}$

A simple example will illustrate the technique.

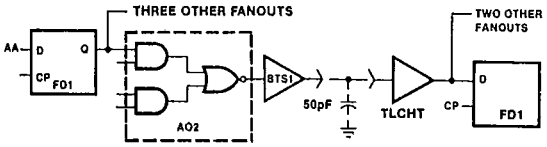

Fig. 5 - Example of worst-case propagation delay through critical path.

The circuit of Fig. 5 must operate over -55°C to +125°C, and 4.75 V to 5.25 V power supply voltage. Using Figs. 3 and 4 and the K_O multiplier, we determine the worst-case maximum delay to be 1.4 x 1.38 x 1.07 = 2.07 times the typical delay.

The FD1 flip-flop, driven by the signal AA, feeds an AO2 AND-NOR gate combination and three other loads. The AO2 drives a BTS1 3-state buffer directly. The BTS1 drives off-chip, through a PC board, and on to another array using a TLCHT input level shifter. The total capacitance at the output, interconnect, and input is 50 pF. The TLCHT drives the D input of an FD1 D flip-flop and two other loads. The delay characteristics of all the macrocells are tabulated in Table III. The total clock-to-clock delay is 27 ns typical, 27 x 2.07 = 56 ns worst-case. GE/RCA Design System programs are used to obtain accurate delays after the logic has been entered into the system.

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Table III - Propagation Delay Calculation

Input Signal AA	FD1 FO=4	AO2 FO=1	3-state Output BTS1 C_L=50pF	TLCHT FO=3	FD1 Set-up	Typical Path Delay	W.C. Path Delay
Goes high	8.6	4.4	9.4	4.1	0.5	27.0	47.0
Goes low	5.8	2.3	8.6	2.4	0.5	19.6	34.1

V_{DD} and V_{SS} Requirements

CMOS is a fast technology rivaling Schottky TTL speeds. High-speed operation places stringent requirements on the ground busing and the number of power and ground pads required to avoid current spikes when the output buffers charge and discharge their output capacitance.

To increase noise immunity, two ground buses are used on the array. All inputs and interior logic are on one bus, all output buffers on a second. These two buses are connected together on a single ground pad.

More than two power (V_{DD}) and ground (V_{SS}) pads may be required to support several high-drive outputs switching simultaneously at fast speeds. For example, the type B1 buffer has a low impedance for high drive capability and may provide a peak transient current of 50 mA. If sixteen B1

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buffers switch simultaneously, a peak current of nearly one amp is generated through the V_{SS} bus, bonding wire, package and out to the PC board. There are, therefore, guidelines on the number of V_{SS} and V_{DD} pins based on three factors:

- the drive capability of the buffer
- the number of buffers switching simultaneously
- the location of power and ground pads relative to the outputs

Each power and ground pad can support a maximum of 64 current units, where a current unit is the peak drive capability of a B14 buffer (max. drive = 0.5 mA). Thus, the sum of the possible current units of all the outputs around a V_{DD} or V_{SS} pad should not exceed 64 current units. Output types can be mixed—high drive when needed, low drive when acceptable to reduce noise and power dissipation. Note that inputs are not taken into account since CMOS inputs sink and source minimal current. Table IV summarizes the guidelines for the maximum number of output pads for a power or ground pad for each buffer type. Further, the 64 current units should be distributed as equally as possible on either side of the power or ground pad, i.e., no signal should be more than 32 current units away from a power or ground pad (see Fig. 6).

Table IV - Maximum Number of Output Pads for Each Buffer Type

Buffer Type	Drive (Current Units*)	Maximum Number of Output Pads for each V_{DD} or V_{SS} Pad
B14	1	64
B18	2	32
B1	4	16
B2	8	8
B3	12	5

*Current Unit = 0.5mA

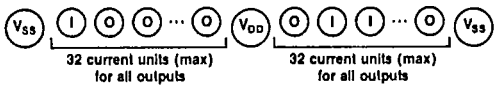

Fig. 6 - Ideal distribution of power, ground and output pads.

Power Dissipation

Power dissipation in CMOS circuits is made up of four basic elements.

The first is due to leakage. It constitutes the quiescent power dissipation and is essentially negligible (few microwatts) for CMOS technology.

The second is dc current through ON transistors. This can be from a variety of sources:

- a low on an input with a pull-up resistor (all TL inputs have 1-megohm nominal pull-up resistors)
- outputs which sink or source current
- any unconnected inputs without a pull-up or pull-down
- any internal gates whose inputs are floating (e.g., a data bus with all the lines disabled)
- inputs at worst-case levels, particularly TTL inputs at 2 volts

Care should be exercised during logic design to make sure that there is a test condition in which all this dc current may be turned off, so that dc leakage may be easily measured.

The third source of power dissipation is due to overlap currents when the P- and N-transistors are switching from the high-to-low state or vice-versa. This contributes less than 10% of the power dissipated and occurs for the transition period when $V_{THI(N)} < V_{IN} < V_{DD} - V_{THI(P)}$.

The fourth and the most important factor is the charging and discharging of circuit capacitance. The charging of a capacitor C to a voltage V through a P-channel device builds up a charge CV and stores energy CV^2. This energy is later discharged through an N-channel transistor in the CMOS P-N pair. When such switching takes place at a frequency "f," the resultant power dissipated in the CMOS circuit is equivalent to $P = CV^2f$. This ac power dissipation usually contributes in excess of 90% of the total power dissipated. Thus, the power dissipation in a CMOS circuit is essentially a function of the frequency and logic configuration. Each internal gate in the PA50000 series typically consumes 20 microwatts/gate/MHz. Each I/O buffer, with its higher output capacitance and larger capacitive loads, consumes 25 microwatts/I/O/MHz/pF. The total power consumption is the sum of the power dissipated by all the gates and I/O buffers switching each cycle. For a specific design, it can be estimated as shown for the examples in Table V. In our experience, even large arrays operating at high clock rates seldom dissipate more than 500 mW.

Table V - Power Dissipation Calculation

Parameter	Array Type	
	PA52200	PA56000
Number of available gates	2224	6000
Percentage of gates utilized (%)	85	75
Number of gates utilized	1890	4500
Number of gates switching each cycle (15%)	284	675
Dissipation/gate/MHz (μW)	20	20
Total core dissipation/ MHz (mW)	5.7	13.5
Number of available I/O buffers	106	168
Percentage of I/O buffers utilized (%) as outputs	50	50
Number of I/O buffers utilized as outputs	53	84
Number of I/O outputs switching each cycle (20%)	11	17
Dissipation/output buffer/ MHz/pf (μW)	25	25
Output Capacitive Load (pF)	50	50
Dissipation/output buffer/ MHz (mW)	1.25	1.25
Total output buffer dissipation/MHz (mW)	13.8	21.3
Total dissipation/MHz (mW)	19.5	34.8
Total dissipation at 10MHz clock speed (mW)	195	348
Total dissipation at 25MHz clock speed (mW)	487	870