



PA7140 PEELTM Array

Programmable Electrically Erasable Logic Array

Features

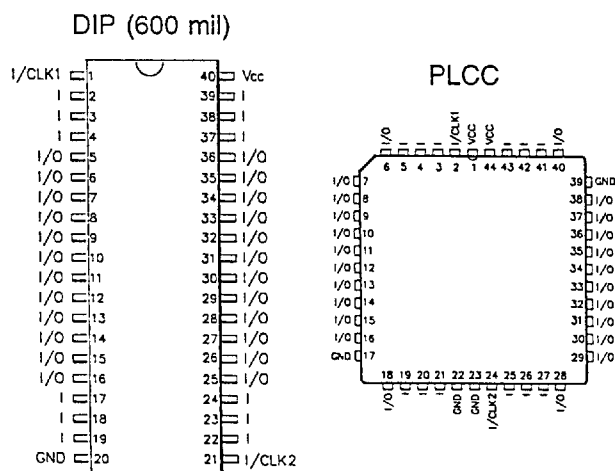
- **CMOS Electrically Erasable Technology**
 - Reprogrammable in 40-pin DIP and 44-pin PLCC packages
- **Versatile Logic Array Architecture**
 - 24 I/Os, 14 inputs, 60 registers/latches
 - Up to 72 logic cell output functions
 - PLA structure with true product-term sharing
 - Logic functions and registers can be I/O-buried
- **Flexible Logic Cell**
 - Up to 3 output functions per logic cell
 - D, T and JK registers with special features
 - Independent or global clocks, resets, presets, clock polarity, and output enables
 - Sum-of-products logic for output enables
- **High-Speed, Moderate Power Consumption**
 - As fast as 13ns/20ns (tpdi/tpd), 66.6MHz fmax
 - ICC 100mA max, 80mA typical
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
 - Integration of multiple PLDs and random logic
 - Buried counters, complex state-machines
 - Comparitors, decoders, multiplexers and other wide-gate functions
- **Development and Programmer Support**
 - ICT PLACE Development Software
 - Fitters for ABEL and CUPL design software
 - Programming support by ICT PDS-3 and other popular 3rd party programmers

General Description

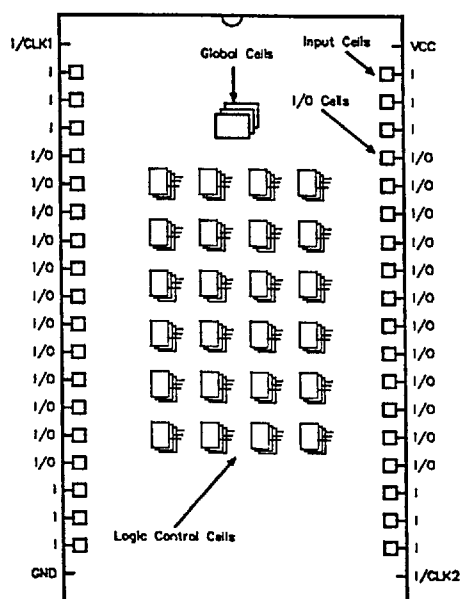
The PA7140 is a member of the Programmable Electrically Erasable Logic (PEEL) Array family based on ICT's 1-micron CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7140 offers a versatile logic array architecture with 24 I/O pins, 14 input pins and 60 registers/latches (24 buried logic cells, 12 input reg/latches, 24 buried I/O reg/latches). Its logic array implements 100 sum-of-product logic functions divided into two groups each serving 12 logic cells. Each group shares half (60) of the 120 product-terms available for logic cells.

The PA7140's logic and I/O cells (LCCs, IOCs) are extremely flexible with up to three output functions per cell (a total of 72 for all 24 logic cells). Cells are configurable as D, T and JK registers with independent or global clocks, resets, presets, clock polarity, and other features, making the PA7140 suitable for a variety of combinatorial, synchronous, and asynchronous logic applications. The PA7140 supports speeds as fast as 13ns/20ns (tpdi/tpdx) and 66.6MHz (fmax) at moderate power consumption 100mA (80mA typical). Packaging includes 40-pin DIP, and 44-pin PLCC. Development and programming support for the PA7140 is provided by ICT and popular third party development tool manufacturers.

Pin Configurations



Block Diagram



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to GND	– 0.5 to + 7.0	V
V _I , V _O	Voltage Applied to Any Pin	Relative to GND ¹	– 0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	± 25	mA
T _{ST}	Storage Temperature		– 65 to + 150	°C
T _{LT}	Lead Temperature	(Soldering 10 seconds)	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial ²	4.75	5.25	V
T _A	Ambient Temperature	Commercial ²	0	+ 70	°C
T _R	Clock Rise Time	(Note 3)		20	ns
T _F	Clock Fall Time	(Note 3)		20	ns
T _{RVCC}	V _{CC} Rise Time	(Note 3)		250	ms

D.C. Electrical Characteristics Over the operating range

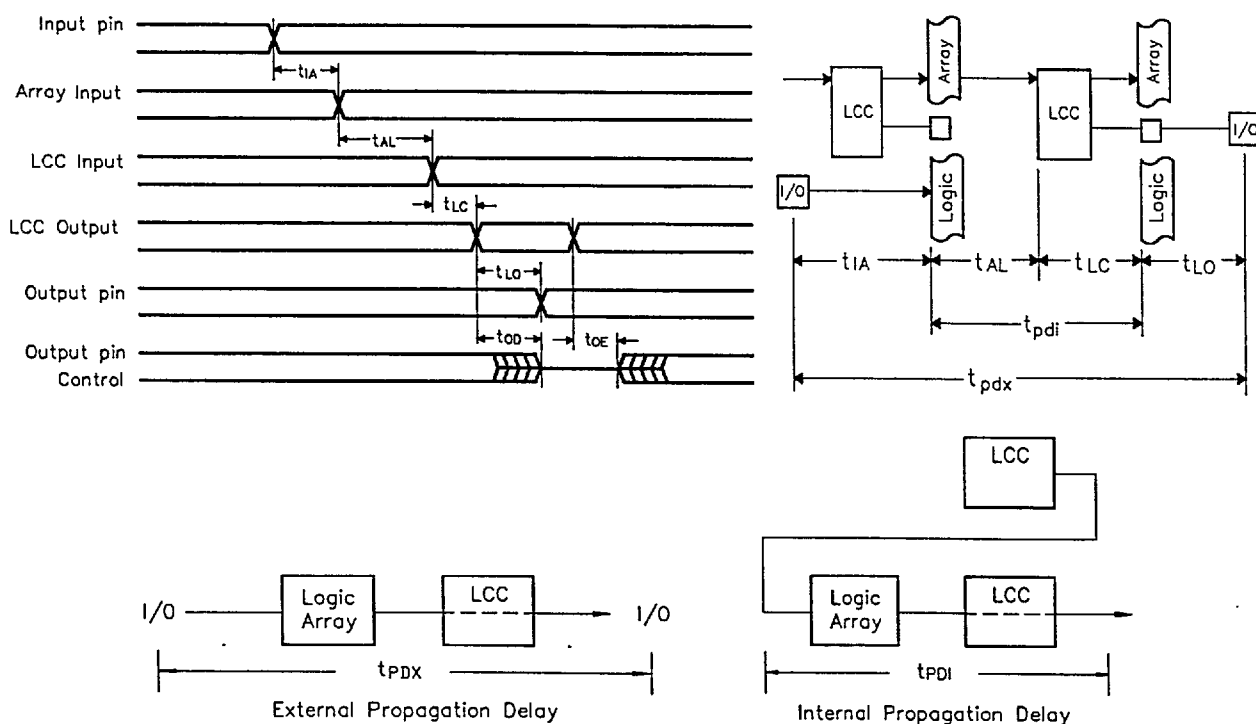
Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage - TTL	V _{CC} = Min, I _{OH} = – 4.0mA	2.4		V
V _{OHc}	Output HIGH Voltage-CMOS	V _{CC} = Min, I _{OH} = –10μA	V _{CC} – 0.1		V
V _{OL}	Output LOW Voltage - TTL	V _{CC} = Min, I _{OL} = 16mA		0.5	V
V _{OLc}	Output LOW Voltage-CMOS	V _{CC} = Min, I _{OL} = 10μA		0.1	V
V _{IH}	Input HIGH Level		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Level		– 0.3	0.8	V
I _{IL}	Input Leakage Current	V _{CC} = Max, GND ≤ V _{IN} ≤ V _{CC}		±10	μA
I _{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V _O ≤ V _{CC}		±10	μA
I _{SC}	Output Short Circuit Current ⁵	V _{CC} =5V, V _O =0.5V, T _A =25°C	– 30	– 120	mA
I _{CC}	V _{CC} Current	V _{IN} = 0V or V _{CC} ^{4,12} f = 25MHz All outputs disabled		100 (typ=80) ²⁰	mA
C _{IN}	Input Capacitance ⁶	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT}	Output Capacitance ⁶			12	pF

A.C. Electrical Characteristics Combinatorial

Over operating conditions

Symbol	Parameters ^{7, 13}	PA7140-20 PA7140-1 ¹⁸		PA7140-25 PA7140-2 ¹⁸		Units
		Min	Max	Min	Max	
t_{pDI}	Propagation delay Internal ($t_{AL} + t_{LC}$)		13		17	ns
t_{pDX}	Propagation delay External ($t_{IA} + t_{AL} + t_{LC} + t_{LO}$)		20		25	ns
t_{IA}	Input or I/O pin to array input		2		2	ns
t_{AL}	Array input to LCC		12		16	ns
t_{LC}	LCC input to LCC output ¹¹		1		1	ns
t_{LO}	LCC output to output pin		5		6	ns
t_{OD}, t_{OE}	Output Disable, Enable from LCC output ⁸		5		6	ns
t_{OX}	Output Disable, Enable from input pin ⁸		20		25	ns

Combinatorial Timing - Waveforms and Block Diagram



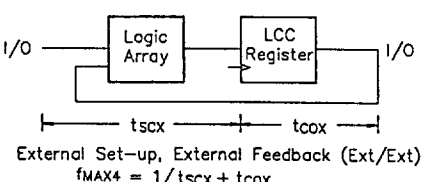
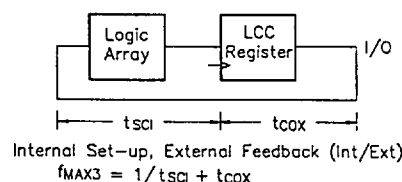
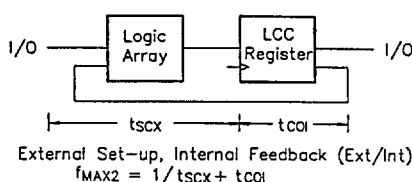
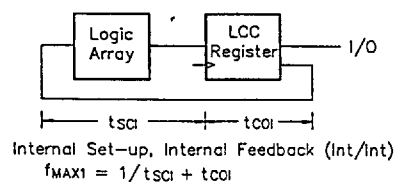
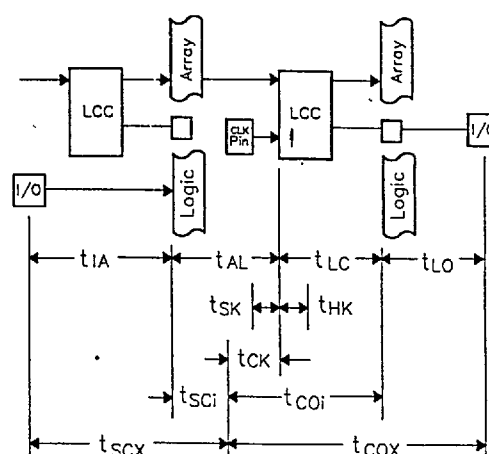
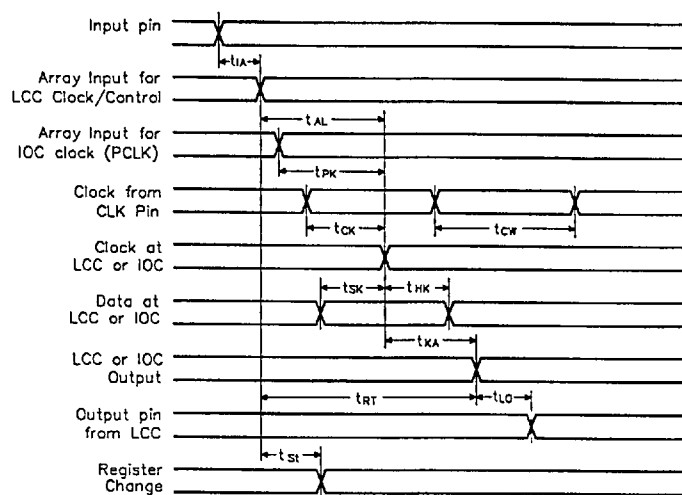


A.C. Electrical Characteristics Sequential

Over operating conditions

Symbol	Parameters ^{7, 13}	PA7140-20 PA7140-1 ¹⁸		PA7140-25 PA7140-2 ¹⁸		Units
		Min	Max	Min	Max	
tSCI	Internal set-up to system-clock ⁹ , - LCC ¹⁵ (tAL + tSK + tLC - tCK)	8		11		ns
tSCX	Input ¹⁷ (Ext.) set-up to system-clock, -LCC(tIA + tSCI)	10		14		ns
tCOI	System-clock to Array Int.-LCC/IOC/INC ¹⁵ (tCK + tLC)		7		8	ns
tCOX	System-clock to Output Ext.- LCC(tCOI + tLO)		12		14	ns
tHX	Input hold time from system clock - LCC	0		0		ns
tSK	LCC input set-up to async. clock ¹⁴ - LCC	1		1		ns
tAK	Clock at LCC or IOC - LCC output	1		1		ns
tHK	LCC input hold time from async. clock - LCC	4		4		ns
tSI	Input set-up to system clock -IOC/INC ¹⁵ (tSK - tCK)	0		0		ns
tHI	Input hold time from system clock-IOC/INC (tCK-tSK)	5		6		ns
tpK	Array input to IOC PCLK clock		9		11	ns
tSPI	Input set-up to PCLK clock -IOC/INC (tSK-tpK-tIA) ¹⁹	0		0		ns
tHPI	Input hold PCLK clock ¹⁸ - IOC/INC (tpK + tIA - tSK)	10		12		ns
tSD	Input set-up to system clock - IOC Sum-D ¹⁶ (tIA + tAL + tLC + tSK - tCK)	10		13		ns
tHD	Input hold time from system clock - IOC Sum-D	0		0		ns
tSDP	Input set-up to PCLK clock - IOC Sum-D (tIA + tAL + tLC + tSK - tpK)	7		9		ns
tHDP	Input hold time from PCLK clock - IOC Sum-D	0		0		ns
tCK	System-clock delay to LCC/IOC/INC		6		7	ns
tCW	System-clock low or high pulse width	7		8		ns
fMAX1	Max system-clock frequency Int/Int 1/(tSCI + tCOI)		66.6		52.6	MHz
fMAX2	Max system-clock frequency Ext/Int 1/(tSCX + tCOI)		58.8		45.4	MHz
fMAX3	Max system-clock frequency Int/Ext 1/(tSCI + tCOX)		50.0		40.0	MHz
fMAX4	Max system-clock frequency Ext/Ext 1/(tSCX + tCOX)		45.4		35.7	MHz
fTGL	Max system-clock toggle frequency 1/(tCW + tCW) ¹⁰		71.4		62.5	MHz
tPR	LCC Preset/Reset to LCC output		1		2	ns
tST	Input to Global Cell preset/reset (tIA + tAL + tPR)		15		20	ns
tAW	Asynch. preset/reset pulse width	8		8		ns
tRT	Input to LCC Reg-Type (RT)		8		10	ns
tRTV	LCC Reg-Type to LCC output register change		1		2	ns
tRTC	Input to Global Cell reg.-type change (tRT + tRTV)		9		12	ns
tRW	Asynch. Reg-Type pulse width	10		10		ns
treset	Power-on reset time for register in clear state ³		5		5	μs

Sequential Timing - Waveforms and Block Diagram



Notes:

- Minimum DC input is - 0.5V, however inputs may under-shoot to - 2.0V for periods less than 20ns.
- Contact ICT for other operating ranges.
- Test points for Clock and V_{CC} in t_R , t_F , t_{CL} , t_{CH} , and t_{RESET} are referenced at 10% and 90% levels.
- I/O pins are 0V or V_{CC} .
- Test one output at a time for a duration of less than 1 sec.
- Capacitances are tested on a sample basis.
- Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
- t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$ (See test loads at end of section 5 for V_{REF} value). t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
- DIP: "System-clock" refers to pin 1/21 high speed clocks. PLCC: "System-clock" refers to pin 2/24 high speed clocks.
- For T or JK registers in toggle (divide by 2) operation only.
- For combinatorial and async-clock to LCC output delay.
- ICC for a typical application: This parameter is tested with the device programmed as a 12-bit D type Counter.
- Test loads are specified at the end of section 3 in this data book.
- "Async. clock" refers to the clock from the Sum term (OR gate).
- The "LCC" term indicates that the timing parameter is applied to the LCC register.
- The "IOC" term indicates that the timing parameter is applied to the IOC register.
- The "INC" term indicates that the timing parameter is applied to the INC register.
- The "IOC/INC" term indicates that the timing parameter is applied to both the IOC and INC registers.
- The "LCC/IOC/INC" term indicates that the timing parameter is applied to the LCC, IOC and INC registers.
- This refers to the Sum-D gate routed to the IOC register for an additional buried register.
- The term "Input" without any reference to another term refers to an (external) input pin.
- PA7140-1 is an alternate number for PA7140-20. PA7140-2 is an alternate number for PA7140-25.
- The parameter t_{SPI} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of $(t_{SK} - t_{PK} - t_{IA})$. This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HPI} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
- Typical (typ) ICC is measured at $T_A = 25^\circ C$, Freq = 25MHz, $V_{CC} = 5V$.