PA83 • PA83A

POWER OPERATIONAL AMPLIFIERS

T-79-23

FEATURES

- LOW BIAS CURRENT, LOW NOISE - FET Input
- PROTECTED OUTPUT - Thermal Shutoff
- FULLY PROTECTED INPUT - Up to ±150V
- WIDE SUPPLY RANGE - ±15V to ±150V
- SECOND SOURCEABLE - BB3583AM/JM

APPLICATIONS

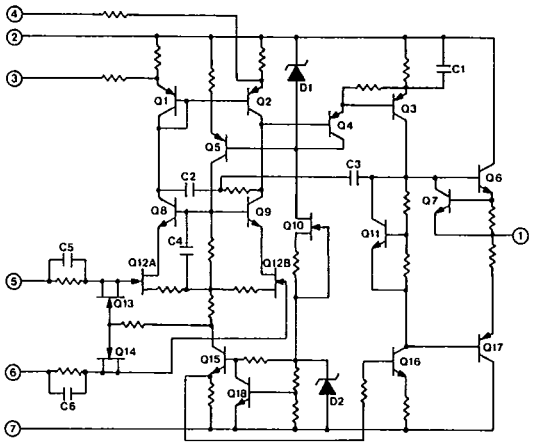
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 290V
- ANALOG SIMULATORS

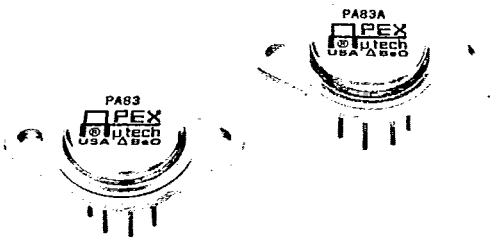
DESCRIPTION

The PA83 is a high voltage operational amplifier designed for output voltage swings up to ±145V with a dual (±) supply or 290V with a single supply. Its input stage is protected against transient and steady state overvoltages up to and including the supply rails. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA83 features an unprecedented supply range and excellent supply rejection. The output stage is biased in the class A/B mode for linear operation. Internal phase compensation assures stability at all gain settings without need for external components. Fixed current limits protect these amplifiers against shorts to common at supply voltages up to 120V. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A built-in thermal shutoff circuit prevents destructive overheating. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

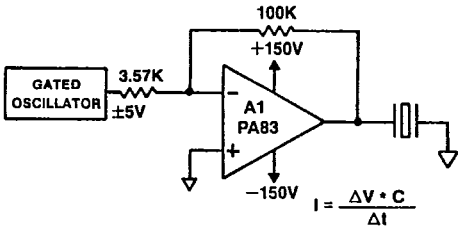
This hybrid circuit utilizes beryllia (BeO) substrates, thick (cermet) film resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8 pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible washers may void the warranty.

EQUIVALENT SCHEMATIC





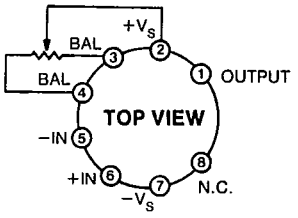
TYPICAL APPLICATION



SIMPLE PIEZO ELECTRIC TRANSDUCER DRIVE

While piezo electric transducers present a complex impedance, they are often primarily capacitive at useful frequencies. Due to this capacitance, the speed limitation for a given transducer/amplifier combination may well stem from limited current drive rather than power bandwidth restrictions. With its drive capability of 75mA, the PA83 can drive transducers having up to 2nF of capacitance at 40kHz at maximum output voltage. In the event the transducer may be subject to shock or vibration, flyback diodes, voltage clamps or other protection networks must be added to protect the amplifier from high voltages which may be generated.

EXTERNAL CONNECTIONS



NOTES: 1. Pin 8 not internally connected.
2. Input offset trimpot optional. Recommended value 100KΩ.

PA83 ABSOLUTE MAXIMUM RATINGS

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SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	Internally Limited
POWER DISSIPATION, internal at $T_C = 25°C$[1]	17.5W
INPUT VOLTAGE, differential	±300V
INPUT VOLTAGE, common-mode	±300V
TEMPERATURE, pin solder-10s max (solder)	300°C
TEMPERATURE, junction	150°C
TEMPERATURE RANGE, storage	−65 to +150°C
OPERATING TEMPERATURE RANGE, case	−55 to +125°C

SPECIFICATIONS

		PA83/PA83J			PA83A			
PARAMETER	**TEST CONDITIONS**[2]	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	$T_C = 25°C$		±1.5	±3		±.5	±1	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±25		±5	±10	µV/°C
OFFSET VOLTAGE, vs. supply	$T_C = 25°C$		±.5			±.2		µV/V
OFFSET VOLTAGE, vs. time	$T_C = 25°C$		±75			*		$\mu V/\sqrt{kh}$
BIAS CURRENT, initial[3]	$T_C = 25°C$		5	50		3	10	pA
BIAS CURRENT, vs. supply	$T_C = 25°C$		.01			*		pA/V
OFFSET CURRENT, initial[3]	$T_C = 25°C$		±2.5	±50		±1.5	±10	pA
OFFSET CURRENT, vs. supply	$T_C = 25°C$		±.01			*		pA/V
INPUT IMPEDANCE, dc	$T_C = 25°C$		10^{11}			*		Ω
INPUT CAPACITANCE	Full temperature range		6			*		pF
COMMON-MODE VOLTAGE RANGE[4]	Full temperature range	$\pm V_S - 10$			*			V
COMMON-MODE REJECTION, dc	Full temperature range		130			*		db
GAIN								
OPEN LOOP GAIN at 10Hz	$T_C = 25°C$, $R_L = 2K\Omega$	96	116		*	*		db
UNITY GAIN CROSSOVER FREQ.	$T_C = 25°C$, $R_L = 2K\Omega$		5		3	*		MHz
POWER BANDWIDTH	$T_C = 25°C$, $R_L = 10K\Omega$		60		40	*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[4], full load	Full temp. range, $I_O = 75mA$	$\pm V_S - 10$	$\pm V_S - 5$		*	*		V
VOLTAGE SWING[4]	Full temp. range, $I_O = 15mA$	$\pm V_S - 5$	$\pm V_S - 3$		*	*		V
CURRENT, peak	$T_C = 25°C$	75			*			mA
CURRENT, short circuit	$T_C = 25°C$		100			*		mA
SLEW RATE[5]	$T_C = 25°C$, $R_L = 2K\Omega$	20	30		*	*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			10			*	nF
CAPACITIVE LOAD, gain>4	Full temperature range			SOA			*	µF
SETTLING TIME to 0.1%	$T_C = 25°C$, $R_L = 2K\Omega$, 10V step		12			*		µs
POWER SUPPLY								
VOLTAGE	$T_C = -55$ to $+125°C$	±15	±150	±150	*	*	*	V
CURRENT, quiescent	$T_C = 25°C$		6	8.5		*	*	mA
THERMAL								
RESISTANCE, ac[5] junction to case	F>60Hz		3.8			*		°C/W
RESISTANCE, dc junction to case	F<60Hz		6	6.5		*	*	°C/W
RESISTANCE, case to air			30			*		°C/W
TEMP. RANGE, case (PA83/PA83A)	Meets full range specification	−25		+85	*		*	°C
TEMP. RANGE, case (PA83J)	Meets full range specification	0		70				°C

NOTES: * The specification of PA83A is identical to the specification for PA83 in applicable column to the left.

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is the TYP rating unless otherwise specified as a test condition.
3. Doubles for every 10°C of temperature increase
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.

CAUTION: The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

PA83 TYPICAL PERFORMANCE GRAPHS

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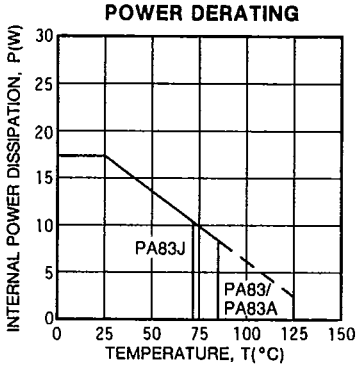
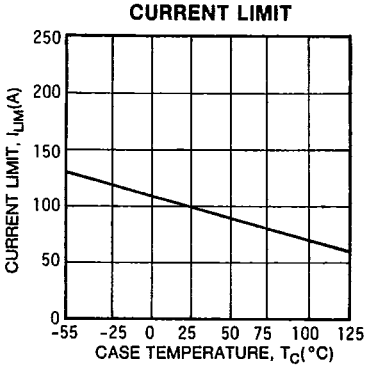
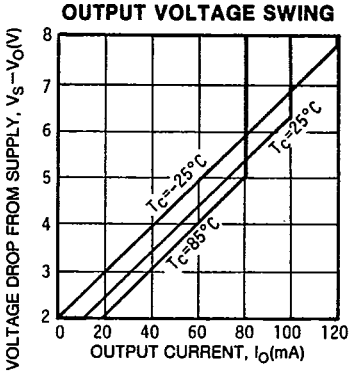
POWER DERATING



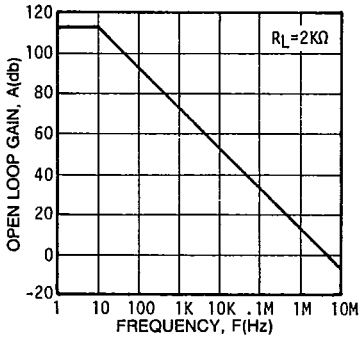
CURRENT LIMIT



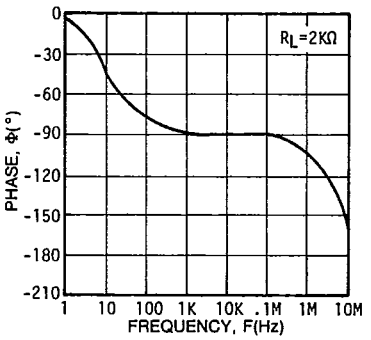
OUTPUT VOLTAGE SWING



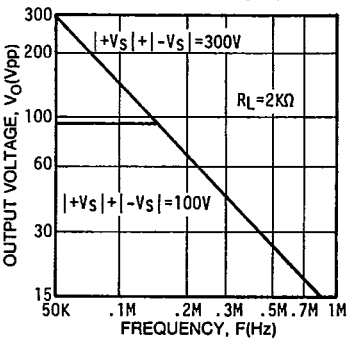
SMALL SIGNAL RESPONSE



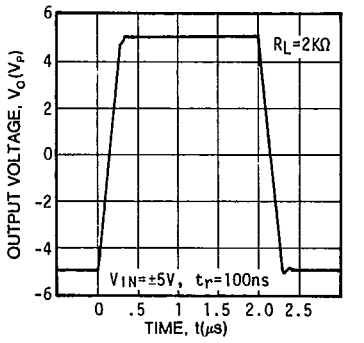
PHASE RESPONSE



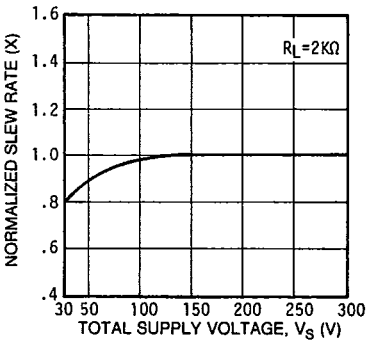
POWER RESPONSE



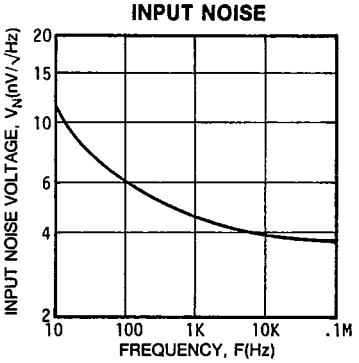
PULSE RESPONSE



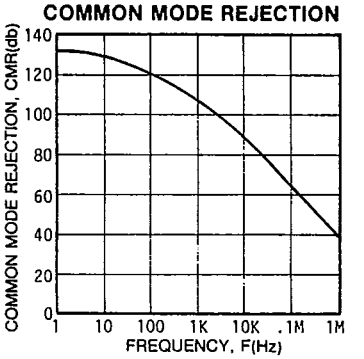
SLEW RATE VS. SUPPLY



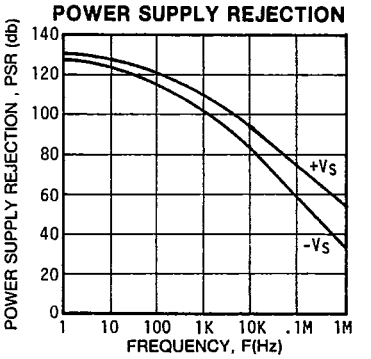
INPUT NOISE



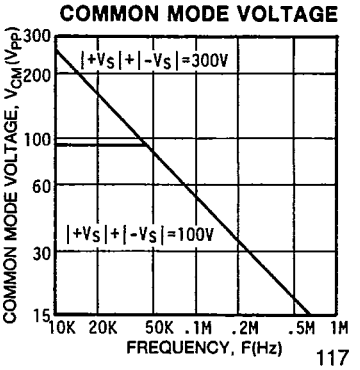
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



PA83 OPERATING CONSIDERATIONS

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GENERAL

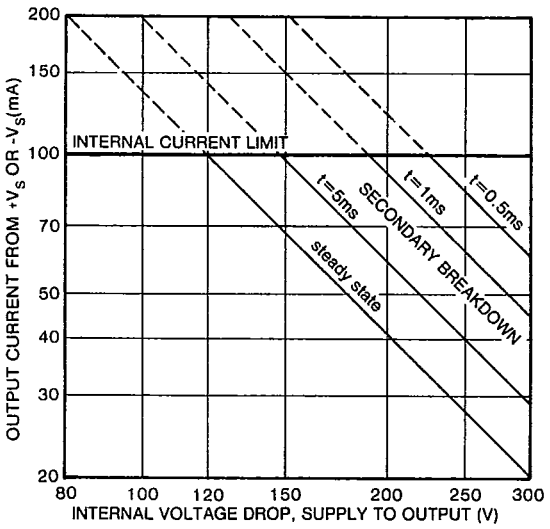
Please read the "General Operating Considerations"section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the applications notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The bipolar output stage of this high voltage amplifier has two distinct limitations:

1. The internal current limit, which limits maximum available output current.
2. The secondary breakdown effect, which occurs whenever the simultaneous collector current and callector-emitter voltage exceed specified limits.

SAFE OPERATING AREA CURVES



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. The following capacitive and inductive loads are safe:

±Vs	C(MAX)	L(MAX)
150V	.7μF	1.5H
125V	2.0μF	2.5H
100V	5.0μF	6.0H
75V	60μF	30H
50V	ALL	ALL

2. Short circuits to ground are safe with dual supplies up to ±120V or single supplies up to 120V.
3. Short circuits to the supply rails are safe with total supply voltages up to 120V. (ie ±60V).
4. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the sustrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive jucntion temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the $T_C = 25°C$ boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

INDUCTIVE LOADS

Two external diodes as shown in figure 1, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

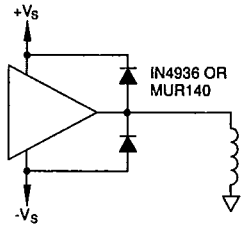


FIGURE 1. PROTECTION, INDUCTIVE LOAD.

APEX μTECH

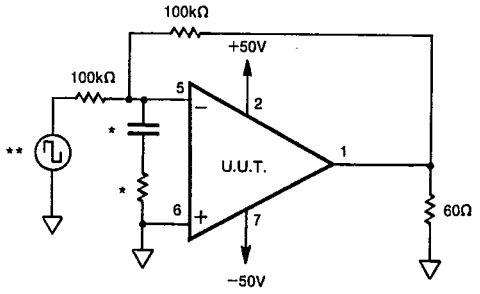
T-79-23

PA83M

TABLE 4 — GROUP A INSPECTION

SG	PARAMETER	SYMBOL	TEMP	PWR	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±150V	V_{IN} = 0, G = 100		8.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±150V	V_{IN} = 0, G = 100		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	V_{IN} = 0, G = 100		5.7	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±150V	V_{IN} = 0, G = 100		50	pA
1	Input Bias Current, −IN	$-I_B$	25°C	±150V	V_{IN} = 0, G = 100		50	pA
1	Input Offset Current	I_{OS}	25°C	±150V	V_{IN} = 0, G = 100		50	pA
3	Quiescent Current	I_Q	−55°C	±150V	V_{IN} = 0, G = 100		10	mA
3	Input Offset Voltage	V_{OS}	−55°C	±150V	V_{IN} = 0, G = 100		5	mV
3	Input Offset Voltage	V_{OS}	−55°C	±15V	V_{IN} = 0, G = 100		7.7	mV
3	Input Bias Current, +IN	$+I_B$	−55°C	±150V	V_{IN} = 0, G = 100		50	pA
3	Input Bias Current, −IN	$-I_B$	−55°C	±150V	V_{IN} = 0, G = 100		50	pA
3	Input Offset Current	I_{OS}	−55°C	±150V	V_{IN} = 0, G = 100		50	pA
2	Quiescent Current	I_Q	125°C	±150V	V_{IN} = 0, G = 100		10	mA
2	Input Offset Voltage	V_{OS}	125°C	±150V	V_{IN} = 0, G = 100		5.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±15V	V_{IN} = 0, G = 100		8.2	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±150V	V_{IN} = 0, G = 100		10	nA
2	Input Bias Current, −IN	$-I_B$	125°C	±150V	V_{IN} = 0, G = 100		10	nA
2	Input Offset Current	I_{OS}	125°C	±150V	V_{IN} = 0, G = 100		10	nA
4	Output Voltage, I_O = 75mA	V_O	25°C	±85V	R_L = 1K	75		V
4	Output Voltage, I_O = 29mA	V_O	25°C	±150V	R_L = 5K	145		V
4	Current Limits	I_{CL}	25°C	±30V	R_L = 100Ω	75	125	mA
4	Stability/Noise	E_N	25°C	±150V	R_L = 5K, G = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±150V	R_L = 5K	20	60	V/μs
4	Open Loop Gain	A_{OL}	25°C	±150V	R_L = 5K, f = 10Hz	96		db
4	Common-mode Rejection	CMR	25°C	±32.5V	R_L = 5K, f = DC, V_{CM} = ±22.5V	90		db
6	Output Voltage, I_O = 40mA	V_O	−55°C	±45V	R_L = 1K	40		V
6	Output Voltage, I_O = 29mA	V_O	−55°C	±150V	R_L = 5K	145		V
6	Stability/Noise	E_N	−55°C	±150V	R_L = 5K, G = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	−55°C	±150V	R_L = 5K	20	60	V/μs
6	Open Loop Gain	A_{OL}	−55°C	±150V	R_L = 5K, f = 10Hz	96		db
6	Common-mode Rejection	CMR	−55°C	±32.5V	R_L = 5K, f = DC, V_{CM} = ±22.5V	90		db
5	Output Voltage, I_O = 40mA	V_O	125°C	±45V	R_L = 1K	40		V
5	Output Voltage, I_O = 29mA	V_O	125°C	±150V	R_L = 5K	145		V
5	Stability/Noise	E_N	125°C	±150V	R_L = 5K, G = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±150V	R_L = 5K	20	60	V/μs
5	Open Loop Gain	A_{OL}	125°C	±150V	R_L = 5K, f = 10Hz	96		db
5	Common-mode Rejection	CMR	125°C	±32.5V	R_L = 5K, f = DC, V_{CM} = ±22.5V	90		db

BURN IN CIRCUIT:



*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

**Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA83Q

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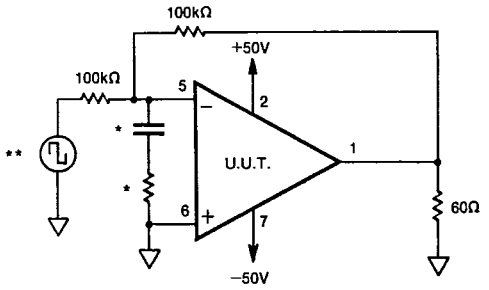
100% TEST TABLE

SG	PARAMETER	SYMBOL	TEMP	PWR	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±150V	V_{IN} = 0, G = 100		8.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±150V	V_{IN} = 0, G = 100		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	V_{IN} = 0, G = 100		5.7	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±150V	V_{IN} = 0, G = 100		50	pA
1	Input Bias Current, −IN	$-I_B$	25°C	±150V	V_{IN} = 0, G = 100		50	pA
1	Input Offset Current	I_{OS}	25°C	±150V	V_{IN} = 0, G = 100		50	pA
3	Quiescent Current	I_Q	−25°C	±150V	V_{IN} = 0, G = 100		10	mA
3	Input Offset Voltage	V_{OS}	−25°C	±150V	V_{IN} = 0, G = 100		4.2	mV
3	Input Offset Voltage	V_{OS}	−25°C	±15V	V_{IN} = 0, G = 100		6.9	mV
3	Input Bias Current, +IN	$+I_B$	−25°C	±150V	V_{IN} = 0, G = 100		50	pA
3	Input Bias Current, −IN	$-I_B$	−25°C	±150V	V_{IN} = 0, G = 100		50	pA
3	Input Offset Current	I_{OS}	−25°C	±150V	V_{IN} = 0, G = 100		50	pA
2	Quiescent Current	I_Q	85°C	±150V	V_{IN} = 0, G = 100		10	mA
2	Input Offset Voltage	V_{OS}	85°C	±150V	V_{IN} = 0, G = 100		4.5	mV
2	Input Offset Voltage	V_{OS}	85°C	±15V	V_{IN} = 0, G = 100		7.2	mV
2	Input Bias Current, +IN	$+I_B$	85°C	±150V	V_{IN} = 0, G = 100		3.2	nA
2	Input Bias Current, −IN	$-I_B$	85°C	±150V	V_{IN} = 0, G = 100		3.2	nA
2	Input Offset Current	I_{OS}	85°C	±150V	V_{IN} = 0, G = 100		3.2	nA
4	Output Voltage, I_O = 75mA	V_O	25°C	±85V	R_L = 1K	75		V
4	Output Voltage, I_O = 75mA	V_O	25°C	±85V	R_L = 5K	145		V
4	Current Limits	I_{CL}	25°C	±30V	R_L = 100Ω	75	125	mA
4	Stability/Noise	E_N	25°C	±150V	R_L = 5K, G = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±150V	R_L = 5K	20	60	V/μs
4	Open Loop Gain	A_{OL}	25°C	±150V	R_L = 5K, f = 10Hz	96		db
4	Common-mode Rejection	CMR	25°C	±32V	R_L = 5K, f = DC, V_{CM} = ±22.5V	90		db
6	Output Voltage, I_O = 55mA	V_O	−25°C	±65V	R_L = 1K	3		V
6	Output Voltage, I_O = 29mA	V_O	−25°C	±150V	R_L = 5K	145		V
6	Stability/Noise	E_N	−25°C	±150V	R_L = 5K, G = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	−25°C	±150V	R_L = 5K	20	60	V/μs
6	Open Loop Gain	A_{OL}	−25°C	±150V	R_L = 5K, f = 10Hz	96		db
6	Common-mode Rejection	CMR	−25°C	±32V	R_L = 5K, f = DC, V_{CM} = ±22.5V	90		db
5	Output Voltage, I_O = 55mA	V_O	85°C	±65V	R_L = 1K	55		V
5	Output Voltage, I_O = 29mA	V_O	85°C	±150V	R_L = 5K	145		V
5	Stability/Noise	E_N	85°C	±150V	R_L = 5K, G = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	85°C	±150V	R_L = 5K	20	60	V/μs
5	Open Loop Gain	A_{OL}	85°C	±150V	R_L = 5K, f = 10Hz	96		db
5	Common-mode Rejection	CMR	85°C	±32V	R_L = 5K, f = DC, V_{CM} = ±22.5V	90		db

BURN IN CIRCUIT:



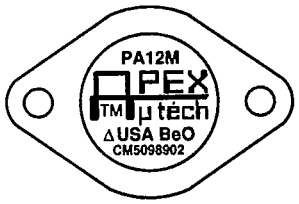
*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

**Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

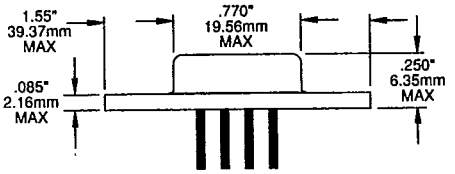
PACKAGE OUTLINE DIMENSIONS

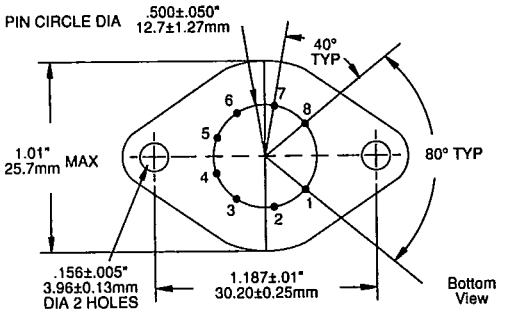
T-90-20

STANDARD 8 PIN TO-3



NOTE: ESD triangle (Δ) on top of package denotes pin 1 location.

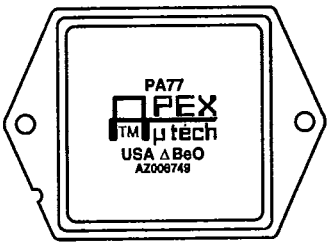




PIN DIAMETER:	.967/1.07mm or .038/.042"
PIN LENGTH:	11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated alloy 52, solderable
PIN MATERIAL, MIL:	Gold plated alloy 52, solderable
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	15 grams or .53 ounces
ISOLATION:	500VDC any pin to case
SOCKETS:	APEX PN: MS03
CAGE JACKS:	APEX PN: MS02 (Set of 8)
HEATSINKS:	APEX PN: HS01 thru HS05

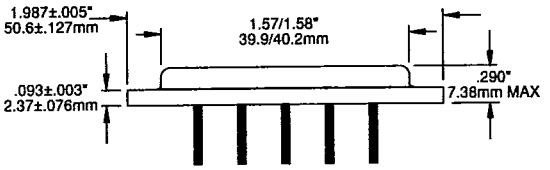
CAUTION
Recommended mounting torque is 4 – 7 in•lbs (.45 – .79 N•m)

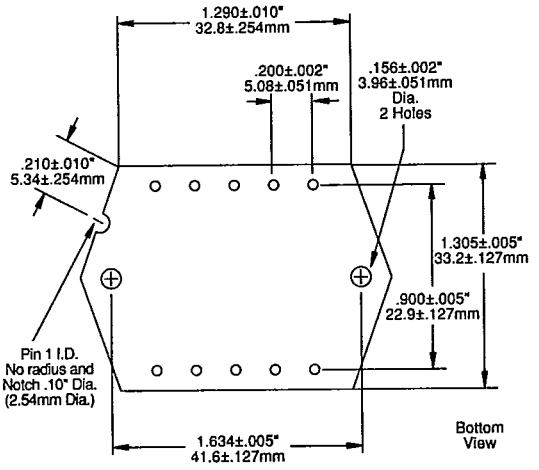
POWER PD10



NOTE: Notch on package base denotes pin 1 location.

PD10/60S





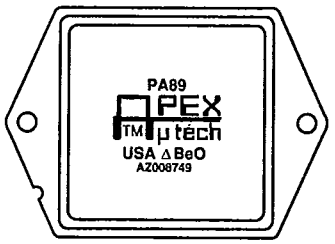
PIN DIAMETER:	1.47/1.58mm or .058/.062"
PIN LENGTH:	11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	36 grams or 1.27 ounces
ISOLATION:	500VDC any pin to case
CAGE JACKS:	MS04 (Set of 12)

CAUTION
Recommended mounting torque is 8 – 10 in•lbs (.90 – 1.13 N•m)

PACKAGE OUTLINE DIMENSIONS

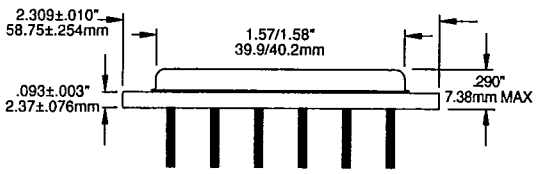
T-90-20

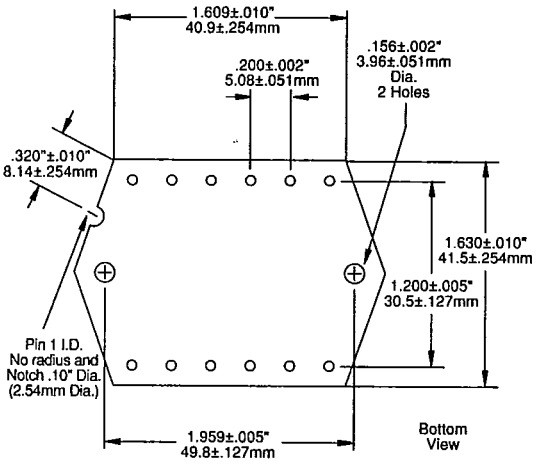
HIGH VOLTAGE PD12



NOTE: Notch on package base denotes pin 1 location.

PD12/25S

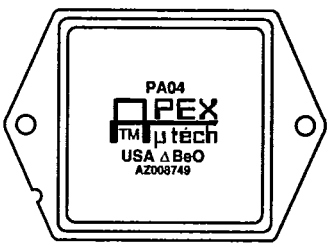




PIN DIAMETER:	.585/.687mm or .023/.027"
PIN LENGTH:	11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	53 grams or 1.87 ounces
ISOLATION:	1200VDC any pin to case

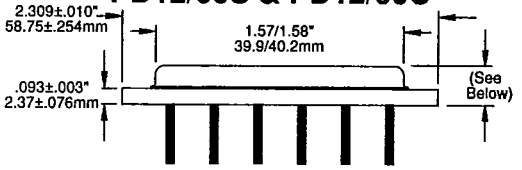
CAUTION
Recommended mounting torque is 8 – 10 in•lbs (.90 – 1.13 N•m)

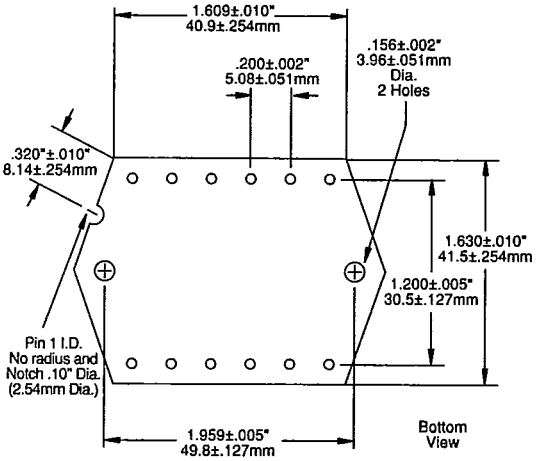
HIGH POWER PD12



NOTE: Notch on package base denotes pin 1 location.

PD12/60S & PD12/60C





PIN DIAMETER:		1.47/1.58mm or .058/.062"
PIN LENGTH:		11.4/12.7mm or .450/.500"
PIN MATERIAL, STD:		Nickel plated steel
ISOLATION:	PD12/60S:	500VDC any pin to case
	PD12/60C:	300VDC any pin to case
HEIGHT:	PD12/60S:	7.38mm or .290" MAX
	PD12/60C:	8.90mm or .350" MAX
PACKAGE:	PD12/60S:	Hermetic, nickel plated steel
	PD12/60C:	Base: Nickel plated copper
	PD12/60C:	Cap: Hermetic, nickel plated steel
WEIGHT:	PD12/60S:	53 grams or 1.87 ounces
	PD12/60C:	58 grams or 2.05 ounces
CAGE JACKS:	Apex PN:	MS04 (Set of 12)
HEAT SINKS:	Apex PN:	HS06
MATING SOCKET:	Apex PN:	MS05

CAUTION Recommended mounting torque is 8–10 in•lbs (.90–1.13 N•m)