LCD Super VGA Controller Chip

1.0 Introduction

The OPTi 92C178, a fully integrated follow-on to the OPTi 92C168, provides an unmatched price/performance LCD VGA solution for portable IBM® compatible personal computers. The 92C178 offers high performance, full integration, low power consumption, complete panel support, and simultaneous LCD/CRT display as part of a highly integrated graphics subsystem.

High performance is made possible by a built-in fixed function graphics accelerator. The accelerator supports BitBlt, polygon fill, line draw, color expansion, and clipping. Acceleration is supported for pixel depths of 8, 15, 16, and 24 bits/pixel. Hardware cursor support and linear addressing support further enhance performance in GUI environments by removing software cursor overhead and eliminating bank switching.

The RAMDAC and clock synthesizer are built into the 92C178. No external logic is required to connect to the 16-bit ISA, 16/32-bit Local bus, or PCI bus. Panels may be driven directly without external drive buffers or separate frame buffer memory (dual scan panels). A complete LCD VGA video subsystem can be implemented with two 256Kx16 DRAM chips.

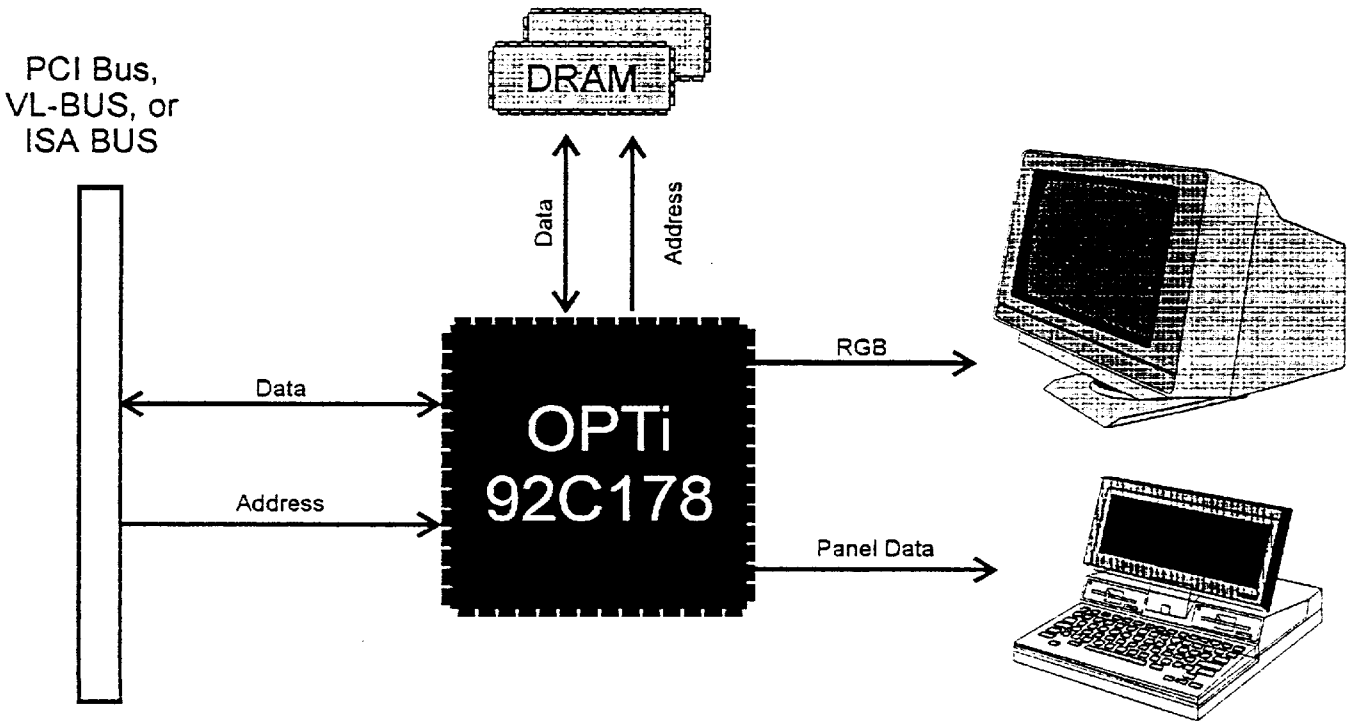
The 92C178 is optimized for minimum power consumption during normal operation and provides three power saving modes. 3.3V/5V mixed voltage operation helps to further reduce video subsystem power consumption.

The 92C178 supports a wide variety of dual scan color/mono STN, single scan color/mono STN and TFT panels. Panel resolutions of 640x480, 800x600 and 1024x768 are supported. The 92C178 supports up to 16.8 million colors on color panels and up to 256 gray scales on monochrome panels.

The 92C178 supports CRT display resolutions up to 1280x1024-256 colors. LCD display is provided at resolutions up to 1024x768 non-interlaced.

The OPTi 92C178 is 100% register level compatible with the IBM VGA standard. OPTi supplies a fully compatible VGA/VESA BIOS, drivers for common applications and operating systems, such as AutoCAD and Windows, and OEM and end-user level utility software.

Figure 1-1 OPTi 92C178 System Block Diagram



2.0 Features

2.1 Features	2.2 Benefits
Integrated true color RAMDAC and clock.	Full integration. One chip solution.
Built-in graphics accelerator. Supports BitBlt, polygon fill, line draw, color expansion and clipping.	Superior performance.
32-bit direct interface with VESA local bus and PCI bus, and 16-bit direct interface with ISA bus.	No external glue logic. Reduced footprint design. Cost savings.
Direct interface to dual scan color/mono STN, single scan color/mono STN, and TFT panels.	No drive buffer or additional video frame buffer requirement. Reduced footprint design.
Support for 800x600 panels: • STN type • TFT type • Expansion of standard VGA modes to 800x600	Provides complete support for new generation laptops which use 800x600 panels.
Advanced power management to minimize power consumption: • Remove backlight power. • Hardware/Software activated Standby Mode. • Hardware/Software activated Suspend Mode. • Deep Sleep Mode. • DPMS	Extends battery life. Flexible power-down options.
3.3V/5V mixed voltage operation.	Optimizes power consumption.
Flexible DRAM configurations: One/two/four 256Kx16 DRAMs, Four/eight/sixteen 256Kx4 DRAMs.	Design flexibility for 1MB or 2MB implementations. Facilitates cost-effective graphics frame buffer solutions.
Support simultaneous display for dual scan STN panel with one 256Kx16 DRAM.	Reduced footprint design. Cost savings for base system.
Hardware cursor (32x32x2 and 64x64x2 cursor sizes supported).	No distracting cursor flicker. Improved performance.
Hardware pop-up icon (64x64x2 and 128x128x2 icon sizes supported).	Use icon as a second hardware cursor to display system status.
Supports up to 16.8 million colors on both CRT and color LCD displays.	Superior color display quality on both LCDs and CRTs.
Supports up to 256 gray shades for mono LCD displays.	Superior monochrome display quality on LCD panels.
Supports the following LCD display adjustment features: • Text mode contrast enhancement. • Reverse video for graphics and text modes. • Vertical expansion and auto-centering.	Provides display flexibility to meet individual requirements.
Screen Saver Option • Blanks screen • HW cursor and pop-up icon remain on the display	Easy to implement. Operating system independent.
Programmable linear addressing.	Eliminates bank switching.
100% hardware/BIOS compatible with IBM VGA standard.	Allows use of any VGA compatible software with the video subsystem.
Multimedia Features • VAFC compatible feature connector • Overlay • Genlock	Multimedia ready.

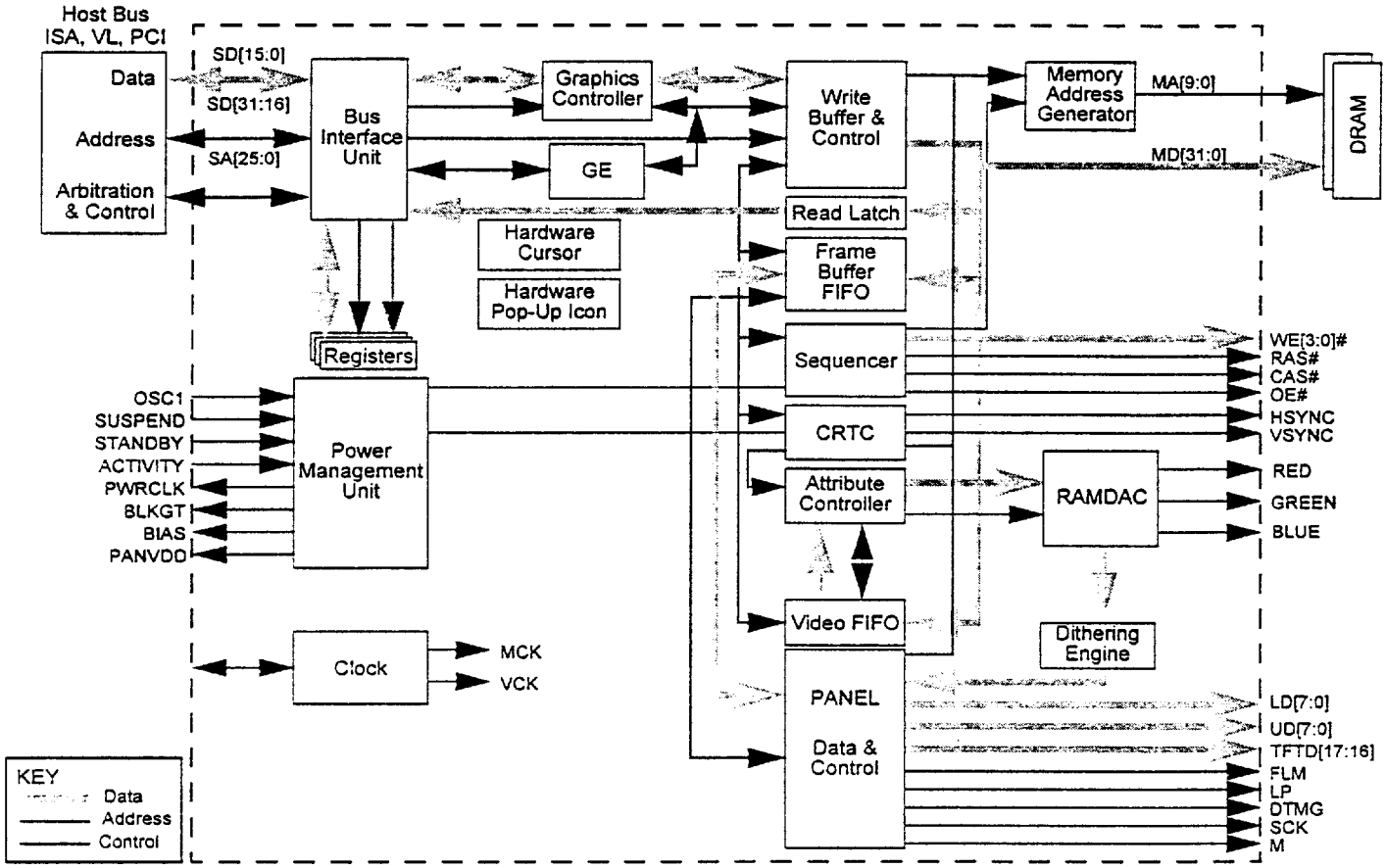
2.3 Architecture

The OPTi 92C178 contains the following major functional modules:

- Bus Interface Unit
- Write Buffer Control Unit
- Graphic Controller
- Memory Sequencer
- Video FIFO
- CRT Controller
- Attribute Controller
- GUI Engine
- Hardware Cursor
- Pop-up Icon
- Frame Buffer Controller
- RAMDAC
- Dithering Engine
- Flat Panel Interface Controller
- Power Management Unit
- Power Distribution Module
- Clock Synthesizer
- Multi-media Module

The function of each module is described in Section 4.0, *Bus Interface Unit*.

Figure 2-1 OPTi 92C178 Functional Block Diagram



2.4 Example Controller Block Diagrams

Figure 2-2 1MB ISA-Bus Solution using Dual Scan Monochrome Panel

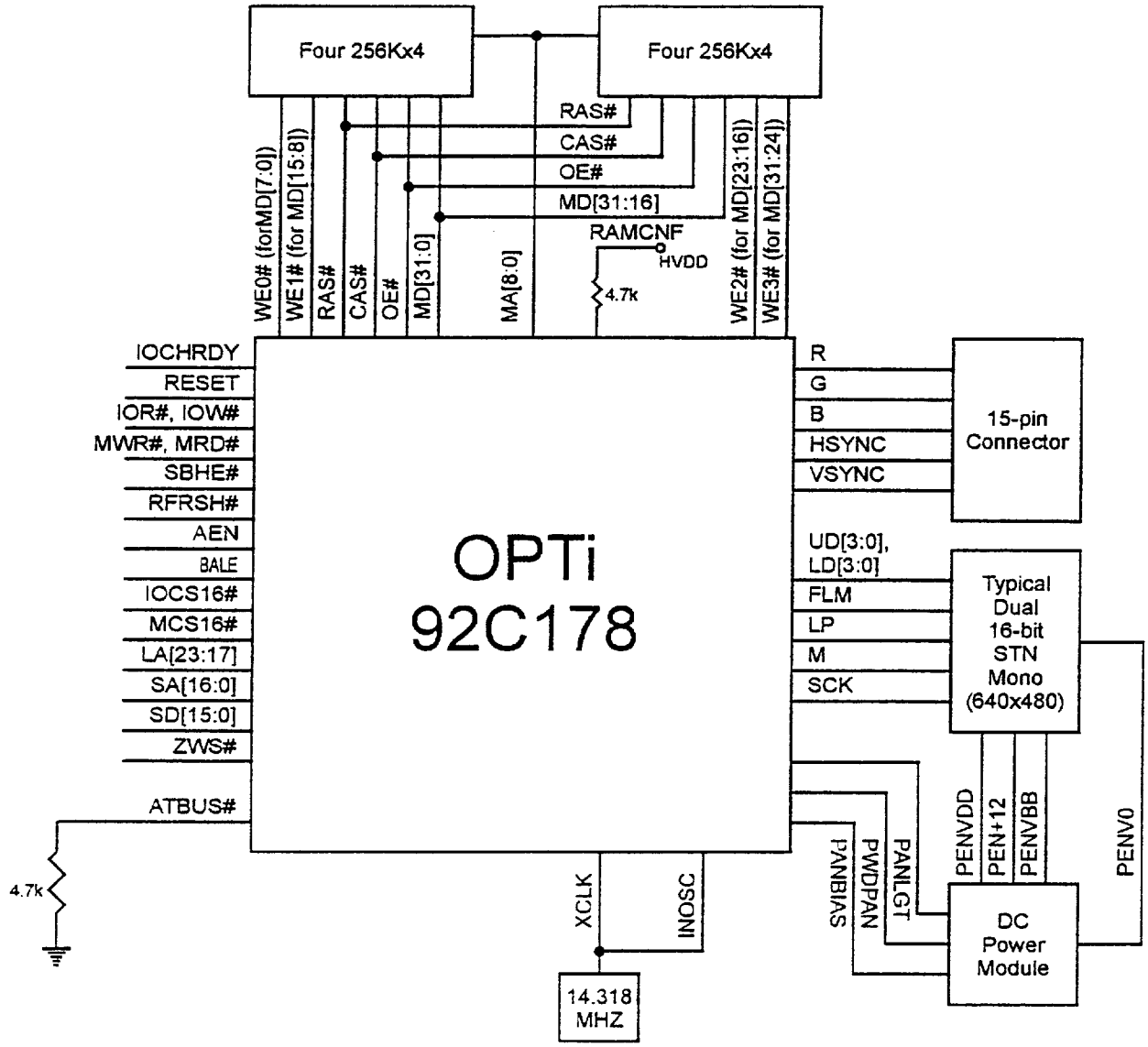


Figure 2-3 1MB 486DX VL-Bus Solution using 9-bit TFT Color Panel

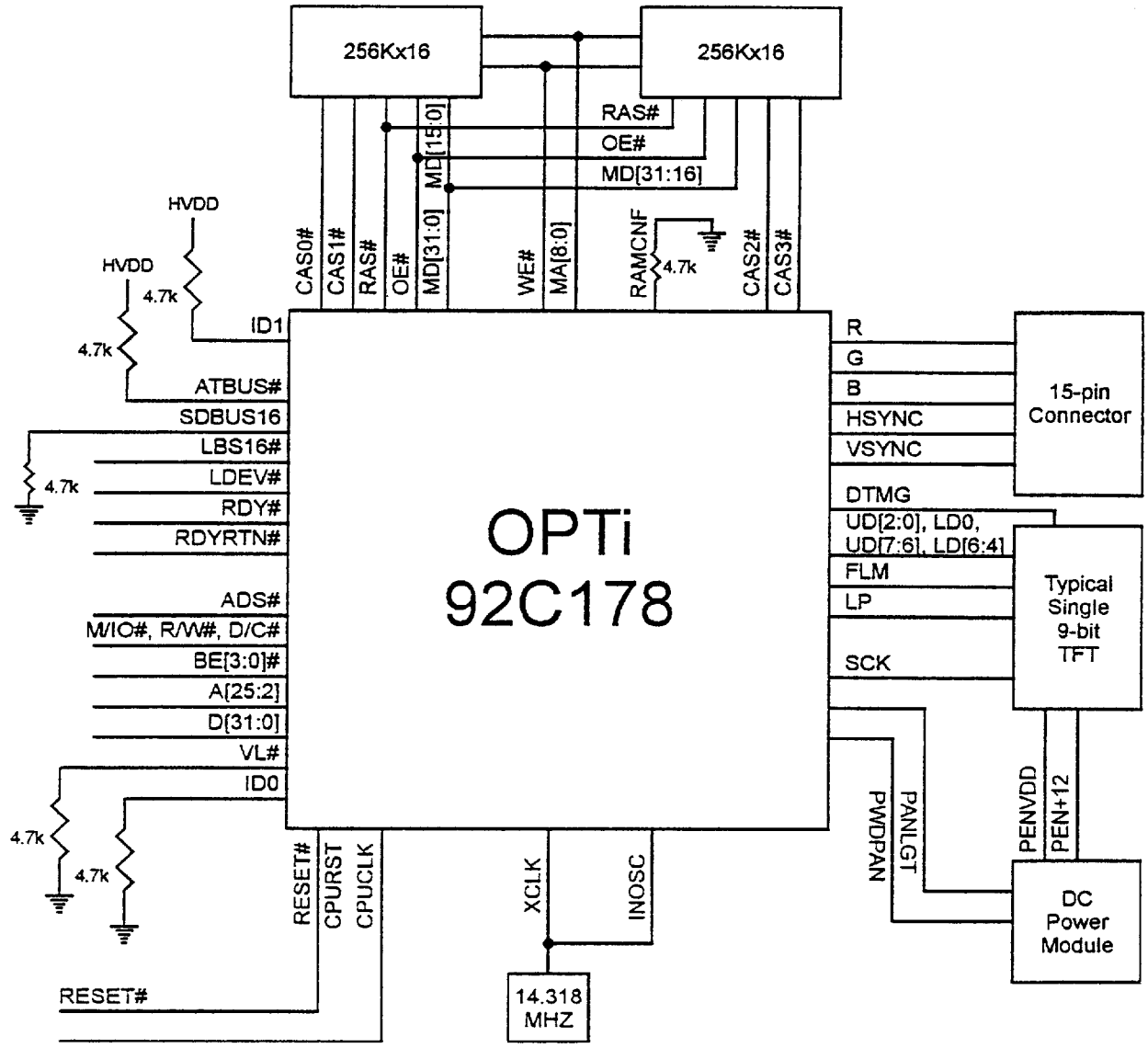
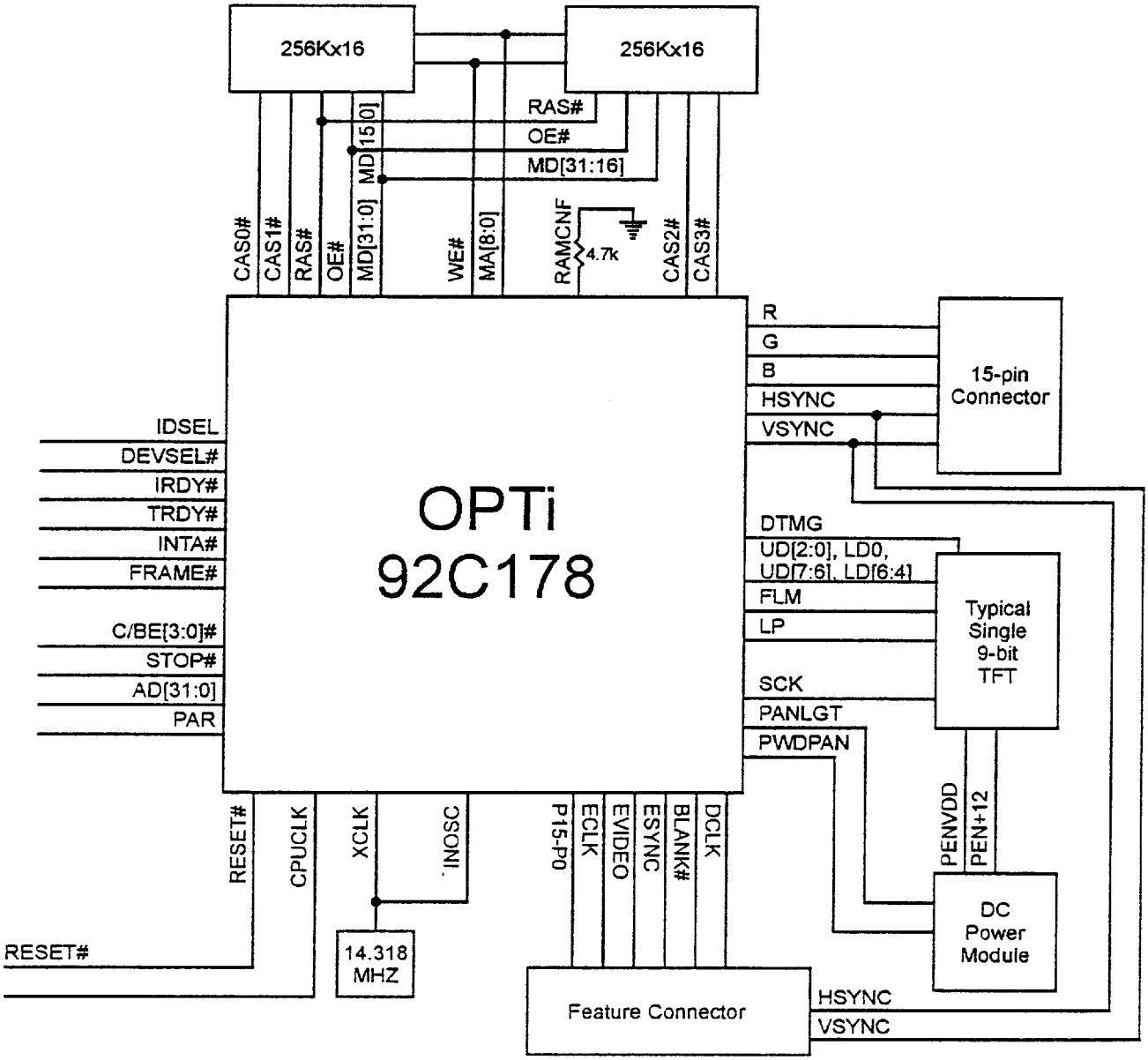


Figure 2-4 1MB 486DX PCI -Bus Solution using 9-bit TFT Color Panel
(with 16-bit Feature Connector)



2.4.1 Definitions of MD31-MD0 at System Reset

Table 2-1 lists the definitions of MD31-MD0 at system reset. To set the given MD bit to a logical 1, pull high through a 4.7Kohm resistor. To set the given bit to a logical 0, pull low through a 4.7KΩ resistor.

NOTE MD31-MD16 do not directly set any register bits in the chip. The OPTi BIOS resets MD31-MD16 and then sets the 92C178 register bits appropriately.

Table 2-1 MD31-MD0 Definitions at Reset

MD[a]	Logical Level		Definition	
MD31	1		Enables Feature Connector. For feature connector enabled, MD definitions for MD15-MD8 hold.	
	0		Disables Feature Connector. For feature connector disabled, MD15-MD8 are not used since configuration pins backward compatible to the 92C168 are available. See Note 1.	
MD30	1		Enable PCI BIOS interface.	
	0		Disable PCI BIOS interface.	
MD29-26	–		Reserved	
MD25	1		Indicates 3.3V CVDD	
	0		Indicates 5V CVDD	
MD24	1		Indicates 3.3V panel interface	
	0		Indicates 5V panel interface	
MD23	1		Indicates 3.3V memory interface	
	0		Indicates 5V memory interface	
MD22	1		Selects single scan panel	
	0		Selects dual scan panel	
MD21 - MD20	Selects panel data interface width			
	MD21	**MD20**	**STN**	**TFT**
	0	0	mono 4-bit (single), mono 8-bit (dual)	9-bit
	0	1	mono 8-bit (single)	12-bit
	1	0	color 8-bit	3-bit
	1	1	color 16-bit	18-bit
MD19	1		Selects TFT panel	
	0		Selects STN panel	
MD18	1		Selects high resolution panel (800x600 or 1024x768)	
	0		Selects 640x480 panel	

Table 2-1 MD31-MD0 Definitions at Reset (cont.)

MD[a]	Logical Level		Definition
MD17 - MD16	Selects the number of Line Pulses per Frame		
	MD17	**MD16**	**Line Pulses per Frame**
	0	0	240
	0	1	242
	1	0	244
	1	1	800x600 (STN or TFT)
MD15	1		Select dual WE# DRAM
	0		Select dual CAS# DRAM
MD14	1		46E8 is the VGA enable port
	0		3C3 is the VGA enable port
MD13	1		Selects 16-bit data bus
	0		Selects 32-bit data bus
MD12	1		Select local bus
	0		Select AT bus
MD11-MD10	Bus ID pins		
	MD11	**MD10**	**Bus ID**
	0	0	PCI Bus
	0	1	386 VL-Bus
	1	0	486 VL-Bus
	1	1	Reserved
MD9	1		Selects general local bus interface
	0		Selects VESA local bus interface
MD8	1		Selects 3.3V for Host Bus Interface
	0		Selects 5V for Host Bus Interface
MD7-MD0	--		Reserved

a. MD15-MD8 are used when the feature connector option is enabled. See feature connector pinout definitions in Section 3.3.11 for details regarding the multiplexed definitions of the feature connector pins.

3.0 Signal Descriptions

3.1 Pin Diagrams

Figure 3-1 ISA Bus Pin Diagram

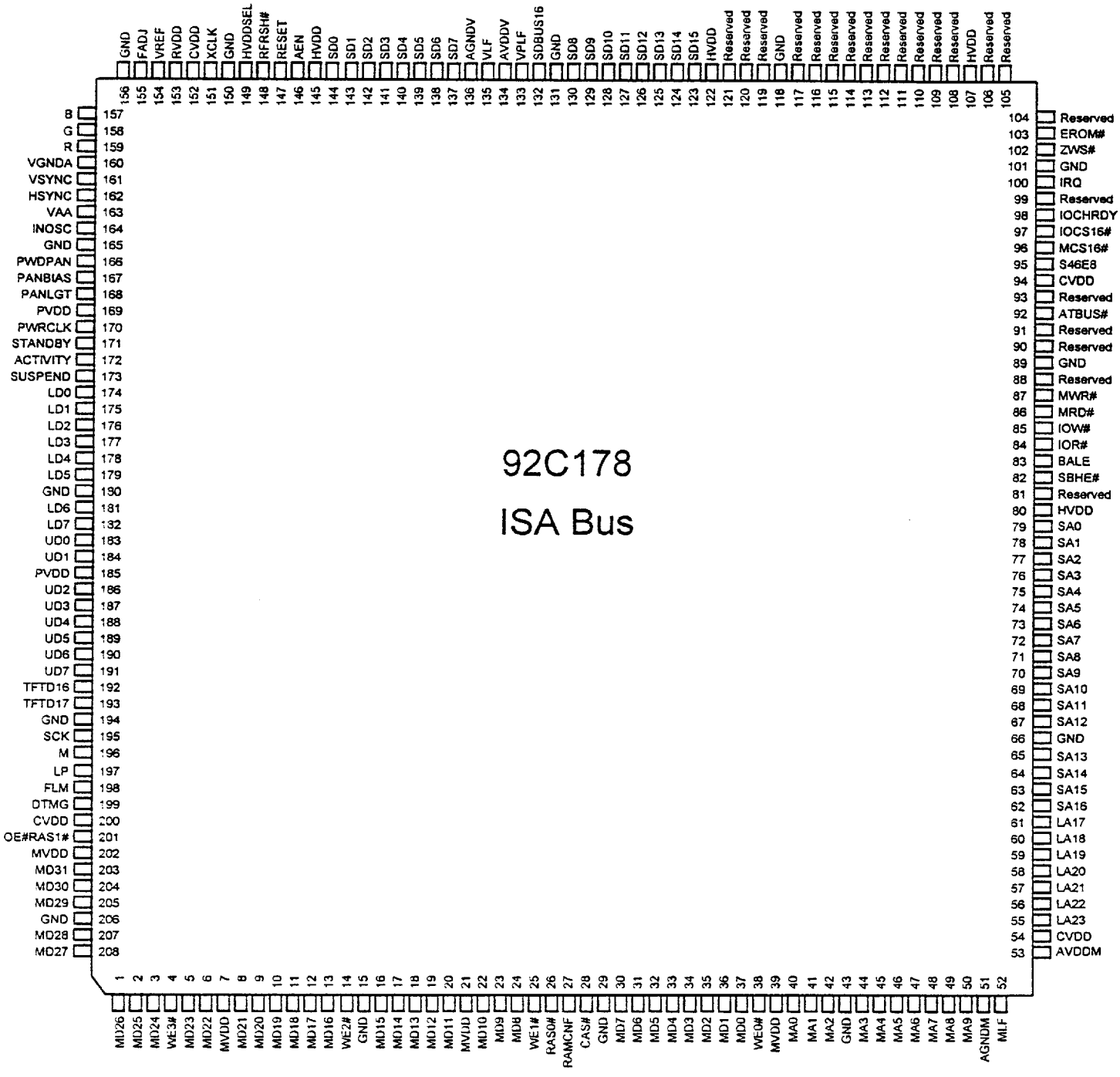


Figure 3-2 VL-Bus Pin Diagram

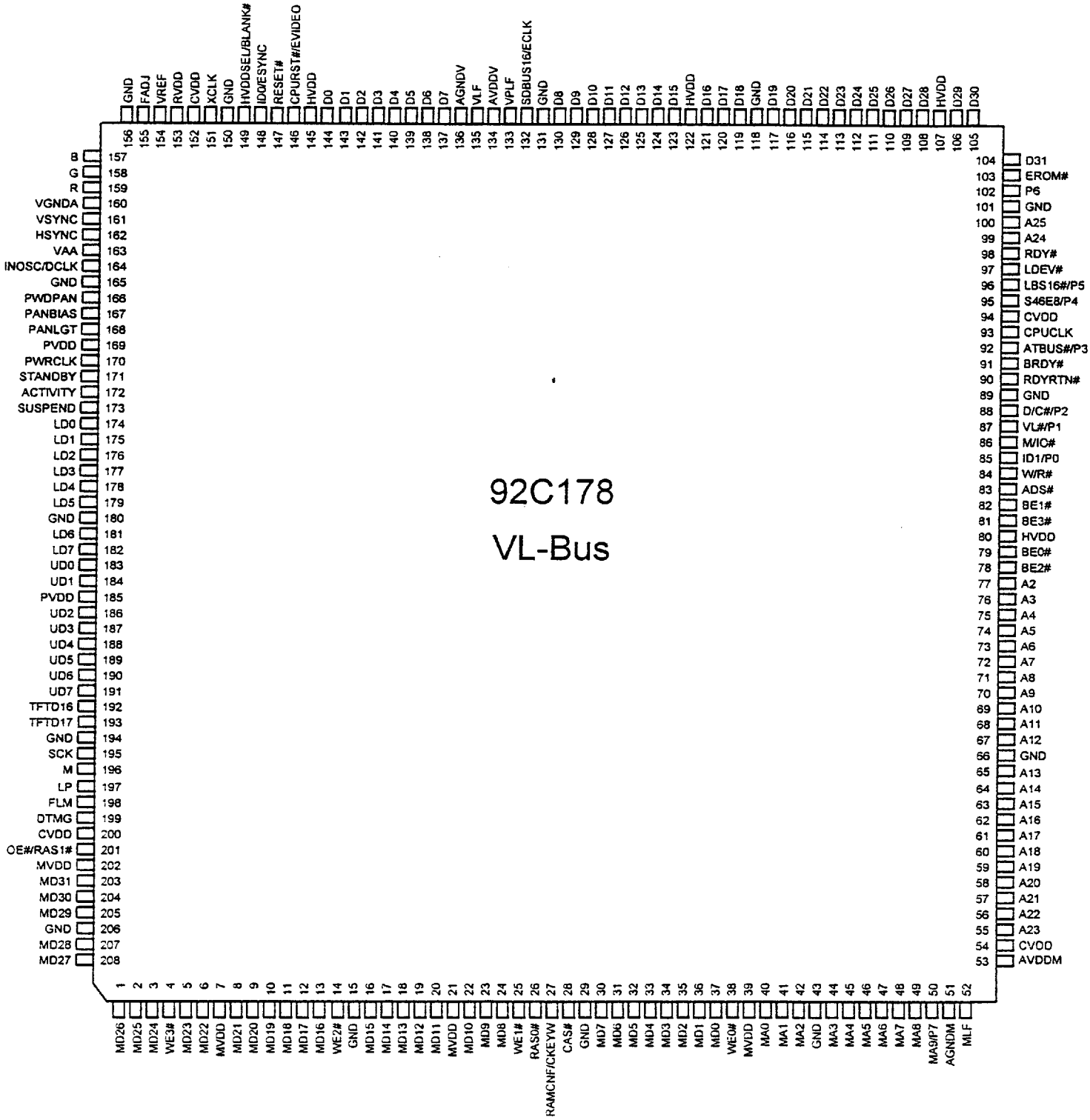
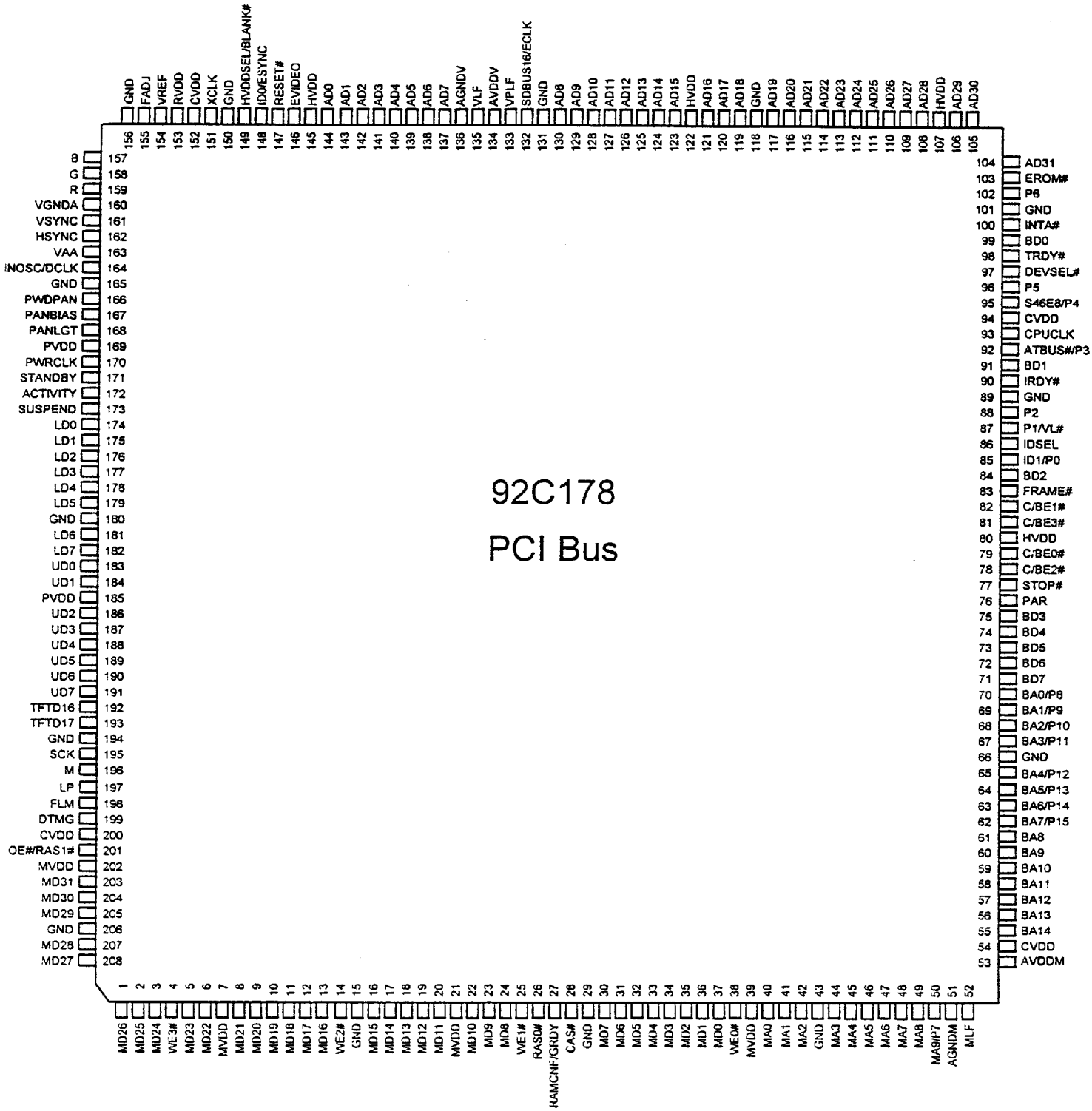


Figure 3-3 PCI Bus Pin Diagram



3.2 Pin Cross-Reference Lists

3.2.1 Alphabetical Pin List-ISA Bus

Pin	Name
81	--
88	--
90	--
91	--
93	--
99	--
104	--
105	--
106	--
108	--
109	--
110	--
111	--
112	--
113	--
114	--
115	--
116	--
117	--
119	--
120	--
121	--
172	ACTIVITY
146	AEN
51	AGNDM
136	AGNDV
92	ATBUS#
53	AVDDM
134	AVDDV
157	B
83	BALE
28	CAS#
54	CVDD
94	CVDD
152	CVDD
200	CVDD
199	DTMG
103	EROM#
155	FADJ
198	FLM
158	G
15	GND

Pin	Name
29	GND
43	GND
66	GND
89	GND
101	GND
118	GND
131	GND
150	GND
156	GND
165	GND
180	GND
194	GND
206	GND
162	HSYNC
80	HVDD
107	HVDD
122	HVDD
145	HVDD
149	HVDDSEL
164	INOSC
98	IOCHRDY
97	IOCS16#
84	IOR#
85	IOW#
100	IRQ
61	LA17
60	LA18
59	LA19
58	LA20
57	LA21
56	LA22
55	LA23
174	LD0
175	LD1
176	LD2
177	LD3
178	LD4
179	LD5
181	LD6
182	LD7
197	LP
196	M

Pin	Name
40	MA0
41	MA1
42	MA2
44	MA3
45	MA4
46	MA5
47	MA6
48	MA7
49	MA8
50	MA9
96	MCS16#
37	MD0
36	MD1
35	MD2
34	MD3
33	MD4
32	MD5
31	MD6
30	MD7
24	MD8
23	MD9
22	MD10
20	MD11
19	MD12
18	MD13
17	MD14
16	MD15
13	MD16
12	MD17
11	MD18
10	MD19
9	MD20
8	MD21
6	MD22
5	MD23
3	MD24
2	MD25
1	MD26
208	MD27
207	MD28
205	MD29
204	MD30

Pin	Name
203	MD31
52	MLF
86	MRD#
7	MVDD
21	MVDD
39	MVDD
202	MVDD
87	MWR#
201	OE#/RAS1#
167	PANBIAS
168	PANLGT
166	PWDPAN
170	PWRCLK
169	PVDD
185	PVDD
159	R
27	RAMCNF
26	RAS0#
147	RESET
148	RFRSH#
153	RVDD
95	S46E8
79	SA0
78	SA1
77	SA2
76	SA3
75	SA4
74	SA5
73	SA6
72	SA7
71	SA8
70	SA9
69	SA10
68	SA11
67	SA12
65	SA13
64	SA14
63	SA15
62	SA16
82	SBHE#
195	SCK
144	SD0

Pin	Name
143	SD1
142	SD2
141	SD3
140	SD4
139	SD5
138	SD6
137	SD7
130	SD8
129	SD9
128	SD10
127	SD11
126	SD12
125	SD13
124	SD14
123	SD15
132	SDBUS16
171	STANDBY
173	SUSPEND
192	TFTD16
193	TFTD17
183	UD0
184	UD1
186	UD2
187	UD3
188	UD4
189	UD5
190	UD6
191	UD7
163	VAA
160	VGNDA
135	VLF
133	VPLF
154	VREF
161	VSYNC
38	WE0#
25	WE1#
14	WE2#
4	WE3#
151	XCLK
102	ZWS#

3.2.2 Numerical Pin List-ISA Bus

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	MD26	43	GND	85	IOW#	127	SD11	169	PVDD
2	MD25	44	MA3	86	MRD#	128	SD10	170	PWRCLK
3	MD24	45	MA4	87	MWR#	129	SD9	171	STANDBY
4	WE3#	46	MA5	88	–	130	SD8	172	ACTIVITY
5	MD23	47	MA6	89	GND	131	GND	173	SUSPEND
6	MD22	48	MA7	90	–	132	SDBUS16	174	LD0
7	MVDD	49	MA8	91	–	133	VPLF	175	LD1
8	MD21	50	MA9	92	ATBUS#	134	AVDDV	176	LD2
9	MD20	51	AGNDM	93	–	135	VLF	177	LD3
10	MD19	52	MLF	94	CVDD	136	AGNDV	178	LD4
11	MD18	53	AVDDM	95	S46E8	137	SD7	179	LD5
12	MD17	54	CVDD	96	MCS16#	138	SD6	180	GND
13	MD16	55	LA23	97	IOCS16#	139	SD5	181	LD6
14	WE2#	56	LA22	98	IOCHRDY	140	SD4	182	LD7
15	GND	57	LA21	99	–	141	SD3	183	UD0
16	MD15	58	LA20	100	IRQ	142	SD2	184	UD1
17	MD14	59	LA19	101	GND	143	SD1	185	PVDD
18	MD13	60	LA18	102	ZWS#	144	SD0	186	UD2
19	MD12	61	LA17	103	EROM#	145	HVDD	187	UD3
20	MD11	62	SA16	104	–	146	AEN	188	UD4
21	MVDD	63	SA15	105	–	147	RESET	189	UD5
22	MD10	64	SA14	106	–	148	RFRSH#	190	UD6
23	MD9	65	SA13	107	HVDD	149	HVDDSEL	191	UD7
24	MD8	66	GND	108	–	150	GND	192	TFTD16
25	WE1#	67	SA12	109	–	151	XCLK	193	TFTD17
26	RAS0#	68	SA11	110	–	152	CVDD	194	GND
27	RAMCNF	69	SA10	111	–	153	RVDD	195	SCK
28	CAS#	70	SA9	112	–	154	VREF	196	M
29	GND	71	SA8	113	–	155	FADJ	197	LP
30	MD7	72	SA7	114	–	156	GND	198	FLM
31	MD6	73	SA6	115	–	157	B	199	DTMG
32	MD5	74	SA5	116	–	158	G	200	CVDD
33	MD4	75	SA4	117	–	159	R	201	OE#/RAS1#
34	MD3	76	SA3	118	GND	160	VGNDA	202	MVDD
35	MD2	77	SA2	119	–	161	VSYNC	203	MD31
36	MD1	78	SA1	120	–	162	HSYNC	204	MD30
37	MD0	79	SA0	121	–	163	VAA	205	MD29
38	WE0#	80	HVDD	122	HVDD	164	INOSC	206	GND
39	MVDD	81	–	123	SD15	165	GND	207	MD28
40	MA0	82	SBHE#	124	SD14	166	PWDPAN	208	MD27
41	MA1	83	BALE	125	SD13	167	PANBIAS		
42	MA2	84	IOR#	126	SD12	168	PANLGT		

3.2.3 Alphabetical Pin List-VL Bus

Pin	Name
77	A2
76	A3
75	A4
74	A5
73	A6
72	A7
71	A8
70	A9
69	A10
68	A11
67	A12
65	A13
64	A14
63	A15
62	A16
61	A17
60	A18
59	A19
58	A20
57	A21
56	A22
55	A23
99	A24
100	A25
172	ACTIVITY
83	ADS#
51	AGNDM
136	AGNDV
92	ATBUS#/P3
53	AVDDM
134	AVDDV
157	B
79	BE0#
82	BE1#
78	BE2#
81	BE3#
91	BRDY#
28	CAS#
93	CPUCLK
146	CPURST#/ EVIDEO
54	CVDD
94	CVDD
152	CVDD
200	CVDD
144	D0
143	D1
142	D2
141	D3
140	D4
139	D5
138	D6
137	D7
130	D8
129	D9
128	D10
127	D11
126	D12
125	D13
124	D14
123	D15
121	D16
120	D17
119	D18
117	D19
116	D20
115	D21
114	D22
113	D23
112	D24
111	D25
110	D26
109	D27
108	D28
106	D29
105	D30
104	D31
88	D/C#/P2
199	DTMG
103	EROM#
155	FADJ
198	FLM
158	G
15	GND
29	GND
43	GND
66	GND
89	GND
101	GND
118	GND
131	GND
150	GND
156	GND
165	GND
180	GND
194	GND
206	GND
162	HSYNC
80	HVDD
107	HVDD
122	HVDD
145	HVDD
149	HVDDSEL/ BLANK#
148	ID0/ESYNC
85	ID1/P0
164	INOSC/DCLK
96	LBS16#/P5
174	LD0
175	LD1
176	LD2
177	LD3
178	LD4
179	LD5
181	LD6
182	LD7
97	LDEV#
197	LP
196	M
86	M/IO#
40	MA0
41	MA1
42	MA2
44	MA3
45	MA4
46	MA5
47	MA6
48	MA7
49	MA8
50	MA9/P7
37	MD0
36	MD1
35	MD2
34	MD3
33	MD4
32	MD5
31	MD6
30	MD7
24	MD8
23	MD9
22	MD10
20	MD11
19	MD12
18	MD13
17	MD14
16	MD15
13	MD16
12	MD17
11	MD18
10	MD19
9	MD20
8	MD21
6	MD22
5	MD23
3	MD24
2	MD25
1	MD26
208	MD27
207	MD28
205	MD29
204	MD30
203	MD31
52	MLF
7	MVDD
21	MVDD
39	MVDD
202	MVDD
201	OE#/RAS1#
102	P6
167	PANBIAS
168	PANLGT
166	PWDPAN
170	PWRCLK
169	PVDD
185	PVDD
159	R
27	RAMCNF/ CKEYW
26	RAS0#
98	RDY#
90	RDYRTN#
147	RESET#
153	RVDD
95	S46E8/P4
195	SCK
132	SDBUS16/ECLK
171	STANDBY
173	SUSPEND
192	TFTD16
193	TFTD17
183	UD0
184	UD1
186	UD2
187	UD3
188	UD4
189	UD5
190	UD6
191	UD7
163	VAA
160	VGNDA
87	VL#/P1
135	VLF
133	VPLF
154	VREF
161	VSYNC
84	W/R#
38	WE0#
25	WE1#
14	WE2#
4	WE3#
151	XCLK

3.2.4 Numerical Pin List-VL Bus

Pin	Name
1	MD26
2	MD25
3	MD24
4	WE3#
5	MD23
6	MD22
7	MVDD
8	MD21
9	MD20
10	MD19
11	MD18
12	MD17
13	MD16
14	WE2#
15	GND
16	MD15
17	MD14
18	MD13
19	MD12
20	MD11
21	MVDD
22	MD10
23	MD9
24	MD8
25	WE1#
26	RAS0#
27	RAMCNF/ CKEYW
28	CAS#
29	GND
30	MD7
31	MD6
32	MD5
33	MD4
34	MD3
35	MD2
36	MD1
37	MD0
38	WE0#
39	MVDD
40	MA0
41	MA1
42	MA2

Pin	Name
43	GND
44	MA3
45	MA4
46	MA5
47	MA6
48	MA7
49	MA8
50	MA9/P7
51	AGNDM
52	MLF
53	AVDDM
54	CVDD
55	A23
56	A22
57	A21
58	A20
59	A19
60	A18
61	A17
62	A16
63	A15
64	A14
65	A13
66	GND
67	A12
68	A11
69	A10
70	A9
71	A8
72	A7
73	A6
74	A5
75	A4
76	A3
77	A2
78	BE2#
79	BE0#
80	HVDD
81	BE3#
82	BE1#
83	ADS#
84	W/R#
85	ID1/P0

Pin	Name
86	M/IO#
87	VL#/P1
88	D/C#/P2
89	GND
90	RDYRTN#
91	BRDY#
92	ATBUS#/P3
93	CPUCLK
94	CVDD
95	S46E8/P4
96	LBS16#/P5
97	LDEV#
98	RDY#
99	A24
100	A25
101	GND
102	P6
103	EROM#
104	D31
105	D30
106	D29
107	HVDD
108	D28
109	D27
110	D26
111	D25
112	D24
113	D23
114	D22
115	D21
116	D20
117	D19
118	GND
119	D18
120	D17
121	D16
122	HVDD
123	D15
124	D14
125	D13
126	D12
127	D11
128	D10

Pin	Name
129	D9
130	D8
131	GND
132	SDBUS16/ECLK
133	VPLF
134	AVDDV
135	VLF
136	AGNDV
137	D7
138	D6
139	D5
140	D4
141	D3
142	D2
143	D1
144	D0
145	HVDD
146	CPURST#/ EVIDEO
147	RESET#
148	ID0/ESYNC
149	HVDDSEL/ BLANK#
150	GND
151	XCLK
152	CVDD
153	RVDD
154	VREF
155	FADJ
156	GND
157	B
158	G
159	R
160	VGNDA
161	VSYNC
162	HSYNC
163	VAA
164	INOSC/DCLK
165	GND
166	PWDPAN
167	PANBIAS
168	PANLGT
169	PVDD
170	PWRCLK

Pin	Name
171	STANDBY
172	ACTIVITY
173	SUSPEND
174	LD0
175	LD1
176	LD2
177	LD3
178	LD4
179	LD5
180	GND
181	LD6
182	LD7
183	UD0
184	UD1
185	PVDD
186	UD2
187	UD3
188	UD4
189	UD5
190	UD6
191	UD7
192	TFTD16
193	TFTD17
194	GND
195	SCK
196	M
197	LP
198	FLM
199	DTMG
200	CVDD
201	OE#/RAS1#
202	MVDD
203	MD31
204	MD30
205	MD29
206	GND
207	MD28
208	MD27

3.2.5 Alphabetical Pin List-PCI Bus

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
172	ACTIVITY	67	BA3/P11	89	GND	37	MD0	167	PANBIAS
144	AD0	65	BA4/P12	101	GND	36	MD1	168	PANLGT
143	AD1	64	BA5/P13	118	GND	35	MD2	76	PAR
142	AD2	63	BA6/P14	131	GND	34	MD3	166	PWDPAN
141	AD3	62	BA7/P15	150	GND	33	MD4	170	PWRCLK
140	AD4	61	BA8	156	GND	32	MD5	169	PVDD
139	AD5	60	BA9	165	GND	31	MD6	185	PVDD
138	AD6	59	BA10	180	GND	30	MD7	159	R
137	AD7	58	BA11	194	GND	24	MD8	27	RAMCNF/GRDY
130	AD8	57	BA12	206	GND	23	MD9	26	RAS0#
129	AD9	56	BA13	162	HSYNC	22	MD10	147	RESET#
128	AD10	55	BA14	80	HVDD	20	MD11	153	RVDD
127	AD11	99	BD0	107	HVDD	19	MD12	95	S46E8/P4
126	AD12	91	BD1	122	HVDD	18	MD13	195	SCK
125	AD13	84	BD2	145	HVDD	17	MD14	132	SDBUS16/ECLK
124	AD14	75	BD3	149	HVDDSEL/BLANK#	16	MD15	171	STANDBY
123	AD15	74	BD4	148	ID0/ESYNC	13	MD16	77	STOP#
121	AD16	73	BD5	85	ID1/P0	12	MD17	171	SUSPEND
120	AD17	72	BD6	86	IDSEL	11	MD18	192	TFTD16
119	AD18	71	BD7	164	INOSC/DCLK	10	MD19	193	TFTD17
117	AD19	79	C/BE0#	100	INTA#	9	MD20	98	TRDY#
116	AD20	82	C/BE1#	90	IRDY#	8	MD21	183	UD0
115	AD21	78	C/BE2#	174	LD0	6	MD22	184	UD1
114	AD22	81	C/BE3#	175	LD1	5	MD23	186	UD2
113	AD23	28	CAS#	176	LD2	3	MD24	187	UD3
112	AD24	93	CPUCLK	177	LD3	2	MD25	188	UD4
111	AD25	54	CVDD	178	LD4	1	MD26	189	UD5
110	AD26	94	CVDD	179	LD5	208	MD27	190	UD6
109	AD27	152	CVDD	181	LD6	207	MD28	191	UD7
108	AD28	200	CVDD	182	LD7	205	MD29	163	VAA
106	AD29	97	DEVSEL#	197	LP	204	MD30	160	VGNDA
105	AD30	199	DTMG	196	M	203	MD31	135	VLF
104	AD31	103	EROM#	40	MA0	52	MLF	133	VPLF
51	AGNDM	146	EVIDEO	41	MA1	7	MVDD	154	VREF
136	AGNDV	155	FADJ	42	MA2	21	MVDD	161	VSYNC
92	ATBUS#/P3	198	FLM	44	MA3	39	MVDD	38	WE0#
53	AVDDM	83	FRAME#	45	MA4	202	MVDD	25	WE1#
134	AVDDV	158	G	46	MA5	201	OE#/RAS1#	14	WE2#
157	B	15	GND	47	MA6	87	P1/VL#	4	WE3#
70	BA0/P8	29	GND	48	MA7	88	P2	151	XCLK
69	BA1/P9	43	GND	49	MA8	96	P5		
68	BA2/P10	66	GND	50	MA9/P2	102	P6		

3.2.6 Numerical Pin List-PCI Bus

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	MD26	43	GND	85	ID1/P0	127	AD11	169	PVDD
2	MD25	44	MA3	86	IDSEL	128	AD10	170	PWRCLK
3	MD24	45	MA4	87	P1/VL#	129	AD9	171	STANDBY
4	WE3#	46	MA5	88	P2	130	AD8	172	ACTIVITY
5	MD23	47	MA6	89	GND	131	GND	173	SUSPEND
6	MD22	48	MA7	90	IRDY#	132	SDBUS16/ECLK	174	LD0
7	MVDD	49	MA8	91	BD1	133	VPLF	175	LD1
8	MD21	50	MA9/P2	92	ATBUS#/P3	134	AVDDV	176	LD2
9	MD20	51	AGNDM	93	CPUCLK	135	VLF	177	LD3
10	MD19	52	MLF	94	CVDD	136	AGNDV	178	LD4
11	MD18	53	AVDDM	95	S46E8/P4	137	AD7	179	LD5
12	MD17	54	CVDD	96	P5	138	AD6	180	GND
13	MD16	55	BA14	97	LDEV#	139	AD5	181	LD6
14	WE2#	56	BA13	98	RDY#	140	AD4	182	LD7
15	GND	57	BA12	99	BD0	141	AD3	183	UD0
16	MD15	58	BA11	100	IRQ	142	AD2	184	UD1
17	MD14	59	BA10	101	GND	143	AD1	185	PVDD
18	MD13	60	BA9	102	P6	144	AD0	186	UD2
19	MD12	61	BA8	103	EROM#	145	HVDD	187	UD3
20	MD11	62	BA7/P15	104	AD31	146	EVIDEO	188	UD4
21	MVDD	63	BA6/P14	105	AD30	147	RESET#	189	UD5
22	MD10	64	BA5/P13	106	AD29	148	ID0/ESYNC	190	UD6
23	MD9	65	BA4/P12	107	HVDD	149	HVDDSEL/BLANK#	191	UD7
24	MD8	66	GND	108	AD28	150	GND	192	TFTD16
25	WE1#	67	BA3/P11	109	AD27	151	XCLK	193	TFTD17
26	RAS0#	68	BA2/P10	110	AD26	152	CVDD	194	GND
27	RAMCNF/GRDY	69	BA1/P9	111	AD25	153	RVDD	195	SCK
28	CAS#	70	BA0/P8	112	AD24	154	VREF	196	M
29	GND	71	BD7	113	AD23	155	FADJ	197	LP
30	MD7	72	BD6	114	AD22	156	GND	198	FLM
31	MD6	73	BD5	115	AD21	157	B	199	DTMG
32	MD5	74	BD4	116	AD20	158	G	200	CVDD
33	MD4	75	BD3	117	AD19	159	R	201	OE#/RAS1#
34	MD3	76	PAR	118	GND	160	VGNDA	202	MVDD
35	MD2	77	STOP#	119	AD18	161	VSYNC	203	MD31
36	MD1	78	C/BE2#	120	AD17	162	HSYNC	204	MD30
37	MD0	79	C/BE0#	121	AD16	163	VAA	205	MD29
38	WE0#	80	HVDD	122	HVDD	164	INOSC/DCLK	206	GND
39	MVDD	81	C/BE3#	123	AD15	165	GND	207	MD28
40	MA0	82	C/BE1#	124	AD14	166	PWDPAN	208	MD27
41	MA1	83	FRAME#	125	AD13	167	PANBIAS		
42	MA2	84	BD2	126	AD12	168	PANLGT		

3.3 Interface Signals

3.3.1 Host Interface- ISA Bus

Pin Name	Pin	Type	Description
AEN	146	I	Address Enable. When active, indicates DMA is occurring over the ISA bus. The 92C178 will ignore any I/O cycles while this signal is active. AEN has no effect on memory read/write commands.
ATBUS#	92	I	Bus configuration pin. For ISA, tie to GND through a 4.7Kohm resistor.
BALE	83	I	Bus Address Latch Enable. Signals LA23 through LA17 are latched inside the 92C178 at the falling edge of this signal.
CPUCLK	93	I	CPU Clock. This pin should be tied to GND through a 4.7Kohm resistor.
EROM#	103	O	Enable BIOS ROM. This signal is activated for memory read cycles which fall in the address range of the video BIOS. The address range is C000:0-C7FFF:F.
IOCHRDY	98	O	I/O Channel Ready. This signal is used to request additional wait states for completion a video memory access cycle. IOCHRDY is not generated for I/O access, BIOS ROM access, or for zero-wait state video memory writes.
IOCS16#	97	O	I/O Chip Select 16 for ISA bus. This signal responds to the host to enable 16-bit I/O access.
IOR#	84	I	ISA bus I/O read strobe.
IOW#	85	I	ISA bus I/O write strobe.
IRQ	100	O	Interrupt Request. Interrupt generation is enabled by bit 5 of the Vertical Sync End Register (3D5.11). Interrupt requests are generated at the vertical display end time.
LA23- LA17	55-61	I	Unlatched system address bus bits 23 through 17.
MCS16#	96	O	Memory Chip Select 16 for ISA bus. This signal responds to the host to enable 16-bit video memory read/writes. The 92C178 will also activate this signal for I/O commands.
MRD#	86	I	ISA bus memory read strobe.
MWR#	87	I	ISA bus memory write strobe.
RESET	147	I	Reset. This pin used initialize the 92C178 to a known state. At the falling edge of RESET, the 92C178 will latch the data on MD31-16 into Configuration Registers 2 and 1 (3C5.1E and 3C5.1F) and the hardware configuration pin values into Configuration Register 0 (3C5.1D).
RFRSH#	148	I	Refresh. This pin indicates that DRAM refresh is occurring over the ISA bus. The 92C178 will ignore any memory read/write cycles while this signal is active. This signal has no effect on I/O commands.
S46E8	95	I	VGA enable port select. A logical 1 selects port 46E8 as the VGA enable port. A logical 0 selects 3C3 as the VGA enable port. Signal should be tied through a 4.7Kohm resistor.
SA16-SA0	62-65, 67-79	I	System address bus bits 16 through 0.
SBHE#	82	I	System Bus High Byte Enable. Enables high byte data transfer on the ISA bus.
SD15:0	123-130, 137-144	I/O	ISA data bus pins 15-0.

3.3.1 Host Interface- ISA Bus (cont.)

Pin Name	Pin	Type	Description
SDBUS16	132	I	Data bus configuration pin. Configures the system data bus as 16-bit or 32-bit. For ISA bus, this pin should be tied to HVDD through a 4.7Kohm resistor.
ZWS#	102	O	Zero Wait State signal. This signal is used to indicate the 92C178 can process a zero wait state video memory write command. ZWS# can be generated when the write buffer is not full.

3.3.2 Host Interface-VESA Local Bus

Pin Name	Pin	Type	Description
A25-A2	100, 99, 55-65, 67-77	I	Local bus address bits 25-2.
ATBUS#/P3	92	I /O	AT Bus Select. When the feature connector is disabled, this pin should be tied high through a 4.7Kohm resistor for local bus configurations. This pin is defined as P3 when the feature connector is enabled. When the feature connector is enabled, the value for ATBUS# is determined by MD12 at power-on.
ADS#	83	I	Address Data Strobe. Indicates start of a local bus cycle.
BE3#-BE0#	81, 78, 82, 79	I	Byte Enables 3-0. A logical 0 indicates valid data for the given byte lane.
BRDY#	91	I	Burst Ready. Signal used to reset the bus interface state machine after a burst cycle on the local bus. The signal is needed since not all system core logic generates RDYRTN# upon completion of a local bus burst cycle.
CPUCLK	93	I	CPU Clock. Timing reference clock for local bus. Bus timing is synchronized to the rising edge of this clock. The clock rate should be 1X CPU clock for a 486 local bus implementation and 2X CPU clock for a 386 local bus implementation. For the 386 local bus implementation, the 92C178 divides the clock internally to drive the chip logic.
CPURST#/ EVIDEO	146	I/O	CPU Reset. This signal is used to reset the 92C178's internal CPU clock divider and to synchronize the internal state machine. The signal should be connected for non-VL Bus solutions which use a 2X input clock (VL# high, and ID1, ID0 configured for i386). This signal is not required for VL-Bus solutions. This pin is defined as EVIDEO when the feature connector is enabled.
D/C#/P2	88	I	Data/Code. Indicates whether the current cycle is transmitting data or code. This pin is defined as P2 when the feature connector is enabled.
EROM#/P7	103	I/O	Enable BIOS ROM. This signal is activated for memory read cycles which fall in the address range of the video BIOS. The address range is C000:0-C7FFF:F. This pin is defined as P7 when the feature connector is enabled.
ID1/P0- ID0/ESYNC	85, 148	I/O I	ID Pins 1 and 0. These pins are used in combination with pin VL# (pin 87) and ATBUS# (pin 92) to configure bus type. Each pin should be tied through a 4.7Kohm resistor. See Table 1 in Bus Interface Unit section for additional details. These pins are described as P0 and ESYNC when the feature connector is enabled. When the feature connector is enabled, ID1 and ID0 are determined by MD11 and MD10, respectively, at power-on.
LBS16#/P5	96	I/O	Local Bus Select 16. Informs the CPU to transfer only up to 16 bits of data. The 92C178 will activate this signal for local bus I/O commands. This pin is defined as P5 when the feature connector is enabled.

3.3.2 Host Interface-VESA Local Bus (cont.)

Pin Name	Pin	Type	Description
LDEV#	97	O	Local Device. Informs the core logic that the 92C178 will respond to the current cycle.
M/IO#	86	I	Memory/IO. Indicates whether the current cycle is a memory or I/O transaction.
RDY#	98	O	Ready. Informs the system core logic that processing for the current local bus cycle has been completed.
RDYRTN#	90	I	Ready Return. This pin is the Ready feedback from the core logic to terminate the current local bus cycle and reset the bus interface state machine.
RESET#	147	I	Reset. This pin used initialize the 92C178 to a known state. At the rising edge of RESET#, the 92C178 will latch the data on MD31-16 into Configuration Registers 2 and 1 (3C5.1E and 3C5.1F) and the hardware configuration pin values into Configuration Register 0 (3C5.1D).
S46E8/P4	95	I /O	VGA enable port select. A logical 1 selects port 46E8 as the VGA enable port. A logical 0 selects 3C3 as the VGA enable port. When the feature connector is disabled, pull high or low through a 4.7Kohm resistor. This pin is defined as P4 when the feature connector is enabled. When the feature connector is enabled, the value for S46E8 is determined by MD14 at power-on.
SD31:0	104-106, 108-117, 119-121, 123-130, 137-144	I/O	These pins are the system data bus that are connected directly to the local data bus. For ISA or 386SX local bus, the SD31:16 pins are not connected.
SDBUS16/ ECLK	132	I	Data bus configuration pin. Configures the system data bus as 16-bit or 32-bit. For ISA bus, this pin should be tied to HVDD through a 4.7Kohm resistor. This pin is defined as ECLK when the feature connector is enabled. When the feature connector is enabled, the value for SDBUS16 is determined by MD13 at power-on.
VL#/P1	87	I/O	VL-Bus Select. Selects VL-bus or general purpose local bus. A logical 0 selects VL-Bus. A logical 1 selects general purpose local bus. Pin should be tied through a 4.7Kohm resistor. This pin is defined as P1 when the feature connector is enabled. When the feature connector is enabled, the value for VL# is determined by MD9 at power-on.
W/R#	84	I	Write/Read. Indicates whether the current cycle is a read or write transaction.

3.3.3 Host Interface-PCI Bus

Pin Name	Pin	Type	Description
AD[31:0]	104-106, 108-117, 119-121, 123-130, 137-144	I/O	Multiplexed Address and Data Lines, bits 31 through 0: These pins are the multiplexed PCI address and data lines. During the address phase, these pins are inputs. During the data phase, these pins are inputs for write cycles or outputs for read cycles.
ATBUS#/P3	92	I/O	AT Bus Select. When the feature connector is disabled, tie this pin high through a 4.7Kohm resistor. This pin is defines as P3 when the feature connector is enabled. When the feature connector is enabled, the value for ATBUS# is determined by MD12 at power-on.
C/BE[3:0]#	81, 78, 82, 79	I	Bus Command and Byte Enables, bits 3 through 0: These pins are the multiplexed PCI command and byte enable lines.

3.3.3 Host Interface-PCI Bus (cont.)

Pin Name	Pin	Type	Description
CPUCLK	93	I	CPU Clock: Timing reference clock for PCI Bus. Connect directly to the PCI Bus Clock.
DEVSEL#	97	O	Device Select: This signal is driven low when the 92C178 decodes its address as the target of the current access.
FRAME#	83	I	Cycle Frame: This pin is driven by the PCI bus master to indicate the beginning and duration of an access.
ID1/P0, ID0/ESYNC	85 148	I/O I	ID Pins 1 and 0. When the feature connector is disabled, these pins should be tied low through a 4.7Kohm resistor. These pins are defined as P0 and ESYNC when the feature connector is enabled. When the feature connector is enabled, the values for ID1 and ID0 are determined by MD10 and MD9, respectively, at power-on.,
IDSEL	86	I	ID Select. This signal is used as a chip select for PCI configuration space accesses.
INTA#	100	O	Interrupt Request. Interrupt generation is enabled by bit 5 of the Vertical Sync End register (3D5.11). Interrupt requests are generated at the Vertical Display Enable End time.
IRDY#	90	I	Initiator Ready: This signal is asserted by the PCI bus master to indicate the ability to complete the current data phase of the transaction.
PAR	76	I/O	Parity: This signal is used to provide even parity across AD31-AD0 and C/BE3#-C/BE0#. This signal is sampled as an input during write cycles and provides correct parity as an output for read cycles.
S46E8/P4	95	I/O	VGA port enable select. A logical 1 selects port 46E8 as the VGA enable port. A logical 0 selects 3C3 as the VGA enable port. When the feature connector is disabled, pull high or low through a 4.7Kohm resistor. This pin is defined as P4 when the feature connector is enabled. When the feature connector is enabled, the value for S46E8 is determined by MD14 at power-on.
SDBUS16/ ECLK	132	I	Data bus configuration pin. When the feature connector is disabled, pull low through a 4.7Kohm resistor. This pin is defined as ECLK when the feature connector is enabled. When the feature connector is enabled, the value for SDBUS16 is determined by MD13 at power-on.
STOP#	77	O	Stop: This signal is used by the target to request the master to stop the current transaction.
TRDY#	98	O	Target Ready: This pin is asserted by the 92C178 to indicate the ability to complete the current data phase of the transaction.
BA14-BA0*	55-65, 67-70	O	BIOS Address bits 14-0. BA7-BA0 function as P15-P8 when the 16-bit feature connector is enabled.
BD7-BD0*	71-75, 84, 91, 99	I	BIOS Data bits 7-0.
EROM#	103	O	Enable BIOS ROM. This signal is activated for memory read cycles which fall in the address range of the video BIOS (C000:0-C7FF:F).

* To enable BA14-BA0 and BD7-BD0 pin definitions, pull MD30 to logical 0 at power-on. Pull MD30 low through a 4.7kΩ resistor.

3.3.4 Memory Interface

Pin Name	Pin	Type	Description
CAS#	28	O	DRAM column address strobe. When signal RAMCNF is pulled low, this pin functions as WE# for display memory (for 256Kx16 dual CAS DRAM).
MA9:0	50-44, 42-40	O	Memory address bus pins 9-0. MA8-MA0 are used for standard 256Kx4 and 256Kx16 DRAM. MA9 is used for asymmetric 256Kx16 DRAM. MA9 functions as P7 when the feature connector is enabled.
MD31:0	203-205, 207-208, 1-3,5-6, 8-13, 16-20, 22-24, 30-37	I/O	Memory data bus pins 31-0.
OE#/RAS1#	201	O	DRAM output enable signal for 512K/1MB configurations. For 2MB configurations, this pin is used as RAS1#. For the 2MB case, the OE# of the DRAM should just be tied to GND.
RAMCNF/ CKEYW	27	I	DRAM Configuration pin. Defines signals WE3#-WE0# and CAS# for different DRAM types. Signal should be tied through a 4.7Kohm resistor. Reference the CAS# and WE# pin descriptions for configuration details. When the feature connector is enabled, this pin is defined as CKEYW and the value for RAMCNF is determined by MD15 at power-on.
RAS0#	26	O	DRAM row address strobe.
WE3#-WE0#	4,14,25,38	O	DRAM Write Enables. When signal RAMCNF (pin 27) is pulled high, these pins are write enable signals for the display memory (for 256Kx4 or 256Kx16 dual WE DRAM). When signal RAMCFG is pulled low, these pins function as CAS# signals for display memory (for 256Kx16 dual CAS DRAM).

3.3.5 CRT Interface

Pin Name	Pin	Type	Description
B	157	O	Blue DAC output. Blue CRT analog video output from the internal DAC module. This pin provides a high impedance current source to drive a doubly terminated 75ohm coaxial cable to the CRT.
FADJ	155	I	Full Scale Current. This pin is connected to GND through a resister to set the full scale current of the DAC. The full scale current is determined by the following equation: IFULLSCALE = 7.7273 * (VREF/R) Recommended value for the resistor is 690Ωs.
G	158	O	Green DAC output. Green CRT analog video output from the internal DAC module. This pin provides a high impedance current source to drive a doubly terminated 75ohm coaxial cable to the CRT.
HSYNC	162	I/TS/ O	Horizontal Sync. This signal provides horizontal sync to the CRT or the feature connector. This signal may be tristated when sync from the feature connector is being used to drive the CRT. The polarity of HSYNC is set by bit 6 of Miscellaneous Output Register (3C2). When configured as an input, the sync signal may be used to genlock the 92C178 to an external video source. When configured as an output, HSYNC may be used to support DPMS.

3.3.5 CRT Interface (cont.)

Pin Name	Pin	Type	Description
R	159	O	Red DAC output. Red CRT analog video output from the internal DAC module. This pin provides a high impedance current source to drive a doubly terminated 75ohm coaxial cable to the CRT.
VREF	154	I	Voltage Reference. This pin is the voltage reference input for the internal RAMDAC. The voltage level requirement is 1.22V
VSYNC	161	I/TS/ O	Vertical Sync. This signal provides vertical sync to the CRT or the feature connector. This signal may be tristated when sync from the feature connector is being used to drive the CRT. The polarity of VSYNC is set by bit 7 of the Miscellaneous Output Register (3C2). When configured as an input, the sync signal may be used to genlock the 92C178 to an external video source. When configured as an output, HSYNC may be used to support DPMS.

3.3.6 Panel Interface

Pin Name	Pin	Type	Description
DTMG	199	O	8-Bit STN Single Scan Color Panel: Signal used as shift clock for panel data bits LD3-LD0. TFT Color Panel: Signal used to enable data to the panel.
FLM	198	O	First Line Marker. This signal indicates the beginning of a frame. For STN panels, the line marker location is programmable by setting bits 7-0 of the First Line Marker Adjust Register (3D5.37). The polarity of this signal is set by bit 2 of the Flat Panel Output Control register (3D5.36)
LP	197	O	Line Pulse. Pulse output used to latch data into the current scan line of the panel. The polarity of this signal is set by bit 1 of the Flat Panel Output Control register (3D5.36)
M	196	O	Modulation Signal. This signal output provides AC inversion. M can be programmed to toggle every frame or every selected number of scan lines. Bits 7-0 of the Flat Panel FR Timing Adjustment Register (3D5.3C) are used for programming these options.
SCK	195	O	Shift Clock. This signal used to shift data into the X-driver of the panel. 8-Bit Single Scan STN Color Panel: Signal used as shift clock for panel data bits UD3-UD0.
TFTD17-TFTD16	193-192	O	TFT Data. These two pins are the blue data bits 5 and 4 respectively for an 18-bit TFT color panel.
UD7-UD0 LD7-LD0	191-186, 184, 183 182, 181, 179-174	O	4-Bit Single Scan STN Monochrome Panel: UD3-UD0 used for panel data. 8-Bit Single Scan STN Monochrome Panel: UD7-UD0 used for panel data. Dual Scan STN Monochrome Panel: For 640x480 panels, UD3-UD0 used for upper panel data and LD3-LD0 used for lower panel data. For 1024x768 panels, UD7-UD0 used for upper panel data and LD7-LD0 used for lower panel data. 8-Bit Single Scan STN Color Panel: UD7-UD0 used for panel data. 16-Bit Single Scan STN Color Panel: UD7-UD0 and LD7-LD0 used for panel data. 8-Bit Dual Scan STN Color Panel: UD3-UD0 used for upper panel data and LD3-LD0 used for lower panel data. 16-Bit Dual Scan STN Color Panel: UD7-UD0 used for upper panel data and LD7-LD0 used for lower panel data. TFT Color Panel: UD7, UD6 are used as green data bits 1 and 0. UD5-UD0 are used as red data bits 5-0. LD7-LD4 are used as blue data bits 3-0. LD3-LD0 are used as green data bits 5-2.

3.3.7 Power Management Interface

Pin Name	Pin	Type	Description
ACTIVITY	172	I	Activity. Pin used to indicate keyboard, mouse and/or VGA activity. A logical 1 indicates a keyboard interrupt, mouse interrupt, access to video memory, or I/O access to the 92C178's registers has occurred. A logical 0 indicates no activity. Activity detection will reset any enabled counter timers inside the 92C178.
INOSC/ DCLK	164	I/O	Power Down Input Oscillator. When the feature connector is disabled, this pin provides the clock input used for the power management logic, and for DRAM refresh timing when the 92C178 is in SUSPEND mode. This pin may be connected to the 14.318MHz system clock or to a 32KHz crystal. Bit 2 of the Power Down Clock Select Register (3D5.47) must be programmed to reflect the clock frequency used. If the system clock is used, bit 2 should be programmed to a logical 1. If the 32KHz crystal is used, bit 2 should be programmed to a logical 0. When the feature connector is enabled, this pin is defined as DCLK. For this case, XCLK (pin 151) is used to provide the clock for Suspend Mode DRAM timing.
PANBIAS	167	O	Panel Bias Power. This signal is used to turn panel bias power (VEE) on or off. Panel bias power is turned on/off during power sequencing and when entering/exiting Standby or Suspend Mode.
PANLGT	168	O	Panel Backlight Power. This signal is used to turn panel backlight power on or off. Panel bias power is turned on/off during power sequencing and when entering/exiting any of the three power-down modes.
PWDPAN	166	O	Panel Drive Power. This signal is used to turn panel drive power (VDD) on or off. Panel bias power is turned on/off during power sequencing and when entering/exiting Standby or Suspend Mode.
PWRCLK	170	O	Clock Power. This signal is used to force the external clock chip into a power-down state. If the external clock chip does not have a power-down pin, this signal can also used to directly shut off the power to the clock chip.
STANDBY	171	I/O	Standby. This pin may be programmed as an input or output. The direction is controlled by bit 3 of the Power Down Clock Select Register (3D5.47). Input: Functions as hardware control to put the 92C178 into the Standby Mode. Hardware Standby Mode is enabled by programming bit 2 of the Power Down Control Register (3D5.44) to a logical 1. Signal polarity is determined by bit 4 of the Power Down Clock Select Register (3D5.47). When STANDBY is activated, the 92C178 will enter the Standby Mode. When it is deactivated, the 92C178 will resume normal operations. Output: Reflects the state of the 92C178. Signal polarity is determined by bit 4 of the Power Down Clock Select Register (3D5.47). When STANDBY is activated, it means the standby counter timer in the has expired and 92C178 is Standby Mode. When it is deactivated, the 92C178 is in standard operating mode.
SUSPEND	173	I	Suspend. Functions as a hardware control to put the 92C178 into Suspend Mode. Hardware Suspend Mode is enabled by programming bit 3 of the Power Down Control Register (3D5.44) to a logical 1. Signal polarity is determined by bit 5 of the Power Down Clock Select Register (3D5.47). When SUSPEND is activated, the 92C178 will enter the Suspend Mode. When it is deactivated, the 92C178 will resume normal operations.

3.3.8 Clock Interface

Pin Name	Pin	Type	Description
MLF	52	–	Memory clock loop filter.
VLF	135	–	Video clock loop filter.

3.3.8 Clock Interface (cont.)

Pin Name	Pin	Type	Description
VPLF	133	--	Reserved signal. Tie to HVDD.
XCLK	151	I	14.318MHz crystal clock input.

3.3.9 Power Interface

Pin Name	Pin	Type	Description
AVDDM	53	Power	Analog power for the memory clock PPL (Phase Lock Loop).
AVDDV	134	Power	Analog power for the video clock PLL.
CVDD	54, 94, 152, 200		Power supply pins for the core logic. The voltage is either 5V or 3.3V + 10%
HVDD	80,107, 122,145		Power supply pins for the host interface. The voltage is either 5V or 3.3V + 10%.
HVDDSEL/ BLANK#	149	I/O	When the feature connector is disabled, this pin is configures the host interface as 3.3V or 5V. A logical 1 selects 3.3V. A logical 0 selects 5V*. The pin should be tied through a 4.7Kohm resistor. This pin is defined as BLANK# when the feature connector is enabled. When the feature connector is enabled, the value for HVDDSEL is determined by MD14 at power-on.
MVDD	202, 7,21,39		Power supply pins for the DRAM interface. The voltage is either 5V or 3.3V + 10%. Bit 1 of the Mixed Voltage Select Register configures the DRAM interface for the voltage on the MVDD pins. A logical 1 configures for 3.3V.
PVDD	169,185		Power supply pins for the panel interface. The voltage is either 5V or 3.3V + 10%. Bit 0 of the Mixed Voltage Select Register configures the panel interface for the voltage on the PVDD pins. A logical 1 configures for 3.3V.
RVDD	153		Power supply pin for the internal ram of the RAMDAC. The voltage is either 5V or 3.3V + 10%. It's voltage must be the same as CVDD.
VAA	163		Power supply for the internal DAC of the RAMDAC. The voltage is 5V + 10%.

* For PCI Bus configurations, HVDDSEL should always be a logical 0.

3.3.10 Signal Ground Interface

Pin Name	Pin	Type	Description
AGNDM	51	GND	Analog ground for the memory clock PLL.
AGNDV	136	GND	Analog ground for the video clock PLL.
GND	15,29,43, 66,89,101,118,131, 150,156, 165,180, 194,206		Ground pins.
VGND	160		Analog ground pin for the DAC module in the RAMDAC.

3.3.11 Feature Connector Interface

NOTE MD31 must be set to a logical 1 at power-on in order to enable the feature connector interface. An 8-bit feature connector interface is supported for PCI bus and VL-Bus. A VAFC compatible 16-bit feature connector interface is supported for PCI bus. Bit 6 of the Extended Mode Control Register (3CF.22) enables the 16-bit feature connector option.

NOTE When the feature connector option is enabled, the bus interface, wake-up port, and DRAM configuration pins are redefined as feature connector pins. MD15-MD8 are used instead to configure the bus interface, wake-up port, and DRAM configuration. See Table 2-1 for details.

Pin Name	Pin	Type	Description
GRDY/ RAMCNF	27	I/O	Graphics Ready Output Signal when the 16-bit feature connector interface is enabled. The GRDY signal indicates the graphics subsystem is ready to latch pixel data on P15-P0. The pin functions as the Color Key Window signal when the 8-bit feature connector interface is enabled. For this case, pin 27 is used in conjunction with the Color Key Overlay function to define a window for overlay. When the feature connector interface is disabled, this pin is used as DRAM configuration input signal RAMCNF.
INOSC/ DCLK	164	I/O	Pixel clock signal when the feature connector interface is enabled. DCLK is an output when ECLK is a logical 1. DCLK is an input when ECLK is a logical 0. When the feature connector interface is disabled, this pin is used as input clock signal INOSC (DRAM refresh clock for SUSPEND mode).
SDBUS16/ ECLK	132	I	Enable Clock signal when the feature connector interface is enabled. This signal controls the buffer direction of DCLK. When ECLK is a logical 1, DCLK is an output. When DCLK is a logical 0, DCLK is an input from the feature connector. When the feature connector interface is disabled, this pin is used as configuration input signal SDBUS16.
ID0/ESYNC	148	I	Enable Sync signal when the feature connector interface is enabled. This signal controls the buffer direction of VSYNC, HYSNC, and BLANK#. When ESYNC is a logical 1, VSYNC, HSYNC, and BLANK# are outputs. When ESYNC is a logical 0, BLANK# is an input from the feature connector. VSYNC and HSYNC will be tristated if genlock is disabled, or inputs if genlock is enabled. When the feature connector interface is disabled, this pin is used as configuration input signal ID0.
CPURST#/ EVIDEO	146	I/O	Enable Video signal when the feature connector interface is enabled. This signal controls the buffer direction of P7 - P0. When ECLK is a logical 1, P7-P0 are outputs. When EVIDEO is a logical 0, P7-P0 are inputs from the feature connector. EVIDEO is defined as an output when the Color Key overlay function is enabled. EVIDEO is defined as an input for all other cases. When the feature connector interface is disabled, this pin is used as input signal CPURST# for the VL-Bus.
HSYNC	162	I/TS/ O	Horizontal Sync. HSYNC is defined as an output when the feature connector interface is disabled. HSYNC may be an output, tristated, or an input when the feature connector interface is enabled. Signal ESYNC and the genlock state determine the direction of HSYNC. HSYNC is an output when signal ESYNC is a logical 1. HSYNC will tristate when ESYNC is a logical 0, and the sync from the feature connector will be used to drive the CRT. If genlock is enabled and ESYNC is a logical 0, HSYNC can be configured as an input and used to genlock the 92C178 to an external video source.
HVDDSEL/ BLANK#	149	I/O	Blank signal when the feature connector interface is enabled. BLANK# is an output when ESYNC is a logical 1. BLANK# is and input when ESYNC is a logical 0. When the feature connector interface is disabled, this pin is used as configuration input signal HVDDSEL.
MA9/P7	50	I/O	Pixel data bit 7 when feature connector interface enabled. P7 is an output when signal EVIDEO is a logical 1. P7 is an input when EVIDEO is a logical 0. When the feature connector interface is disabled, this pin is used as memory address bit 9 for asymmetric DRAM.

3.3.11 Feature Connector Interface (cont.)

NOTE MD31 must be set to a logical 1 at power-on in order to enable the feature connector interface. An 8-bit feature connector interface is supported for PCI bus and VL-Bus. A VAFC compatible 16-bit feature connector interface is supported for PCI bus. Bit 6 of the Extended Mode Control Register (3CF.22) enables the 16-bit feature connector option.

NOTE When the feature connector option is enabled, the bus interface, wake-up port, and DRAM configuration pins are redefined as feature connector pins. MD15-MD8 are used instead to configure the bus interface, wake-up port, and DRAM configuration. See Table 2-1 for details.

Pin Name	Pin	Type	Description
P6	102	I/O	Pixel data bit 6 when feature connector interface enabled. P6 is an output when signal EVIDEO is a logical 1. P6 is an input when EVIDEO is a logical 0. When the feature connector is interface is disabled, this pin is not used (VL-Bus and PCI bus).
LBS16#/P5	96	I/O	Pixel data bit 5 when feature connector interface enabled. P5 is an output when signal EVIDEO is a logical 1. P5 is an input when EVIDEO is a logical 0. When the feature connector interface is disabled, this pin is used as output signal LBS16# for the VL-Bus.
S46E8/P4	95	I/O	Pixel data bit 4 when feature connector interface enabled. P4 is an output when signal EVIDEO is a logical 1. P4 is an input when EVIDEO is a logical 0. When the feature connector interface is disabled, this pin is used as configuration input signal S46E8.
ATBUS#/P3	92	I/O	Pixel data bit 3 when feature connector interface enabled. P3 is an output when signal EVIDEO is a logical 1. P3 is an input when EVIDEO is a logical 0. When the feature connector interface is disabled, this pin is used as configuration input signal ATBUS#.
D/C#/P2	88	I/O	Pixel data bit 2 when feature connector interface enabled. P2 is an output when signal EVIDEO is a logical 1. P2 is an input when EVIDEO is a logical 0.
VL#/P1	87	I/O	Pixel data bit 1 when feature connector interface enabled. P1 is an output when signal EVIDEO is a logical 1. P1 is an input when EVIDEO is a logical 0. When the feature connector interface is disabled, this pin is used as configuration input signal VL#.
ID1/P0	85	I/O	Pixel data bit 0 when feature connector interface enabled. P0 is an output when signal EVIDEO is a logical 1. P0 is an input when EVIDEO is a logical 0. When the feature connector interface is disabled, this pin is used as configuration input signal ID1.
VSYNC	161	I/TS/O	Vertical Sync. VSYNC is defined as an output when the feature connector interface is disabled. VSYNC may be an output, tristated, or an input when the feature connector interface is enabled. Signal ESYNC and the genlock state determine the direction of VSYNC. VSYNC is an output when signal ESYNC is a logical 1. VSYNC will tristate when ESYNC is a logical 0, and the sync from the feature connector will be used to drive the CRT. If genlock is enabled and ESYNC is a logical 0, VSYNC can be configured as an input and used to genlock the 92C178 to an external video source.
BA7/P15-BA0/P0	62-65, 67-70	I/O	Pixel data bits 15-8 for the 16-bit feature connector option. This option is supported for PCI bus only. Bit 6 of the Extended Mode Control Register (3CF.22) enables this option. When the 16-bit feature connector option is disabled, these pins may be used as BIOS address bits 7-0 for PCI solutions which require a separate video ROM (e.g., add-on card solution). Tie MD30 to GND through a 4.7kΩ resistor to enable this option.

4.0 Bus Interface Unit

The OPTi 92C178 allows connection directly to the ISA bus, PCI Bus, VL-Bus, or 386 and 486 direct local bus. No external bus logic is required. The data bus may be up to 32-bits wide. Bus selection depends on the setting of the configuration pins as illustrated in Table 4-1.

Table 4-1 Bus Selection Configuration Pins

ATBUS# (92)	VL# (87)	ID0 (148)	ID1 (85)	Selected Bus
0	X	X	X	ISA Bus
1	1	0	0	PCI Bus
1	0	1	0	386 VL-Bus
1	0	0	1	486 VL-Bus
1	0	1	1	Reserved
1	1	1	0	386DX direct local bus
1	1	0	1	486SX/DX direct local bus
1	1	1	1	Reserved

The Bus Interface Unit provides decoding logic for both I/O and memory commands. The proper handshaking signals are provided to handle given bus protocols. The Bus Interface Unit also provides the necessary decoding logic and control signal EROM# to allow BIOS ROM accesses when the 92C178 is implemented as a plug-in peripheral.

For CPU read/writes of video memory, Segment Offset Register A (3CF.20) and Segment Offset Register B (3CF.21) can be used as Source and Destination respectively to speed CPU access to display memory. Linear addressing may also be implemented to eliminate bank switching overhead.

4.1 Write Buffer and Control

The Write Buffer queues CPU memory write commands which cannot be executed immediately because of memory bandwidth arbitration. The commands queued in the Write Buffer are executed as soon as display memory bandwidth is available. Once the address and the data of the CPU command is in the write buffer, the 92C178 immediately releases the CPU for ensuing cycles. The end result is maximized CPU bandwidth.

The Write Buffer data path is 32-bits wide. The depth can be programmed to zero, two, or four levels (bits 1, 0 of 3C5.14). The default value is four levels deep. The Write Buffer control logic allows packing of consecutive byte and word commands if the address of the commands are within a double word boundary.

4.2 Graphic Controller

The Graphic Controller manipulates the CPU data before it is sent to the display memory. The data path is 32-bits wide. For a write operation, the Graphic Controller performs data rotation, masking, and set/reset of the CPU data. Logical operations may also be performed using the CPU data and the data in the read latch. For a read operation, the Graphic Controller takes DRAM data from the read latch and either feeds the data directly back to the CPU, or performs a color compare operation before feeding the data back to CPU.

4.3 Memory Sequencer

The Memory Sequencer generates the timing for the display DRAM. The timing generated includes that for RAS, CAS, WE, OE, and multiplexed address. The memory clock which drives this logic is optimized for the speed of the DRAM used. The Memory Sequencer generates CAS- before-RAS refresh cycles, Random Read and Random Early Write cycles, Fast Page Read and Fast Page Early Write cycles. Multiple CAS or WEs are generated depending on the setting of RAMCNF (pin 27). A logical zero on this pin selects multiple CAS, while a logical one selects multiple WEs.

The Memory Sequencer allocates video memory bandwidth for the GUI engine, CPU access, screen refresh, DRAM refresh, hardware cursor access (if enabled), pop-up icon access (if enabled), and frame buffer access (if dual scan LCD panel is used) as follows:

The allocation between the GUI engine or CPU access and screen refresh is based on the status of the video FIFO. Priority is given to the screen refresh function.

DRAM refresh is allocated at the end of each scan line. At this allocated period, the 92C178 will generate CAS-before-RAS refresh cycles to ensure that the DRAM refresh timing requirement is meet. The number of CAS-before-RAS refresh cycles is selectable by bit 6 of the Vertical Sync End Register (3D5.11).

The hardware cursor and pop-up icon accesses are allocated at the beginning of any scan line in which the hardware cursor or pop-up icon appears. Depending on the size of the cursor or icon, the 92C178 will generate two (32X32X2) or four (64X64X2) page mode CAS cycles to fetch the cursor or icon pattern from the off screen area of the display RAM.

Frame buffer access is allocated at the end of each screen refresh period (during vertical blanking period) provided the frame buffer FIFO needs to be filled.

4.4 Video FIFO

The Video FIFO allows the Memory Sequencer to allocate cycles more efficiently and therefore to optimize CPU bandwidth. The Memory Sequencer fetches data from the display DRAM with fast page mode read cycles and loads the data to the Video FIFO. The data in the Video FIFO is then delivered to the Attribute Controller. The Video FIFO can be set to 4, 8, 12 or 16 levels by programming bits 5,4 of the Extended FIFO Control Register (3C5.13). A threshold value can be set as well by programming bits 2-0 of 3C5.13. The threshold can be from one level of empty to eight levels of empty. If the data in the Video FIFO is below the programmed threshold, then the screen refresh cycle takes priority over CPU access.

4.5 CRT Controller (CRTC)

The CRT Controller generates the horizontal sync and vertical sync for the CRT display monitor and provides a BLANK# signal to the integrated RAMDAC and feature connector. The CRT registers provides the flexibility to configure the horizontal and vertical timing, the text cursor position, the starting display address, split screen, screen horizontal panning, and other display related functions.

For flat panel display, there are shadow registers which can be configured to meet the fixed display timing requirements of the panel. The shadow registers are locked or unlocked by programming bit 5 of the CRTC External Control Register (3D5.33).

The CRTC also performs vertical expansion and auto centering for LCD panels. Vertical Expansion for 640x480 panels is enabled by programming bit 4 of the Panel Display Control Register (3D5.35) to a logical 1. For 1024x768 panels, bit 7 of the Starting Address Overflow Register (3D5.31) is also used to control vertical expansion. For VGA text mode, vertical expansion is performed by adding three blank scan lines between adjacent vertical rows or by using an 8x19 font with the bottom three pixel rows blank instead of the standard 8x16 font. For graphics modes, the Vertical Expansion Adjustment Register (3D5.38) may be used to define a scan line offset from which to start the double scan line pattern for vertical expansion.

Auto-centering is enabled by programming bit 5 of the Panel Display Control Register to a logical 1. Parameters to center the screen horizontally and vertically are programmed into the Horizontal Centering Adjustment Register (3D5.39) and the Vertical Centering Adjustment Register (3D5.3A), respectively.

4.6 Attribute Controller

The Attribute Controller takes video memory data from the Video FIFO and serializes it in accordance with the display mode structure (e.g. text, 4-bit/pixel, 8-bit/pixel, etc.). The video data, along with hardware cursor and pop-up icon data, is merged together and then routed to the RAMDAC. The Attribute Controller controls blinking and underline for text modes, and pixel panning for both graphic and text modes. For flat panel display, the Attribute Controller provides contrast enhancement for text modes and reverse video for both text and graphic modes.

4.7 GUI Engine

The 32-bit GUI Engine provides acceleration of those functions which most greatly enhance graphics performance in GUI environments, such as Microsoft Windows. Acceleration is supported for 8-bit, 15-bit, 16-bit, and 24-bit/pixel modes. Any graphics resolution up to 1280x1024 may be accelerated. A summary of the available GUI functions follows:

- BitBLT
- Color Expansion
- Fast Polygon Fill
- Area Fill
- Line Draw
- Short Stroke Vector Draw
- Rectangular Clipping
- Raster Operations

Programming the GUI Engine register set is facilitated by a one level deep Register Queue and Memory Mapped I/O registers. The Register Queue allows the complete set of GUI registers to be programmed for the next GUI operation without having to wait for the completion the current GUI operation. A status bit (bit 1 of the GUI Accelerator Status/Start Register - memory map location BF800h) indicates the state of the Register Queue. Memory Mapping the GUI Engine's I/O registers allows for faster programming of the 92C178's GUI Engine register set, since memory read/write operations can be used to access the registers instead of slower I/O read/write operations. Memory Mapped I/O is enabled by programming bit 7 of the Extended Mode Control Register (3CF.22) to a logical 1. Bits 3 and 2 of the Miscellaneous Register (3CF.06) must also be programmed to a logical 1 and a logical 0 respectively.

A short discussion of each of the GUI Engine functions follows:

4.7.1 BitBLT

Bit-Block transfer, or BitBLT, is among the most important of the GUI Engine functions. The BitBLT function is used to move blocks of graphics data from a source location in video memory or system memory to a specified destination in video memory or system memory. The direction of data transfer is determined by bits 7 (source) and 6 (destination) of the Bit-

BLT Mode Register - memory map location BF801h. A logical 1 for the given bit selects system memory. A logical 0 selects video memory. Raster operations between the source and destination data are supported.

A standard BitBLT function and an 8x8 Pattern BitBLT function are supported. Bit 2 of the BitBLT Mode Register controls the BitBLT function type. A logical 1 selects 8x8 Pattern BitBLT. Color data, Monochrome data, or a fixed color may be selected for each function. Bits 1 and 0 of the BitBLT Mode Register control this selection.

In Windows, BitBLT is most often used to perform SRCCOPY and PATCOPY. The direction of data transfer is typically from video memory to video memory, or from system memory to video memory.

4.7.2 Color Expansion

The Color Expansion function is used in cases where only a foreground color and a background color (for instance, black text on a white background) are required to fill a given display area. For these cases (e.g. BitBLTing from a monochrome source pattern), a single bit of data can be used to represent a given pixel on the screen. The bit is used as a lookup to a Foreground Color Register and a Background Color Register in the GUI Engine register set. The Foreground Color Register contains the 8, 16, or 24-bit foreground color to be filled. The Background Color Register contains the background color to be filled. If the given bit is a logical 1, the foreground color will be filled. If the given bit is a logical 0, the background color.

Transparency for Color Expansion is also supported. Bit 4 of the BitBLT mode register enables/disables the transparency effect. A logical 1 enables transparency. When transparency is enabled, the original background color of the destination is retained.

In Windows, Color Expansion is most often used to perform TextOut operations, where font data is transferred from system memory to video memory.

4.7.3 Fast Polygon Fill

Fast Polygon Fill is used to fill geometric shapes such as trapezoids, triangles, etc. This function makes use of a specialized scan line fill technique to fill the geometric shapes. The shapes may be filled with a solid color or a pattern (monochrome or color source pattern is supported). Source color selection is via bits 1 and 0 of the BitBLT mode register. Raster Operations between the source and destination data are supported.

4.7.4 Area Fill

The Area Fill function is used to fill an area in display memory (usually on the screen) with a fixed color. The color to be filled is programmed into the Foreground Color register. Raster Operations between the source and destination data are supported.

4.7.5 Line Draw

The Line Draw function is based on the Bresenham algorithm. This function may be used to draw a solid line (or lines) of any length/direction within the defined bitmap. The color to be used is programmed into the Foreground Color register. This function is especially useful in CAD programs (e.g. AutoCAD) where drawings are constructed using large numbers of vectors.

4.7.6 Short Stroke Vector Draw

The Short Stroke Vector Draw function is a specialized line draw function. This function may be used to draw solid lines of up to 16-pixels in length in one of eight directions (0, 45, 90, 135, 180, 225, 270, 315 degrees). Up to two Short Stroke Vectors may be drawn at once. The color to be used is programmed into the Foreground Color register.

In Windows, this function is useful for drawing the borders of geometric shapes (e.g. ellipses). This function is also very useful in MCAD applications, where large numbers of short, solid lines are often required to represent a given mechanical shape.

4.7.7 Rectangular Clipping

The Rectangular Clipping function is most easily described as a rectangular mask function. The rectangular area is defined by four registers; the Clip Left Register, Clip Right Register, Clip Top Register, and Clip Bottom Register. In Windows, Clipping is most useful for TextOut operations.

4.7.8 Raster Operations

The Raster Operations function facilitates the logical mixing of source and destination graphics data. The 92C178 supports 2ROPs, or 16 raster operation. Reference the Raster Operation Code Register - memory map location B8F02 for additional detail on available raster operations.

4.8 Hardware Cursor

The Hardware Cursor supports a 32X32X2 or a 64X64X2 user defined pattern. The cursor pattern is stored in the upper 1K or 2K of display memory. The Hardware Cursor operates for all standard VGA graphic and text modes, 4 bit per pixel extended graphics planar modes, and 8/16/24-bit per pixel packed-pixel modes.

The cursor pattern has 2-bits to represent a pixel. Each bit corresponds to a plane. Table 4-2 shows the cursor display state corresponding to the value of the cursor pattern.

Table 4-2 Cursor Display State

Cursor Plane 0	Cursor Plane 1	Cursor Display State
0	0	Cursor color 0
1	0	Cursor color 1
0	1	Transparent
1	1	Invert video data

The cursor position is defined relative to the cursor offset from the top-left corner of the display screen. The cursor position X is in pixels and it is specified by 3CF.23 for the lower eight bits and 3CF.24 for the remaining three higher order bits. The cursor position Y is in scan lines and it is specified by 3CF.25 for the lower eight bits and 3CF.26 for the remaining three higher order bits. The cursor offset is specified by the Hardware Cursor Y Origin Register (3CF.2E) and the Hardware Cursor X Origin Register (3CF.2F). The cursor position is changed only on VSYNC following a write to the cursor Y position registers.

For 32X32 cursor size, each cursor pattern requires 256 bytes. The cursor pattern is stored in the top 1K of display memory. Up to four cursor patterns may be loaded. The active cursor pattern is selected by programming the bits 3 and 2 of the Hardware Cursor Pattern Address Offset register (3CF.2D).

For 64X64 cursor size, each cursor pattern requires 1024 bytes. The cursor pattern is stored in the top 2K of display memory. Up to two cursor patterns may be loaded. The active cursor pattern is selected by programming bit 2 of 3CF.2D.

The cursor pattern data for cursor plane 0 and cursor plane 1 is loaded into display memory one cursor scan line at a time. For each cursor scan line, cursor plane 0 data is loaded first, followed by the cursor plane 1 data. This loading sequence continues until all 32/64 scanlines have been loaded into display memory. The cursor pattern is mapped to the display memory using linear packed-pixel addressing.

4.9 Pop-up Icon

The Pop-up Icon supports a 64X64X2 user defined pattern and it is expandable to 128X128. The Pop-up Icon is stored directly below the Hardware Cursor in an off-screen area of the display memory. The Pop-up Icon operates for all standard VGA graphic and text modes, 4 bit per pixel extended graphics planar modes, and 8/16/24-bit per pixel packed-pixel modes.

The pop-up icon has 2-bits to represent a pixel. Each bit corresponds to a plane. Table 4-3 shows the Pop-up Icon's display state corresponding to the value of the Pop-up-Icon pattern.

Table 4-3 Pop-Up Icon Display State

Pop-up Icon Plane 0	Pop-up Icon Plane 1	Pop-up Icon Display State
0	0	Pop-up icon color 0
1	0	Pop-up icon color 1
0	1	Transparent
1	1	Pop-up icon color 3

The Pop-up Icon's position is defined relative to the top-left corner of the display screen. The Pop-up Icon X position is defined in pixels and it is specified by register 3CF.30 for the lower eight bits and register 3CF.31 for the remaining higher order three bits. The Pop-up Icon Y position is defined in scan lines and it is specified by register 3CF.32 for the lower eight bits and register 3CF.33 for the remaining higher order three bits. The Pop-up Icon position is changed only on VSYNC following a write to the icon Y position registers.

The Pop-up Icon pattern requires 1024 bytes and is stored 2K from top of the display memory. When the Pop-up Icon is enabled, the cursor pattern can only be stored in the top 1K of the display memory. This means only one cursor pattern may be stored for a 64x64x2 Hardware Cursor.

The Pop-up Icon pattern data for pop-up icon plane 0 and pop-up icon plane 1 is loaded into display memory one scan line at a time. For each scan line, Pop-up Icon plane 0 data is loaded first, followed by the Pop-up Icon plane 1 data. The loading sequence continues until all 64 scanlines have been loaded into display memory. The Pop-up Icon pattern is mapped to the display memory using linear packed-pixel addressing.

Programming bit 1 of the Pop-up Icon Control Register to a logical 1 will allow the icon to be expanded to 128x128 size. This is accomplished by double scanning in the Y direction and duplicating each pixel in the X direction.

4.10 Frame Buffer Controller

The Frame Buffer Controller is used for dual scan LCD panels. The scan sequence for the dual scan panel requires that two scan lines be output to the display at a time; one for the upper panel and one for the lower panel. The CRTC controller fetches the video data from display memory sequentially, however. In order to display the video data for a dual scan panel correctly, a half-frame of the panel video data needs to be stored in a frame buffer. For the 92C178, the frame buffer is display memory.

The Frame Buffer Controller consists of two FIFOs. One is for frame buffer reads and the other is for frame buffer writes. Both frame buffers are 32-bits wide. Depth is selectable with bit 6 of the FIFO Control Register (3C5.13). The write frame buffer receives data from the Panel Data Control module and sends the data to an off-screen area of the display memory. The read frame buffer reads the data from the off-screen area of display memory and sends the data to the panel data control for display.

4.11 RAMDAC

The internal true color RAMDAC has a 24-bit wide pixel data port. This means that HiColor™ (5-5-5 format and 5-6-5 format) and true color modes (8-8-8 format) can be supported without having to double or triple the pixel clock rate. Three 8-bit D/A converters generate RS-343A compatible red, green, and blue video signals. The signal outputs can drive a doubly-terminated 75 ohm coax cable directly without the need for external buffers.

The RAMDAC has a VGA compatible triple 6-bit color lookup table (CLUT). The RAMDAC supports 4-bit/pixel modes, 8-bit pseudo color (256 colors) modes, and CLUT bypass versions of HiColor and true color modes. The palette DAC register I/O addresses and functionality are 100% compatible with the VGA standard.

Two external pins are used to control current in the RAMDAC. VREF (pin 154) connects to an external band-gap reference circuit which generates 1.22V to the RAMDAC. This voltage reference is used along with the resistor value on pin FADJ (pin 155) to set the full scale current output of the red, green, and blue Digital to Analog Converters (DACs). The desired resistor value may be determined by the following equation.

$$R = 7.7273 \times ((VREF) \div (IFULLSCALE))$$

To achieve a full scale reference current of 14mA, which will deliver 0.7V peak to peak on the RGB outputs, a 690ohm resistor is recommended.

Table 4-4 shows the resolutions and color depths supported by the internal RAMDAC.

Table 4-4 CRT Display Resolutions

Resolution	Text Mode	Number of Colors (Number of bits)				
		16 (4)	256 (8)	32K (16)	64K (16)	16M (24)
640 x 480			Yes	Yes	Yes	Yes
800 x 600		Yes	Yes	Yes	Yes	
1024 x 768		Yes	Yes	Yes	Yes	
1280x1024		Yes	Yes			
	132 col	Yes				

4.12 Dithering Engine

The dithering engine uses frame rate modulation and pattern dithering to generate up to 64 gray shades. A technique called Space Dithering is used to expand the 64 gray shades to 256 gray shades. Space Dithering uses specialized dithering patterns to achieve the additional gray shades. For color panels, the ability to display 256 shades of red, green and blue means true color images can be displayed (256^3 = 16M colors). Space Dithering can be enabled/disabled by programming bit 7 of the Panel Display Control Register (3D5.35). A logical 1 disables Space Dithering.

There is separate control for TFT panel dithering as well. Bit 6 of the Panel Display Control Register (3D5.35) may be used to enable/disable the TFT panel dithering. A logical 0 enables TFT dithering.

4.13 Flat Panel Interface Controller

The Flat Panel Interface Controller takes data from the RAMDAC's color palette lookup table or from the attribute controller and converts the color information to monochrome by using the NTSC algorithm for monochrome panels (Y = 0.3R + 0.59G + 0.11B). For color panels, the NTSC conversion is skipped. The R, G, and B data or the converted NTSC data then passes through a MUX to select one of the 256 gray shades for R, G, and B intensity for a color panel or gray intensity for a monochrome panel. After passing through the MUX, the pixel data become 3-bits per pixel for a color panel or 1-bit per pixel for a monochrome panel. The pixel data is then formatted in accordance to the particular panel being used. The formatted data is then output to the flat panel for display. For a dual scan panel, half of the panel data is sent to the frame buffer via the Frame Buffer FIFO.

The Flat Panel Interface Controller also generates the neces-

sary control signals for the panel interface. The First Line Marker signal (FLM) is used to indicate the beginning of a frame. The polarity of this signal is controlled by bit 2 of the Flat Panel Output Control Register (3D5.36). A logical 0 selects positive polarity. The Line Pulse signal (LP) tells the panel to latch data into the current scan line for display. Signal polarity is controlled by bit 1 of the Flat Panel Output Control Register (3D5.36). A logical 0 selects positive polarity. The Shift Clock (SCLK) is used to shift panel data into the panel's shift register. For color TFT panels, the Data Enable signal (DTMG) is used to indicate the beginning valid panel data. The Frame Rate signal (M) is used by some panels to properly sync panel data. M may be programmed to toggle every frame or every programmed number of scan lines. Bits 7-0 of the Flat Panel FR Timing Adjustment Register (3D5.3C) are used to control the signal toggling.

4.13.1 LCD Panel Types and Resolutions

Table 4-5 and Table 4-6 show the panel types that are supported by the Flat Panel Interface Controller.

Table 4-5 Color Panel Types

Panel Type	640x480	800x600	1024x768
Single Panel, Single Drive STN Color Panel (8-bit & 16-bit data interfaces)	256 colors (8-bit pixel) 32K or 64K colors (16-bit pixel) 16M colors (24-bit pixel)		
Dual Panel, Dual Drive STN Color Panel (8-bit & 16-bit data interfaces)	256 colors (8-bit pixel) 32K or 64K colors (16-bit pixel) 16M colors (24-bit pixel)	256 colors (8-bit pixel) 32K or 64K colors (16-bit pixel)*	
Single Panel, Serial Data TFT Color Panel (3-bit, 9-bit, 12-bit & 18-bit data interfaces)	256 colors (8-bit pixel) 32K or 64K colors (16-bit pixel) 16M colors (24-bit pixel)	256 colors (8-bit pixel) 32K or 64K colors (16-bit pixel)	256 colors (8-bit pixel) 32K or 64K colors (16-bit pixel)[a]

a. 2MB DRAM required.

Table 4-6 Monochrome Panel Types

Panel Type	640x480	1024x768
Dual Panel, Dual Drive STN Mono Panel (8-bit data interface)	64 shades or 256 shades	64 shades
Single Panel, Single Drive STN Mono Panel (4-bit & 8-bit data interfaces)	64 shades or 256 shades	64 shades

4.13.2 Expansion

The 92C178 supports expansion of standard VGA text and graphics modes to fill 640x480 and 800x600 panels. Bit 4 of the Panel Display Control Register (3D5.35) controls vertical expansion for 640x480 panels. A logical 1 enables vertical expansion. Bits 2-0 of the 800x600 Expansion Register (3D5.24) control expansion for 800x600 panels. Bits 2 and 0 control horizontal expansion as follows:

Bit 2	Bit 0	Function
0	0	Disables horizontal expansion
0	1	Enables Horizontal expansion. Replicate every 4th pixel.
1	0	Reserved
1	1	Horizontal expansion for VGA text modes. Force 10-dot text mode for 8 or 9-dot text.

Bit 1 controls vertical expansion (a logical 1 enables vertical expansion). A logical 1 enables vertical expansion.

Modes are expanded in the following manner for 640x480 panels:

Mode	Vertical Expansion Technique
640x200 graphics	Double scanned and every 5th line replicated - total 480 lines

Mode	Vertical Expansion Technique
640x350 graphics	Replicate 1st two lines and last 3 lines of each 14 line set - total 475 lines
640x400 graphics	Replicate every 5th line - total 480 lines
400 line text	Three blank lines inserted between each character row - total 475 lines Alternatively, an 8x19 font can be used - total 475 lines

Modes are expanded in the following manner for 800x600 panels

Mode	Expansion Technique
640x200 graphics	Replicate every 4th pixel horizontally - total 800 pixels Triple scan each line - total 600 lines
640x350 graphics	Replicate every 4th pixel horizontally - total 800 pixels Replicate every other line - total 525 lines
640x400 graphics	Replicate every 4th pixel horizontally - total 800 pixels Replicate every other line - total 600 lines
400 line text (9-dot)	Replicate the 9th pixel of each character - total 800 pixels Replicate every other line - total 600 lines
400 line text (8-dot)	Triplicate the 8th pixel of each character - total 800 pixels Replicate every other line - total 600 lines

4.14 Power Management Unit

The Power Management Unit generates the power-up and power-down sequencing control for the panel. The power sequencing is used to maximize panel lifetime. During the power-up sequence, panel VDD power is turned on first. The panel control and data signals are then activated. Finally, the panel VEE power is turned on. During the power-down sequence, the panel VEE power is turned off first. Next, the control and data signals are deactivated. Lastly, panel VDD power is turned off.

The Power Management Unit supports three level of power down modes. They are described as follows:

- *Panel Backlight ON/OFF*
  The panel backlight is turned off when there is no keyboard, mouse, or VGA (video memory access or I/O access to the graphics controller) activity for a specified period. The period is determined by programming an internal counter timer. Bit 7 of the Power Down Backlight Timeout Register (3D5.46) is used to enable the counter timer. A logical 1 enables the timer. Bits 4-0 of 3D5.46 set the counter timer starting value. The programmable range is 0 - 31 minutes in one minute increments. Panel backlight power is restored upon detection of keyboard, mouse, or VGA activity.

- *Standby Mode*
  The Standby Mode can be invoked via a hardware control pin, by software programming a register bit, or by using a dedicated internal counter timer. Programming bit 2 of the Power Down Control Register (3D5.44) enables the hardware power-down method. When signal STANDBY (pin 171) is toggled to the enable Standby Mode state, the 92C178 immediately enters the Standby Mode. The polarity of the STANDBY pin is programmable. Bit 4 of the Power Down Clock Select Register (3D5.47) determines polarity. A logical 0 selects positive polarity. Toggling STANDBY to its standard operation state will cause the 92C178 to resume normal operations.

  Software register control of the Standby Mode is accomplished by programming bit 0 of 3D5.44. Setting this bit to a logical 1 will cause the 92C178 to immediately enter Standby Mode. Programming the bit back to a logical 0 will cause the 92C178 to resume normal operations.

  For the counter timer method, Standby Mode is invoked when there is no keyboard, mouse, or VGA (video memory access or I/O access to the graphics controller) activity for a period determined by the internal counter timer. Bit 7 of the Power Down Standby Timeout Register (3D5.45) is used to enable the counter timer. A logical 1 enables the timer. Bits 4-0 of 3D5.45 set the counter timer starting value. The programmable range is 0 - 31 minutes in one minute increments. Standard power-on operations resume upon detection of keyboard, mouse, or VGA activity.

  While in Standby Mode, the video clock is turned off. CPU activity is maintained. The memory clock can be reduced to minimize power consumption by programming bits 1 and 0 of the Power Down Refresh Control Register (3D5.47). The memory clock can be divided by 1, 2, 4, or 8. Register data is retained by the power supply. Table 4-7 shows a summary of the state of each of the 92C178's interfaces during Standby Mode.

Table 4-7 Standby Mode Interface States

Interface	Pin State Description
CRT	R, G, B, HSYNC, VSYNC set for DPMS Standby.

Interface	Pin State Description
LCD Panel	Panel control pins (FLM, LP, DTMG, M, and SCK) and panel data pins (TFTD17, TFTD16, UD7 - UD0, and LD7 - LD0) are driven low and then tristated.
DRAM	All pins active.
Host Bus	All pins active.
Power Management	Pins ACTIVITY, SUSPEND, STANDBY are active
Clock Synthesizer	XCLK input active (VCK shut off inside chip).

- *Suspend Mode*

  The Suspend Mode can be invoked via a hardware control pin or by software programming a register bit. Programming bit 3 of the Power Down Control Register (3D5.44) enables the hardware power-down method. When signal SUSPEND (pin 173) is toggled to the enable Suspend Mode state, the 92C178 immediately enters the Suspend Mode. The polarity of the SUSPEND pin is programmable. Bit 5 of the Power Down Clock Select Register (3D5.47) determines polarity. A logical 0 selects positive polarity. Toggling SUSPEND to its standard operation state will cause the 92C178 to resume normal operations.

  Software register control of the Suspend Mode is accomplished by programming bit 1 of 3D5.44. Setting this bit to a logical 1 will cause the 92C178 to immediately enter Suspend Mode. Programming the bit back to a logical 0 will cause the 92C178 to resume normal operations.

  For suspend mode, both the video clock and memory clock are turned off. DRAM contents are retained by separate clock that provides a 32KHz memory refresh clock. The 32KHz clock source may be a direct input from a 32KHz oscillator, or may be derived from the 14.318MHz motherboard system clock. Register data is retained by the power supply.

  Table 4-8 shows the state of each of the 92C178's interfaces during software invoked Suspend Mode.

Table 4-8 Software Suspend Mode Interface States

Interface	Pin State Description
CRT	R, G, B, HSYNC, VSYNC set for DPMS Suspend.
LCD Panel	Panel control pins (FLM, LP, DTMG, M, and SCK) and panel data pins (TFTD17, TFTD16, UD7 - UD0, and LD7 - LD0) are driven low and then tristated.
DRAM	Signals RAS#, CAS# are active (CAS before RAS refresh cycles). MD31 - MD0 are configured as inputs only. MA8 - MA0 are frozen at last address before power down invoked. OE# retains its last state before Suspend Mode invoked. WE# is held at a logical 1.
Host Bus	Data bits are configured as inputs only. Only IO writes are allowed. Since no memory writes are performed during Suspend Mode, output signal ZWS# is driven to its inactive state.
Power Management	Pins ACTIVITY, SUSPEND, STANDBY are active
Clock Synthesizer	XCLK input active if used to generate DRAM refresh clock (when feature connector enabled). INOSC input active if used to generate DRAM refresh clock (when feature connector disabled).

Table 4-9 shows the state of each of the 92C178's interfaces during hardware invoked Suspend Mode.

Table 4-9 Hardware Suspend Mode Interface States

Interface	Pin State Description
CRT	R,G,B, HSYNC, VSYNC is set for DPMS Suspend.
LCD Panel	Panel control pins (FLM, LP, DTMG, M, and SCK) and panel data pins (TFTD17, TFTD16, UD7 - UD0, and LD7 - LD0) are driven low and then tristated.
DRAM	Signals RAS#, CAS# are active (CAS before RAS refresh cycles). MD31 - MD0 are configured as inputs only. MA8 - MA0 are frozen at last address before power down invoked. OE# retains its last state before Suspend Mode invoked. WE# is held at a logical 1.

Interface	Pin State Description
Host Bus	All host interface outputs tristated. All host interface inputs inactive. Suspend Mode must be resumed by toggling SUSPEND pin.
Power Management	Pins ACTIVITY, SUSPEND, STANDBY are active
Clock Synthesizer	XCLK input active if used to generate DRAM refresh clock (feature connector enabled). INOSC input active when used to generate DRAM refresh clock (feature connector disabled).

- *Deep Sleep Mode*
  Deep Sleep Mode is selected by programming bit 6 of the Power Down Control register (3D5.44) to a logical 1. Toggling the SUSPEND input then enables Deep Sleep Mode. In Deep Sleep Mode, all power can be removed from the chip except for MVDD. MVDD is needed to keep the Power Management Logic and CAS# before RAS# DRAM refresh logic active. The 92C178 register contents should be saved to disk. Only the power management interface (pins ACTIVITY, SUSPEND, STANDBY) and the DRAM refresh logic (INOSC, CAS#, RAS#) are active during Deep Sleep Mode. The DRAM refresh logic can be turned off for DRAM which supports self refresh. Toggling SUSPEND to its standard operation state will cause the 92C178 to exit from Deep Sleep Mode.

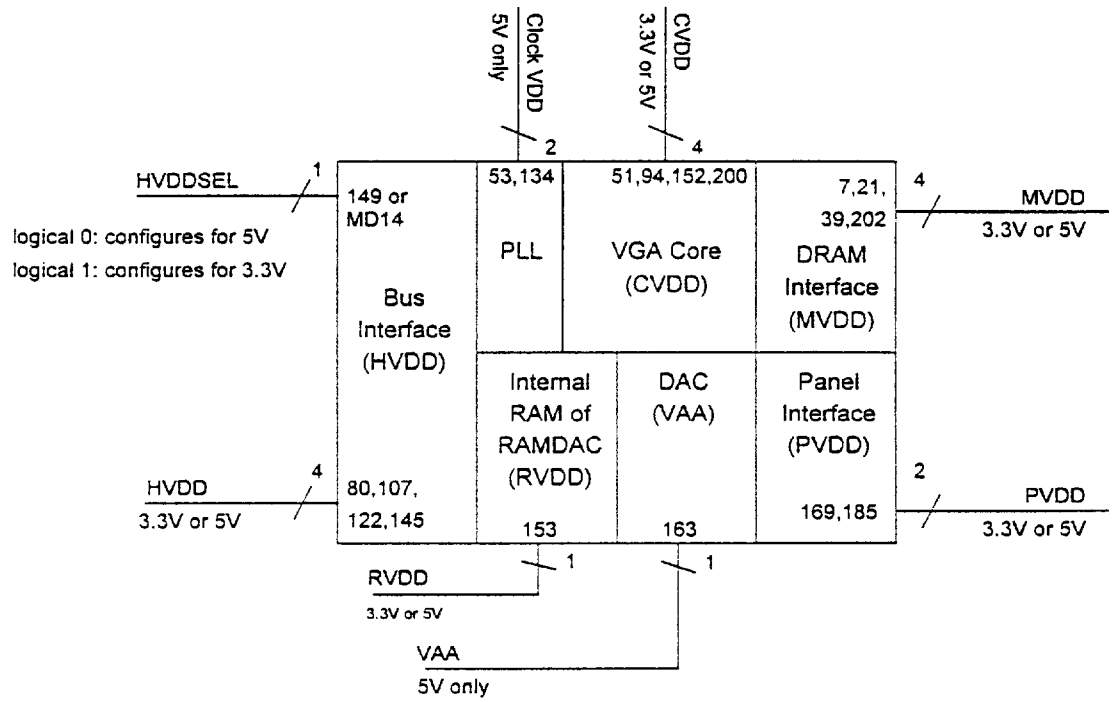
4.15 Power Distribution Module

Digital power is applied separately to six different areas in the 92C178. These areas are the VGA core (Memory Sequencer, CRT Controller, Graphics Controller, and Attribute Controller), the Bus Interface Unit, the Panel Interface Controller, the DRAM interface, and the internal RAM of the RAMDAC and the color synthesizer. The RAMDAC voltage must be the same as the VGA core. The clock synthesizer voltage must be 5V. With the exception of these, any mixed combination of +3.3V or +5V power can be separately applied to these modules. For the Bus Interface Unit, signal HVDDSEL is used to select the voltage. A logical 1 selects 3.3V. A logical 0 selects 5V. For the DRAM interface, bit 1 of the Mixed Voltage Selection Register (3D5.23) must be set to a logical 1 when 3.3V is applied. For the Panel Interface Controller, bit 0 3D5.23 must be set to a logical 1 when 3.3V is applied.

4.16 Clock Synthesizer

The clock synthesizer module provides video clock and a memory clock. The video clock may be selected from one of four programmable video clock groups. Each group is individually programmable from 25MHz to 100MHz. The memory clock is programmable from 30MHz to 80MHz. All frequencies are derived from a 14.318MHz input (XCLK-pin 151).

Figure 4-1 Power Rail Block Diagram



4.17 Multimedia Module

The Multimedia Module provides Feature Connector support, Genlock to an external video source, Overlay capabilities, and a mode switching RAMDAC.

4.17.1 Feature Connector

The 92C178 provides support for an 8-bit VAFC compatible 16-bit feature connector interface. 8-bit feature connector support is provided for VL-bus solutions and PCI solutions. 16-bit support is provided for PCI solutions.

For 8-bit solutions, data from the feature connector may be clocked in at the rising edge of each DCLK, or at the rising and falling edges of each DCLK. Clocking is controlled by bits 4:2 of the Overlay Control Register (3CF.40). When these bits select 15-bit or 16-bit RGB color as the data format for the feature connector input data, data is automatically clocked in at the rising edge (low-byte) and falling edge (high byte) of DCLK.

The 16-bit feature connector option offers VAFC baseline function compatibility as well as some additional overlay options (Section 4.17.3, Overlay). To enable the 16-bit feature connector solution for PCI, set bit 6 of the Extended Mode Control Register to a logical 1.

4.17.2 Genlock

To support video overlay on a pixel by pixel basis, the video data from the feature connector must be synchronized with the graphics data from the 92C178. This synchronization is defined as "Genlock". To accomplish this, the 92C178 can be configured to input VSYNC, HSYNC, or both VSYNC and HSYNC from the feature connector. The sync information is then used to synchronize the graphics data frame with the incoming video data frame. This method for synchronizing the two data frames is intended for configurations where the pixel clock from the remote video source is the same as the pixel clock from the graphics controller.

The Genlock function is controlled by the Genlock Control register (3CF.4B). Bit 7 enables/disables VSYNC Genlock. Bit 6 enables/disables HSYNC Genlock. In both cases, a logical 1 enables Genlock for the given sync signal.

4.17.3 Overlay

Three types of overlay are supported:

1. **Pass-Through Overlay**
   The entire display frame is replaced with video data from the feature connector. To accomplish this, the ESYNC, EVIDEO, and ECLK inputs are pulled low and remain low. The graphics data from display memory is ignored. Genlock is not required for Pass-Through Overlay.
2. **Overlay using EVIDEO**
   The video source from the feature connector controls overlay on a pixel by pixel basis. When given pixel(s) from display memory are to be overlaid with video data from the feature connector, EVIDEO is pulled low by the remote video source. The pixel in display memory is then replaced with the video pixel from the feature connector. EVIDEO can be toggled on a pixel by pixel basis. This function is selected by programming bits 1 and 0 of the Overlay Control register (3CF.40) to a logical 0 and a logical 1 respectively.
3. Overlay with Color Key:
   a. **Full Screen Overlay with Color Key**
      The 92C178 controls overlay on a pixel by pixel basis. For this case, EVIDEO is configured as an output. When the color key condition is met (e.g. pixel data = color key value), the 92C178 drives EVIDEO low. The pixel in display memory is then replaced with the video pixel from the feature connector. EVIDEO can be toggled on a pixel by pixel basis. This function is selected by programming both bits 1 and 0 of the Overlay Control register (3CF.40) to a logical 1.
   b. **Overlay with Color Key in a Window**
      This overlay function operates in the same manner as Full Screen Overlay with Color Key, except that the Color Key is used only within a localized window. The window is defined by six overlay window registers within the 92C178, which define the horizontal start and end and the vertical start and end of the window. If the display update location is within the defined window and if the color key condition is met, output signal GRDY is driven high. GRDY should be connected to EVIDEO through an inverter, so EVIDEO will be driven low. The pixel in display memory is then replaced with the video pixel from the feature connector. GRDY can be toggled on a pixel by pixel basis. This function is selected by programming bits 1 and 0 of the Overlay Control register (3CF.40) to a logical 1 and a logical 0 respectively.

For all overlay types, the video data stream must be applied at all times, even when video data from the feature connector is being ignored. Some form of genlock is required (e.g., external video device genlocks video and graphics data or 92C178 genlocks video and graphics data) for Overlay using EVIDEO and Overlay with a Color Key.

4.17.4 RAMDAC

The internal RAMDAC of the 92C178 allows mode switching between the overlay window and the surrounding graphics screen. This means that the overlay window color depth can be set independently of the color depth of the surrounding graphics. For instance, the overlay window could be at 16-bits/pixel while the surrounding graphics is at 8-bits/pixel. To invoke DAC mode switching, program bit 5 of the Overlay Control Register (3CF.40) to a logical 1, then use bits 4-2 of the same register to indicate the color mode of the feature connector input data.

5.0 Register Description

This section describes the OPTi 92C178 register set. The standard VGA core registers are listed in table format. For detailed bit level information on the VGA core registers, please reference one of the many available VGA programmer's reference guides. A recommended VGA programming reference book is the Programmer's Guide to the EGA and VGA Cards (Second Edition) by Richard M. Ferraro. The book is published by Addison-Wesley.

A table listing and bit level detail are provided for the 92C178's extended register set.

5.1 VGA Register Port Map

Table 5-1 VGA Register Port Map

Address	Port
3C0h	Attribute Controller write
3C1h	Attribute Controller read
3C2h	Miscellaneous Output (write)/Input Status Register 0 (read)
3C3h	Video Subsystem Enable
3C4h	Sequencer Index
3C5h	Sequencer Data
3C6h	DAC Pixel Mask
3C7h	Pixel Address Read Mode (write)/DAC State (read)
3C8h	Pixel Mask Write
3C9h	Pixel Data
3CEh	Graphics Controller Index
3CFh	Graphics Controller Data
3x4h[1]	CRT Controller Address
3x5h[1]	CRT Controller Data
3xAh[1]	Feature Control (write)/Input Status Register 1 (read)
46E8h	Video Subsystem Enable

1. "x" = D for color modes and B for monochrome modes.

5.2 Standard VGA Register Tables

Table 5-2 VGA General Registers

Register Name	Address	Index
Miscellaneous Output	3CCh = read port 3C2h = write port	–
Input Status Register 0	3C2h = read port	–
Input Status Register 1	3xAh = read port	–
Feature Control Register	3CAh = read port 3xAh = write port	–
Video Subsystem Enable	3C3h	–
Video Subsystem Enable	46E8h	–

Table 5-3 VGA Sequencer Registers

Register Name	Address	Index
Sequencer Index	3C4h	–
Reset	3C5h	00h
Clocking Mode	3C5h	01h
Plane Mask	3C5h	02h
Character Map Select	3C5h	03h
Memory Mode	3C5h	04h

Table 5-4 CRTC Registers

Register Name	Address	Index
CRTC Index	3x4h	–
Horizontal Total	3x5h	00h
Horizontal Display End	3x5h	01h
Horizontal Blanking Start	3x5h	02h
Horizontal Blanking End	3x5h	03h
Horizontal Sync Start	3x5h	04h
Horizontal Sync End	3x5h	05h
Vertical Total	3x5h	06h
Overflow	3x5h	07h
Screen Preset Row Scan	3x5h	08h
Maximum Scan Line	3x5h	09h
Cursor Start	3x5h	0Ah
Cursor End	3x5h	0Bh
Start Address High	3x5h	0Ch
Start Address Low	3x5h	0Dh
Cursor Location High	3x5h	0Eh
Cursor Location Low	3x5h	0Fh

Table 5-4 CRTC Registers (cont.)

Register Name	Address	Index
Vertical Sync Start	3x5h	10h
Vertical Sync End	3x5h	11h
Vertical Display End	3x5h	12h
Offset	3x5h	13h
Underline Location	3x5h	14h
Vertical Blanking Start	3x5h	15h
Vertical Blanking End	3x5h	16h
Mode Control	3x5h	17h
Line Compare	3x5h	18h

Table 5-5 Graphics Controller Registers

Register Name	Address	Index
Graphics Controller Index	3CEh	--
Set/Reset	3CFh	00h
Set/Reset Enable	3CFh	01h
Color Compare	3CFh	02h
Data Rotate	3CFh	03h
Read Map Select	3CFh	04h
Mode	3CFh	05h
Miscellaneous	3CFh	06h
Color Don't Care	3CFh	07h
Bit Mask	3CFh	08h

Table 5-6 Attribute Controller Registers

Register Name	Address	Index
Attribute Controller Index	3C0h write/ 3C1h read	--
Color Palette Registers	3C0h write/ 3C1h read	00h -Fh
Mode Control	3C0h write/ 3C1h read	10h
Overscan Color	3C0h write/ 3C1h read	11h
Color Plane Enable	3C0h write/ 3C1h read	12h
Horizontal Pixel Panning	3C0h write/ 3C1h read	13h
Color Select	3C0h write/ 3C1h read	14h

Table 5-7 OPTi GUI Engine Registers

Register Name	Address	Index
Status/Start Register	X3C4h	00h
BitBLT Mode	X3C4h	01h
BitBLT Raster Operation	X3C4h	02h
Display Configuration	X3C4h	03h
Source Start X/Diagonal Step Constant	X3C4h	04h
Source Start Y/Axial Step Constant	X3C4h	06h
Destination Start X	X3C4h	08h
Destination Start Y	X3C4h	0Ah
BitBLT Width	X3C4h	0Ch
BitBLT Height	X3C4h	0Eh
Short Stroke Vector	X3C4h	10h
Error Term	X3C4h	12h
Source Pitch and Base Address Offset	X3C4h	14h
Foreground Color	X3C4h	18h
Background Color	X3C4h	1Ch
Clip Left	X3C4h	20h
Clip Right	X3C4h	22h
Clip Top	X3C4h	24h
Clip Bottom	X3C4h	26h

Table 5-8 92C178 Extended Registers

Register Name	Address	Index
Unlock Extended Registers	3C5h	10h
Extended Mode Control	3C5h	11h
Extended Clock Select	3C5h	12h
Video FIFO Control	3C5h	13h
Write Buffer Control	3C5h	14h
Extended Miscellaneous Control	3C5h	15h
System Interface Control	3C5h	16h
Miscellaneous Pin Control	3C5h	17h
Configuration Register 0	3C5h	1Dh
Configuration Register 1	3C5h	1Eh
Configuration Register 2	3C5h	1Fh
Configuration Register 3	3C5h	2Eh
Offset A	3CFh	20h
Offset B	3CFh	21h

Table 5-8 92C178 Extended Registers (cont.)

Register Name	Address	Index
Extended Mode Control	3CFh	22h
Hardware Cursor X Position Low	3CFh	23h
Hardware Cursor X Position High	3CFh	24h
Hardware Cursor Y Position Low	3CFh	25h
Hardware Cursor Y Position High	3CFh	26h
Hardware Cursor Color Register 0	3CFh	27h-29h
Hardware Cursor Color Register 1	3CFh	2Ah-2Ch
Hardware Cursor Pattern Address Offset	3CFh	
Hardware Cursor Y Origin	3CFh	2Eh
Hardware Cursor X Origin	3CFh	2Fh
Pop-up Icon X Position Low	3CFh	30h
Pop-up Icon Y Position High	3CFh	31h
Pop-up Icon Y Position Low	3CFh	32h
Pop-up Icon Y Position High	3CFh	33h
Pop-up Icon Color Register 0	3CFh	34h-36h
Pop-up Icon Color Register 1	3CFh	37h-39h
Pop-up Icon Color Register 1	3CFh	3Ah-3Ch
Pop-up Icon Control	3CFh	3Dh
Scratch Pad Registers	3x5h	1Dh,1Eh
Mixed Voltage Selection	3x5h	23h
Device ID Registers	3x5h	28h, 29h
Extended Overflow	3x5h	30h
Starting Address Overflow	3x5h	31h
Interlaced Horizontal Retrace	3x5h	32h
Extended CRTC Control	3x5h	33h
Panel Select	3x5h	34h
Panel Display Control	3x5h	35h
Panel Output Control	3x5h	36h
FLM Adjustment	3x5h	37h

Table 5-8 92C178 Extended Registers (cont.)

Register Name	Address	Index
Vertical Expansion Adjustment	3x5h	38h
Horizontal Centering Adjustment	3x5h	39h
Vertical Centering Adjustment	3x5h	3Ah
Horizontal Centering for 1024x768 Panel	3x5h	3Bh
Modulation Adjustment	3x5h	3Ch
Power Down Control	3x5h	44h
Standby Mode Timeout	3x5h	45h
Power Down Backlight Timeout	3x5h	46h
Power Down Clock Select	3x5h	47h
Power Down Refresh Control	3x5h	48h

Table 5-9 Internal RAMDAC Registers

Register Name	Address	Index
Pixel Mask	3C6h	–
Pixel Address Read Mode	3C7h (for write)	–
DAC State	3C7h (for read)	–
Pixel Address Write Mode	3C8h	–
Pixel Data	3C9h	–

Table 5-10 Clock Synthesizer Registers

Register Name	Address	Index
Video Clock Group 0 (VCK0) Input Frequency Divider	3C4h	20h
Video Clock Group 0 (VCK0) VCO Frequency Divider	3C4h	21h
Video Clock 1 (VCK1) Input Frequency Divider	3C4h	22h
Video Clock Group 1 (VCK1) VCO Frequency Divider	3C4h	23h
Video Clock 2 (VCK2) Input Frequency Divider	3C4h	24h
Video Clock Group 2 (VCK2) VCO Frequency Divider	3C4h	25h
Video Clock 3 (VCK3) Input Frequency Divider	3C4h	26h

Table 5-10 Clock Synthesizer Registers (cont.)

Register Name	Address	Index
Video Clock Group 3 (VCK3) VCO Frequency Divider	3C4h	27h
Memory Clock Input Frequency Divider	3C4h	28h
Memory Clock VCO Frequency Divider	3C4h	29h

Table 5-11 Overlay Control Registers

Register Name	Address	Index
Overlay Control	3CFh	40h
Color Key Register 0	3CFh	41h
Color Key Mask Register 0	3CFh	43h
Overlay Window Horizontal Start	3CFh	45h
Overlay Window Horizontal End	3CFh	46h
Overly Window Horizontal Pixel Alignment	3CFh	47h
Overlay Window Vertical Start	3CFh	48h
Overlay Window Vertical End	3CFh	49h
Overlay Window Vertical Overflow	3CFh	4Ah
Genlock Control	3CFh	4Bh

Table 5-12 CRTC Shadow Registers

Register Name	Address	Index
Miscellaneous Output Register	3C2h	–
Horizontal Total for single dot modes[a]	3x5h	00h
Horizontal Total for double dot modes.[b]	3x5h	01h
Horizontal Blanking Start	3x5h	02h
Horizontal Blanking End	3x5h	03h
Horizontal Sync Start	3x5h	04h
Horizontal Sync End	3x5h	05h
Vertical Total	3x5h	06h
Overflow (bits 0, 2, 3, 5, 7 shadowed)	3x5h	07h
Maximum Scan Line (bit 5 shadowed)	3x5h	09h

Table 5-12 CRTC Shadow Registers (cont.)

Register Name	Address	Index
Vertical Sync Start	3x5h	10h
Vertical Sync End (bits 3-0 shadowed)	3x5h	11h
Vertical Blanking Start	3x5h	15h
Vertical Blanking End	3x5h	16h

a. Display End hardwired to 4Fh.
b. Display End hardwired to 27h.

Additional Notes for Shadow Registers:

1. Bit 5 of the Panel Output Control Registers allows selection of 1or multiple sets of shadow registers. A logical 1 selects 3 sets. See Note 4 for additional details.
2. If multiple shadow register sets are selected, 3D5.02 - 3D5.05 are shadowed for all panel resolutions.
3. If a single set of shadow registers is selected, 3D5.02 - 3D5.05 are only shadowed for 1024x768 panels.
4. If multiple shadow register sets are selected, two sets of 3D5.02 - 3D5.05 will be available, one set of 3C2 will be available, and three sets of the remaining shadow registers will be available.
5. See Panel Output Control Register for additional details.

Table 5-13 PCI Configuration Space Registers

Register Name	Byte Location in Configuration Space Header
Device ID	02h - 03h
Vendor ID	00h - 01h
Command	04h - 05h
Status	06h - 07h
Revision	08h
Class Code	09h - 0Bh
Cache Line Size	0Ch
Latency Timer	0Dh
Header Type	0Eh
BIST	0Fh
Base Address	10h - 27h
Expansion ROM Base Address	30h - 33h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Min_Gnt	3Eh
Max_Lat	3Fh

5.3 92C178 GUI Engine Register Set

The 92C178 GUI engine register set may be accessed via the standard I/O port method or as a memory mapped I/O block. To access the GUI register set via the standard I/O method, use X3C0h as the 16-bit index port and X3C4 as the 32-bit data port. "X" may be any value for PCI configurations. For ISA and VL-Bus configurations "X" is hardwired to value Fh.

To access the GUI register set as a memory mapped I/O block, set bit 7 of the Extended Mode Control Register (3CF.22) to a logical 1 and bits 3, 2 of the Miscellaneous Register (3CF.06) to 0, 1 respectively.

The memory map location for the GUI registers is B8F00h - B8F24h. 8-bit, 16-bit and 32-bit write cycles are supported.

Table 5-14 is a diagram of the memory mapped I/O register structure.

Table 5-14 Memory Mapped I/O Register Structure

Port	31:24	23:16	15:8	7:0
B8F00	Display Configuration	BitBLT Raster	BitBLT Mode	GUI Engine Status Start
B8F04	Source Start Y/Axial Step Constant		Source Start X/Diagonal Step Constant	
B8F08	Destination Start Y		Destination Start X	
B8F0C	BitBLT Height		BitBLT Width/Short Stroke Vector	
B8F10	Error Term/Source Pitch			
B8F14				
B8F18		Foreground Color		
B8F1C		Background Color		
B8F20	Clip Right		Clip Left	
B8F24	Clip Bottom		Clip Top	

5.3.1 GUI Engine Status/Start Register

I/O Port: X3C4h

Index: Write value 00h to index port location X3C0h

Memory Map Location: B8F00h

Bits	Function
7-5	Function Select
4	X Direction Select
3	Y Direction Select
2	CPU Write Enable Status
1	GUI Engine Register Queue Status
0	GUI Engine Busy

Bit 7 - 5: GUI Engine Function Select. The operation will start when the given function is selected. Be sure all applicable registers are programmed before selecting the GUI function type. Bits 7-5 select GUI engine functions as follows:

7	6	5	Function Selected
1	1	1	No operation
0	0	1	BitBLT
0	1	0	Fast Polygon Fill
0	1	1	Short Stroke Vector Draw
1	0	0	Line Draw (Bressenham algorithm)

For standard programming, a write to these register bits engages the engine to perform the selected function. A Quick Start feature is also available. This feature is enabled by programming bit 7 of the Display Configuration Register. With the Quick Start feature enabled, a write to the BitBLT Width Register will engage the engine to perform the function currently selected by bits 7-5 of this register. The Quick Start feature is most useful for Fast Polygon Fill operations.

Bit 4: X Direction Select. This bit selects the horizontal direction of the selected BitBLT operation.
Logical 1: Selects bottom to top.
Logical 0: Selects top to bottom (default).

Bit 3: Y Direction Select. This bit selects the vertical direction of the selected BitBLT operation.
Logical 1: Selects bottom to top.
Logical 0: Selects top to bottom (default).
Note BitBLT directions other than the default are useful for cases of overlapping Source and Destination.

Bit 2: CPU Write Enable Status. This bit is intended to provide CPU write status for memory to screen operations, particularly color expansion. This bit is read only.
Logical 1: Indicates the CPU will need to wait before the next write command to display memory.
Logical 0: Indicates 92C178 is ready to accept a host write.

Bit 1: GUI Engine Register Queue Status. All GUI Engine registers may be queued with the exception of this register. This bit is read only.
Logical 1: Indicates the GUI Engine Register Queue is empty.
Logical 0: Indicates the GUI Engine Register Queue is full.

Bit 0: GUI Engine Busy. This bit is read only.
Logical 1: Indicates GUI engine is busy.
Logical 0: Indicates GUI engine is idle.

5.3.2 BitBLT Mode Register

I/O Port: X3C4h

Index: Write value 01h to index port location X3C0h

Memory Map Location: B8F01h

Bits	Function
7	BitBLT Source Select
6	BitBLT Destination Select
5	Enable Clipping
4	Enable Monochrome Transparency
3	Enable Source Pitch
2	Enable 8x8 Pattern BitBLT
1,0	Source Map Color Selection

Bit 7: BitBLT Source Select.
Logical 1: Selects system memory as the source for the BitBLT operation.
Logical 0: Selects display memory as the source for the BitBLT operation.

Bit 6: BitBLT Destination Select.
Logical 1: Selects system memory as the destination for the BitBLT operation.
Logical 0: Selects display memory as the destination for the BitBLT operation.
Note Screen to Screen and Memory to Screen operations are fully supported. Screen to Memory operations are supported for SRCOPY only. Memory to Memory operations are not supported.

Bit 5: Enable Clipping.
Logical 1: Enables the Rectangular Clipping function. Registers X3C4.20 (Clip Left Register), X3C4.22 (Clip Right Register), X3C4.24 (Clip Top Register), X3C4.26 (Clip Bottom Register) determine the boundary area for clipping.
Logical 0: Disables the Rectangular Clipping function.

Bit 4: Enable Monochrome Transparency.
Logical 1: Enables monochrome transparency. This feature is intended for use with a monochrome source. When monochrome transparency is enabled, only the foreground color of the monochrome source is filled at the destination. The original destination background color is maintained.
Logical 0: Disables monochrome transparency.

Bit 3: Enable Source Pitch.
Logical 1: Enables source pitch. The source pitch is defined as the number of pixels locations from a pixel on a given row to the same pixel location in the next row. Enable this bit to address the BitBLT area in a linear fashion. Bits 14-3 of X3C4.12 set the source pitch. This selection is intended for TextOut functions which involve font caching.
Logical 0: Disables source pitch. Use X/Y addressing.

Bit 2: Enable 8x8 Pattern BLT.
Logical 1: Enables 8x8 pattern BLT. At the start of a BLT operation, an 8x8 color or monochrome source pattern is read from display memory. This pattern is repeatedly filled to the selected destination.
Logical 0: Disables 8x8 pattern BLT. Use pixel by pixel BLT operation.

Bits 1,0: Source Map Color Selection for BitBLT and Fast Polygon Fill Operations.

1	0	Source Map
0	0	Color
0	1	Monochrome (e.g. for Color Expansion). Color is determined by the Foreground and Background Color Registers.
1	0	Fixed Color (e.g. for Area Fill). Color is determined by the Foreground Color Register.
1	1	Reserved

5.3.3 BitBLT Raster Operation Register

I/O Port: X3C4h

Index: Write value 02h to index port location X3C0h

Memory Map Location: B8F02h

Bits	Function
7	Clipping Type
6	Reserved
5	Last Pixel Off
4	Major Axis
3-0	Raster Operation Select

Bit 7: Clipping Type. Selects whether the clipping function is performed inside or outside the clipping rectangle.
Logical 1: The clipping function is performed outside the clipping rectangle (standard clipping).
Logical 0: The clipping function is performed inside the clipping rectangle.

Bit 6: Reserved.

Bit 5: Last Pixel Off.
Logical 1: Selects last pixel off for line draw operations. Set this bit for Polyline applications.
Logical 0: Selects last pixel on for line draw operations. Use this setting for stand-alone lines.

Bit 4: Major Axis Select.
Logical 1: Indicates the Y-axis is the major axis for line draw.
Logical 0: Indicates the X-axis is the major axis for line draw.

Bits 3-0: Raster Operation Select. Sixteen two-operand raster operations are supported.

Bit 3	2	1	0	Raster Operation (Microsoft Designation)	Boolean Equation
0	0	0	0	Blackness	0
0	0	0	1	NOTSRCERASE	~(S+D)
0	0	1	0	–	~S*D
0	0	1	1	NOTSRCCOPY	~S
0	1	0	0	SRCERASE	~D*S
0	1	0	1	DSTINVERT	~D
0	1	1	0	SRCINVERT	~(S+D)
0	1	1	1	–	~(S*D)
1	0	0	0	SRCAND	S+D
1	0	0	1	–	S=D
1	0	1	0	–	D
1	0	1	1	MERGEPAINT	~S+D
1	1	0	0	SRCCOPY	S
1	1	0	1	–	S+~D
1	1	1	0	SRCPAINT	S+D
1	1	1	1	Whiteness	1

5.3.4 Display Configuration Register

I/O Port: X3C4h

Index: Write value 03h to index port location X3C0h. This register is used when the Source Pitch bit (bit 3) in the BitBLT Mode Register is disabled.

Memory Map Location: B8F03h

Bits	Function
7	Enable Quick Start
6, 5	Data Width Write to GUI Engine
4-2	X Resolution
1,0	Pixel Depth

Bit 7: Enable Quick Start.
Logical 1: Enables Quick Start feature.
Logical 0: Disables Quick Start feature.

Bits 6,5: Data Width Write to GUI Engine. These bits are typically used for color expansion operations.

7	6	Data Width for GUI Engine Write
0	0	1 Byte
0	1	2 Bytes
1	0	4 Bytes
1	1	Reserved

Bits 4-2: X Resolution. Indicates X resolution of the current graphics display mode. The value is used to convert X/Y pixel addressing to linear pixel addressing.

4	3	2	X Resolution
0	0	0	640 pixels
0	0	1	800 pixels
0	1	0	1024 pixels
0	1	1	1280 pixels
1	0	0	1600 pixels
1	0	1	2048 pixels
1	1	0	Reserved
1	1	1	Reserved

Bits 1,0: Pixel Depth. Indicates pixel depth of current graphics display mode. The value is used to convert X/Y pixel addressing to linear pixel addressing.

1	0	Pixel Depth (bits/pixel)
0	0	Reserved
0	1	8
1	0	16
1	1	24

5.3.5 Source Start X/Diagonal Step Constant Register

I/O Port: X3C4h

Index: Write value 04h to index port location X3C0h

Memory Map Location: B8F04h

Bits	Function
15-(12)	Reserved
(14) 11-0	Source Start X Coordinate

Bits 15-(12): Reserved. Bit 15 is reserved when source is monochrome. Bits 15-12 are reserved when source is color

Bits (14)11-0: Source Start X Coordinate. Source start X coordinate for X/Y pixel addressing. Bits 14-0 are used when the source is monochrome. Bits 11-0 are used when the source is color.

Note If the Source Pitch bit (X3C4.01h bit 3) is set, bits 15-12 are reserved. Bits 11-3 are the lower nine bits of the source start linear address within the 2MB display memory space. Bits 2-0 represent the pixel position within one byte of the linear address.

When performing line draws which use the Bresenham algorithm, this register is defined as the Diagonal Step Constant Register. For the line draw case, bits 15 and 14 are reserved, and bits 13-0 contain the diagonal step constant value K2. The value K2 is determined in software by the following equation:

$$K2 = 2 * (min(|dx|, |dy|) - max(|dx|, |dy|))$$

5.3.6 Source Start Y/Axial Step Constant Register

I/O Port: X3C4h

Index: Write value 06h to index port location X3C0h

Memory Map Location: B8F06h

Bits	Function
15-(12)	Reserved
(14) 11-0	Source Start Y Coordinate/K1

Bits 15-(12): Reserved. Bit 15 is reserved when source is monochrome. Bits 15-12 are reserved when source is color.

Bits (14)11-0: Source Start Y Coordinate. Source start Y coordinate for X/Y pixel addressing. Bits 14-0 are used when the source is monochrome. Bits 11-0 are used when the source is color.

Note If the Source Pitch bit (X3C4.01h bit 3) is set, bits 11-0 are the upper 12 bits of the source start linear address.

When performing line draw using the Bresenham algorithm, this register is defined as the Axial Step Constant Register. For the line draw case, bits 15 and 14 are reserved, and bits 13-0 contain the axial step constant value K1. The value K1 is determined in software by the following equation:
K1 = 2 * (min (|dx | , | dy |))

5.3.7 Destination Start X Register

I/O Port: X3C4h

Index: Write value 08h to index port location X3C0h

Memory Map Location: B8F08h

Bits	Function
15-12	Reserved
11-0	Destination Start X Coordinate

Bits 15-12: Reserved.

Bits 11-0: Destination Start X Coordinate. Specifies destination X coordinate for a BitBLT or Fast Polygon Fill operation.

5.3.8 Destination Start Y Register

I/O Port: X3C4h

Index: Write value 0Ah to index port location X3C0h

Memory Map Location: B8F0Ah

Bits	Function
15-12	Reserved
11-0	Destination Start Y Coordinate

Bits 15-12: Reserved.

Bits 11-0: Destination Start Y Coordinate. Specifies destination Y coordinate for a BitBLT or Fast Polygon Fill operation.

5.3.9 BitBLT Width/Short Stroke Register

I/O Port: X3C4h

Index: Write value 0Ch to index port location X3C0h.

Memory Map Location: B8F0Ch

BitBLT Width Case

Bits	Function
15-12	Reserved
11-0	BitBLT Width

Bits 15-12: Reserved.

Bits 11-0: BitBLT Width. Value programmed is width of BitBLT operation - 1.
When the Quick Start feature is enabled, a write to this register will engage the GUI engine to perform the function currently programmed into bit 7-5 of the GUI Engine Status/Start Register.

Short Stroke Vector Case

Bits	Function
15-13	Drawing Direction for Short Stroke Vector 0
12	Draw or Move for Short Stroke Vector 0
11-8	Pixel Length of Short Stroke Vector 0
7-5	Drawing Direction for Short Stroke Vector 1
4	Draw or Move for Short Stroke Vector 1
3-0	Pixel Length of Short Stroke Vector 1

Bits 15-13: Drawing Direction for Short Stroke Vector 0. Selects one of eight octants as follows:

Bit 15	14	13	Drawing Direction (degrees)
0	0	0	0
0	0	1	45
0	1	0	90
0	1	1	135
1	0	0	180
1	0	1	225
1	1	0	270
1	1	1	315

Bit 12: Draw or Move for Short Stroke Vector 0. This bit may be used to draw a patterned short stroke vector.
Logical 1: Draw pixel. The color is determined by the value in the Foreground Color Register.
Logical 0: Move to next pixel location but do not draw pixel.

Bits 11-8: Pixel Length of Short Stroke Vector 0. The value programed equals the pixel length of the vector - 1.

Bits 7-5: Drawing Direction for Short Stroke Vector 1. Selects one of eight octants as follows:

Bit 7	6	5	Drawing Direction (degrees)
0	0	0	0
0	0	1	45
0	1	0	90
0	1	1	135
1	0	0	180
1	0	1	225
1	1	0	270
1	1	1	315

Bit 4: Draw or Move for Short Stroke Vector 1. This bit may be used to draw a patterned short stroke vector.
Logical 1: Draw pixel. The color is determined by the value in the Foreground Color Register.
Logical 0: Move to next pixel location but do not draw pixel.

Bits 3-0: Pixel Length of Short Stroke Vector 1. The value programed equals the pixel length of the vector - 1.
Short Stroke Vector 0 is always drawn first.

5.3.10 BitBLT Height Register

I/O Port: X3C4h

Index: Write value 0Eh to index port location X3C0h

Memory Map Location: B8F0Eh

Bits	Function
15-12	Reserved
11-0	BitBLT Height

Bits 15-12: Reserved.

Bits 11-0: BitBLT Height. Value programmed is height of BitBLT operation - 1.

5.3.11 Error Term/Source Pitch Register

I/O Port: X3C4h

Index: Write value 12h to index port location X3C0h

Memory Map Location: B8F12h

Error Term Case (for Bresenham Line Draw)

Bits	Function
15, 14	Reserved
13-0	Error Term

Bits 15, 14: Reserved.

Bits 13-0: Error Term. The value programmed specifies the error term for a Bressenham Line Draw operation. The equation for determining the value follows:

For starting X location of the line < ending X location of the line -
*Error Term=2 * min (|dx | , | dy |) - max (| dx | , | dy |) - 1*
For starting X location of the line >= ending X location of the line -
*Error Term=2 * min (|dx | , | dy |) - max (| dx | , | dy |)*

Source Pitch Case (for BitBLT operations)

Bits	Function
15	Reserved
14-3	Source Pitch
2-0	Reserved

Bit 15: Reserved.

Bits 14-3: Source Pitch. Specifies the number of pixel locations from any pixel in a given row to the same pixel location in the next row. This value is used when Source Pitch operation is enabled. Bit 3 of X3C4.01 (BitBLT Mode Register) enables Source Pitch operation.

Bits 2-0: Reserved.

5.3.12 Foreground Color Register

I/O Port: X3C4h

Index: Write value 18h to index port location X3C0h

Memory Map Location: B8F18h

Bits	Function
31-24	Reserved
23-0	Foreground Color

Bits 31-24: Reserved.

Bits 23-0: Foreground Color. The color value may be up to 24-bits. This color value may be used for Color Expansion, Area Fill, or Line Draw functions. For the color expansion case, a logical 1 from the monochrome source bitmap selects a foreground color fill. For Area Fill, the foreground color value is used to fill the given area. For Line Draw functions (Bressenham and Short Stroke), the foreground color value determines the color of the line.

5.3.13 Background Color Register

I/O Port: X3C4h

Index: Write value 1Ch to index port location X3C0h

Memory Map Location: B8F1Ch

Bits	Function
31-24	Reserved
23-0	Background Color

Bits 31-24: Reserved.

Bits 23-0: Background Color. The color value may be up to 24-bits. This color value is used for Color Expansion. A logical 0 from the monochrome source bitmap selects a background color fill.

5.3.14 Clip Left Register

I/O Port: X3C4h

Index: Write value 20h to index port location X3C0h

Memory Map Location: B8F20h

Bits	Function
15-12	Reserved
11-0	Clip Left Location

Bits 15-12: Reserved.

Bits 11-0: Clip Left Location. The value programmed specifies the left edge of the clipping rectangle. When Clipping is enabled, any part of the BitBLT operation beyond the left edge of the specified clipping rectangle will be masked off. Clipping is enabled by programming bit 5 of X3C4.01 (BitBLT Mode Register) to a logical 1.

5.3.15 Clip Right Register

I/O Port: X3C4h

Index: Write value 22h to index port location X3C0h

Memory Map Location: B8F22h

Bits	Function
15-12	Reserved
11-0	Clip Right Location

Bits 15-12: Reserved.

Bits 11-0: Clip Right Location. The value programmed specifies the right edge of the clipping rectangle. When Clipping is enabled, any part of the BitBLT operation beyond the right edge of the specified clipping rectangle will be masked off. Clipping is enabled by programming bit 5 of X3C4.01 (BitBLT Mode Register) to a logical 1.

5.3.16 Clip Top Register

I/O Port: X3C4h

Index: Write value 24h to index port location X3C0h

Memory Map Location: B8F24h

Bits	Function
15-12	Reserved
11-0	Clip Top Location

Bits 15-12: Reserved.

Bits 11-0: Clip Top Location. The value programmed specifies the top edge of the clipping rectangle. When Clipping is enabled, any part of the BitBLT operation above the top of the specified clipping rectangle will be masked off. Clipping is enabled by programming bit 5 of X3C4.01 (BitBLT Mode Register) to a logical 1.

5.3.17 Clip Bottom Register

I/O Port: X3C4h

Index: Write value 26h to index port location X3C0h

Memory Map Location: B8F26h

Bits	Function
15-12	Reserved
11-0	Clip Bottom Location

Bits 15-12: Reserved.

Bits 11-0: Clip Top Location. The value programmed specifies the bottom edge of the clipping rectangle. When Clipping is enabled, any part of the BitBLT operation below the bottom of the specified clipping rectangle will be masked off. Clipping is enabled by programming bit 5 of X3C4.01 (BitBLT Mode Register) to a logical 1.

5.4 92C178 Extended Registers

The following is a detailed description of the 92C178's extended register set. The power-on default for all extended registers (with the exception of the Device ID Registers, 3D5.28 and 3D5.29) is 0h.

5.4.1 Unlock Extended Registers Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 10h to Sequencer Address Register location 3C4.

Bits	Function
7-0	Lock/Unlock the Extended Registers

Bits 7-0: Lock/Unlock Extended Registers. A value of XXXX1010 written to this register will unlock all OPTi 92C178 extended registers. Any other value written to this register will lock the extended registers. When the extended registers are locked, the value read back from this register is always 0Fh.

5.4.2 Extended Mode Control Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 11h to Sequencer Address Register location 3C4.

Bits	Function
7, 6	Reserved
5	Divide INVCK by 3
4	Divide INVCK by 2
3	Select 32K or 64K Color Mode
2	Select True Color Mode
1	Select 15/16-Bit Per Pixel Mode
0	Select Extended 256-Color Mode

Bits 7, 6: Reserved.

Bit 5: Divide VCK by 3. Set to a logical 1 for true color modes. The Sequencer divides VCK by 3. The divided clock is then sent to the internal RAMDAC as the pixel clock.

Bit 4: Divide VCK by 2. Set to a logical 1 for 15/16-bit per pixel modes. The Sequencer divides VCK by 2. The divided clock is then sent to the internal RAMDAC as the pixel clock.

Bit 3: Select 32K or 64K Color Mode.
Logical 1: Selects 5-6-5 version of HiColor mode.
Logical 0: Selects 5-5-5 version of HiColor mode.

Bit 2: Select True Color Mode. Set this bit to a logical 1 to select true color mode.

Bit 1: Select 15/16-Bit Per Pixel Mode. Set this bit to a logical 1 to select HiColor mode.

Bit 0: Select Extended 256-Color Mode. Set this bit to a logical 1 to select and extended 256 color mode (e.g. 640x480, 800x600, 1024x768).

5.4.3 Clock Select Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 12h to Sequencer Address Register location 3C4.

Bits	Function
7	Enable Interlaced Mode
6, 5	Reserved
4	Do Not Allow Divide by 2 for INVCK
3	Divide INMCK by 2
2	Divide INVCK by 2
1	Select Internal/External Clock
0	IOVCK1 and IOVCK2 Direction Select

Bit 7: Enable Interlaced Mode
Logical 1: Enables interlaced mode.
Logical 0: Enables non-interlaced mode.

Note Bit 3 of the Starting Address Overflow Register (3D5.31) must also be set to a logical 1 to enable interlaced mode.

Bits 6, 5: Reserved

Bit 4: Do not allow divide by two for INVCK.
Logical 1: Do not allow INVCK to be divided by 2. This bit overrides bit 3 of the Clocking Mode Register (3C5.01).
Logical 0: Allow division of INVCK by two. Bit 3 of register 3C5.01 can be used to divide INVCK by two.
The setting of this bit has no effect on bit 2 of this register.

Bit 3: Divide INMCK by two.
Logical 1: Divide INMCK by two.
Logical 0: Do not divide INMCK by two.

Bit 2: Divide INVCK by two.
Logical 1: Divide INVCK by two.
Logical 0: Do not divide INVCK by two.

Bit 1: Select Internal/External Clock.
Logical 1: Selects Internal Clock. All other bits in this register are not used of the internal clock is selected.
Logical 2: Selects External Clock.

Bit 0: IOVCK1 and IOVCK2 Direction Select.
Logical 1: Defines IOVCK1 and IOVCK2 as clock select output pins 2 and 3 to the external clock chip. The logical level output for these signals is programmed by setting bits 6 and 5 respectively of this register.
Logical 0: Defines IOVCK1 and IOVCK2 as video clock inputs 2 and 3 to the 92C178. Video clock input 1 is IOVCK0. For this case, video clock selection is determined by bits 3 and 2 of the Miscellaneous Output Register (3C2).

5.4.4 FIFO Control Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 13h to Sequencer Address Register location 3C4.

Bits	Function
7	Reserved
6	Select Frame Buffer FIFO Depth
5, 4	Video FIFO Depth Select
3	Reserved
2-0	Video FIFO Threshold

Bit 7: Reserved.

Bit 6: Select Frame Buffer FIFO Depth. The Frame Buffer FIFO is used for STN dual scan panels.
Logical 1: Selects 8 levels.
Logical 0: Selects 6 levels.

Bits 5, 4: Video FIFO Depth Select. Video FIFO depth is dependent upon mode selection.

5	4	Levels
0	0	16
0	1	12
1	0	8
1	1	4

Bit 3: Reserved.

Bits 2-0 Video FIFO Threshold Select. When the number of empty levels in the Video FIFO is greater than or equal to the programmed threshold value, then the Video FIFO must be filled above the threshold before CPU access requests from the Write Buffer can be processed.

5.4.5 Write Buffer Control Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 14h to Sequencer Address Register location 3C4.

Bits	Function
7-5	Reserved
4	Tristate Control for DRAM Interface Pins
3	Screen Refresh Bandwidth Select
2	Reserved
1, 0	Select Write Buffer Depth

Bits 7-5: Reserved. Bits 7 and 6 are logical 0. Bit 5 is a logical 1.

Bit 4: Tristate Control for DRAM Interface Pins. This bit can be used for board testing.
Logical 1: Tristate RAS#, CAS#, WE#, OE#, and MA9-MA0.
Logical 0: Standard DRAM interface signal operations.

Bit 3: Screen Refresh Bandwidth Select.
Logical 1: Enables a video FIFO operation request to terminate a CPU access cycle.
Logical 0: Standard bandwidth allocation operations.

Bit 2: Reserved.

Bits 1, 0: Select Write Buffer Depth.

1	0	Levels
0	0	4
0	1	Reserved
1	0	2
1	1	0

5.4.6 Extended Miscellaneous Control Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 15h to Sequencer Address Register location 3C4.

Bits	Function
7, 6	Linear Address Window Location
5	DRAM Interface
4	Wrap-Around
3	Frame Buffer FIFO
2	2MB DRAM
1	Select Asymmetric DRAM
0	INMCK Frequency Greater than 45MHz

Bits 7, 6: Linear Address Window Location. These bits along with bits 3-0 of 3C5.16 select the location of the linear address window.

Bit 5: DRAM Interface. Set this bit to a logical 1 to support a 32-bit DRAM interface (eight 256Kx4 or two 256Kx16 DRAMs).
Set this bit to a logical 0 to support a 16-bit DRAM interface.

Bit 4: Wrap-Around.
Logical 1: Use this setting for modes that require more than 256K of memory.
Logical 0: Wrap around to start of display memory after 256K.

Bit 3: Frame Buffer FIFO.
The FIFO is used to support dual scan LCD panels. With the Frame Buffer FIFO enabled, data from the LCD panel is stored in the video frame buffer. Simultaneous display for a CRT and a dual scan LCD panel can thus be supported.
Logical 1: Selects full-frame storage for Frame Buffer FIFO.
Logical 0: Selects half-frame storage for Frame Buffer FIFO (default).

Bit 2: 2MB DRAM. Set this bit to a logical 1 to support 2MB of DRAM.

Bit 1: Select Asymmetric DRAM.
Logical 1: Selects asymmetric DRAM support. MA9-MA0 used to address the DRAM.
Logical 0: Selects standard DRAM support. MA8-MA0 used to address the DRAM.

Bit 0: INMCK Frequency Greater than 45MHz. Set this bit to a logical 1 when the frequency of INMCK is greater than 45MHz.

5.4.7 Extended System Interface Control Register

Read/Write Port: 3C5

Index: This register is accessed by writing a value of 16h to Sequencer Address Register location 3C4.

Bits	Function
7	Palette Snooping
6	8/16-Bit ISA Memory Read/Write
5	Enable 32-Bit Pipelining
4	16-Bit Local Bus Interface
3-0	Linear Address Window Location

Bit 7: Palette Snooping.
Logical 1: Enables palette snooping for VL-Bus.
Logical 0: Disables palette snooping for VL-Bus.

Bit 6: 8/16-Bit ISA Memory Read/Write.
Logical 0: Forces 8-bit memory access cycles on ISA bus. This setting is useful for dual monitor configurations (e.g. monochrome card in same system as 92C178).
Logical 1: 16-bit memory cycles on ISA bus.

Bit 5: Enable 32-Bit Pipelining.
Logical 1: Enables i386 write command pipeline support.
Logical 0: Disables i386 write command pipeline support.

Bit 4: 16-Bit Local Bus Interface
Logical 1: Configures the 92C178 for 16-bit local bus interface (e.g. for 386SX)
Logical 0: Configures the 92C178 for 32-bit local bus interface (e.g. 386DX, 486SX/DX)

Bits 3-0: Linear Address Window Location.
These bits, along with bit 7,6 of 3C5.15, are used to select the location of the linear address window. Allowable values are 1h-Fh (2nd to 64th MB). The value 0h (default setting) disables linear addressing.
The standard VGA address space (A000-BFFF) is still valid when linear addressing is turned on. This allows selective use of linear addressing with device drivers.

5.4.8 Extended Miscellaneous Control Register 2

Read/Write Port: 3C5h

Index: This register is accessed by writing a value of 17h to Sequencer Address location 3C4h.

Bits	Function
7	Test Clock
6	Feature Connector Enable
5	GRDY Enable
4	Reserved
3	Enable DPMS
2	CAS Precharge Adjust
1,0	CPU Bus Cycle Adjustment

Bit 7: Test Clock.
Logical 1: VCLK and MCLK output on signals TFT16 and TFT17.
Logical 0: TFT16 and TFT17 retain their standard signal definitions.

Bit 6: Feature Connector Enable.
Logical 1: Enables Feature Connector.
Logical 0: Disables Feature Connector.
Feature Connector pin definitions backward compatible to the 92C168.

Bit 5: GRDY Enable.
Logical 1: Enables GRDY output (pin 27). This signal is used to define an overlay window area for 8-bit feature connector and as VAFC signal GRDY for 16-bit feature connector.
Logical 0: Disables GRDY output (pin 27)

Bit 4: Reserved.

Bit 3: Enable DPMS (Display Power Management Signaling).
Logical 1: Enables DPMS. DPMS will be invoked when Standby or Suspend power down modes are enabled.
Logical 0: Disables DPMS.

Bit 2: CAS Precharge Adjust.
Logical 1: Set CAS precharge pulse to two MCLK cycles.
Logical 0: Set CAS precharge pulse to one MCLK cycle.

Bits 1.0: CPU Bus Cycle Adjustment.

1	0	MCLK Cycles
0	0	Standard I/O and Memory Cycles (default).
0	1	Reduce I/O and Memory Cycles by the value of 1MCLK
1	0	Reduce I/O and Memory Cycles by the value 2 MCLKs
1	1	Reduce I/O and Memory Cycles by the value 3 MCLKs

5.4.9 Configuration Register 0 (read only)

Read Port: 3C5

Index: This register is accessed by writing a value of 1Dh to Sequencer Address Register location 3C4.

Bits	Function
7	Dual CAS# or Dual WE# DRAM Configuration
6	VGA Enable Port
5	Bus Size
4	ISA/Local Bus Interface
3	VESA/General Local Bus Interface
2, 1	Bus Interface ID
0	Reserved

Bit 7: Dual CAS# or Dual WE# DRAM Configuration. When the feature connector is disabled, this bit reflects the value of RAMCNF (pin 27) at power-on.
Logical 1: Dual WE# DRAM Configuration (for 256Kx16 dual WE# or 256Kx4 DRAM)
Logical 0: Dual CAS# DRAM Configuration (for 256Kx16 dual CAS# DRAM)

Bit 6: VGA Enable Port. When the feature connector is disabled, this bit reflects the value of S46E8 (pin 95) at power-on.
Logical 1: 46E8 is VGA enable port.
Logical 0: 3C3 is VGA enable port.

Bit 5: Bus Size. When the feature connector is disabled, this bit reflects the value of SDBUS16 (pin 132) at power-on.
Logical 1: 16-Bit data bus (for ISA or 386SX local bus)
Logical 0: 32-Bit data bus (for 386/486 local bus).

Bit 4: ISA/Local Bus Interface. When the feature connector is disabled, this pin reflects the value of ATBUS# (pin 92) at power-on.
Logical 1: Local Bus.
Logical 0: ISA Bus.

Bit 3: VESA/General Local Bus Interface. When the feature connector is disabled, this bit reflects the value of VL# (pin 87) at power-on.
Logical 1: General local bus interface.
Logical 0: VESA local bus interface (VL-Bus).

Bits 2, 1: Bus Interface ID. When the feature connector is disabled, these bits reflect the value of ID1 (pin 85) and ID0 (pin 148) at power-on.

2	1	Bus ID
0	0	PCI Bus
0	1	386 VL-Bus
1	0	486 VL-Bus
1	1	Reserved

Bit 0: Reserved.

5.4.10 Configuration Register 1 (read only)

Read Port: 3C5

Index: This register is accessed by writing a value of 1Eh to Sequencer Address Register location 3C4. Bits 7-0 of this register correspond to MD23-MD16 respectively at power-up. BIOS reads these values at power-up and configures the appropriate extended registers for the selected panel.

Bits	Function
7	Indicate 3.3V/5V Memory Interface
6	Select Single/Dual Scan
5, 4	Select Panel Data Interface Width

3	Select TFT/STN Panel
2	Select 1024x768 Panel
1, 0	Select Number of Line Pulses Per Frame

Bit 7: Indicate 3.3V/5V Memory Interface.
Logical 1: 3.3V.
Logical 0: 5V.

Bit 6: Select Single/Dual Scan.
Logical 1: Selects single scan panel.
Logical 0: Selects dual scan panel.

Bits 5, 4: Select Panel Data Interface Width.

5	4	For STN	For TFT
0	0	mono 4 -bit (single) mono 8-bit (dual)	9-bit
0	1	mono 8-bit (single)	12-bit
1	0	color 8-bit	3-bit
1	1	color 16-bit	18-bit

Bit 3: Select TFT/STN Panel.
Logical 1: Selects TFT panel.
Logical 0: Selects STN panel.

Bit 2: Select 1024x768 panel.
Logical 1: Selects 1024x768 panel
Logical 0: Selects 640x480 panel.

Bits 1, 0: Select Number of Line Pulses Per Frame. This setting applies to dual scan STN panels.

1	0	Line Pulses Per Frame
0	0	240
0	1	242
1	0	244
1	1	Reserved

5.4.11 Configuration Register 2 (read only)

Read Port: 3C5

Index: This register is accessed by writing a value of 1Fh to Sequencer Address Register location 3C4. Bits 7-0 of this register correspond to MD31-MD24 respectively at power-up. BIOS reads these values at power-up and configures the Mixed Voltage Register (3D5.23) for the selected voltage.

Bits	Function
7	Enable/Disable Feature Connector
6	Enable/Disable PCI ROM Interface
5-2	Reserved
1	Indicate 3.3V/5V CVDD
0	Select 3.3V/5V Panel Interface

Bit 7 Enable/Disable Feature Connector.
Logical 1: Enable feature connector.
Logical 0: Disable feature connector

Bit 6 Enable/Disable PCI ROM Interface.
Logical 1: Enables PCI ROM interface.
Logical 0: Disables PCI ROM interface.

Bits 5-2: Reserved.

Bit 1: Indicate 3.3V/5V CVDD.
Logical 1: Indicates 3.3V.
Logical 0: Indicates 5V.

Bit 0: Selects 3.3V/5V Panel Interface.
Logical 1: Selects 3.3V
Logical 0: Selects 5V.

5.4.12 Configuration Register 3 (read only)

Read Port: 3C5h

Index: This register is accessed by writing a value of 2Eh to Sequencer Address location 3C4h. Bits 7-0 of this register correspond to MD15-MD8 respectively at power-up. BIOS reads these values at power-up and configures the appropriate extended registers. Note: These MD definitions hold when the feature connector is enabled. When the feature connector is disabled, configuration pins backward compatible to the 92C168 are used. See the Feature Connector Pin description, Section 3.3.11 for details

Bits	Function
7	Dual CAS# or Dual WE# DRAM Configuration (MD15)
6	VGA Enable Port (MD14)
5	Bus Size (MD13)
4	ISA/Local Bus Interface (MD12)
3	VESA/General Local Bus Interface (MD9)
2,1	Bus Interface ID (MD11-ID1, MD10-ID0)
0	Bus Interface Voltage Select (MD8)

Bits 7: Dual CAS# or Dual WE# DRAM Configuration. When the Feature Connector is enabled, this bit reflects the value of MD15 at power-on.
Logical 1: Selects dual WE# DRAM configuration.
Logical 0: Selects dual CAS# DRAM configuration.

Bit 6: VGA Enable Port. When the Feature Connector is enabled, this bit reflects the value of MD14 at power-on.
Logical 1: Selects 46E8 as VGA enable port.
Logical 0: Selects 3C3 as VGA enable port.

Bit 5: Bus Size. When the Feature Connector is enabled, this bit reflects the value of MD13 at power-on.
Logical 1: Selects 16-bit data bus.
Logical 0: Selects 32-bit data bus.

Bit 4: ISA/Local Bus Interface. When the Feature Connector is enabled, this bit reflects the value of MD12 at power-on.
Logical 1: Selects local bus.
Logical 0: Selects ISA bus.

Bit 3: VESA/General Local Bus Interface. When the Feature Connector is enabled, this bit reflects the value of MD9 at power-on.
Logical 1: Selects general local bus interface.
Logical 0: Selects VESA local bus interface (VL-Bus).

Bits 2,1: Bus Interface ID. When the Feature Connector is enabled, this bit reflects the values of MD11 and MD10 at power-on.

Bit 2 (ID0)	Bit 1 (ID1)	Bus ID
0	0	PCI Bus
1	0	386 VL-Bus
0	1	486 VL-Bus
1	1	Reserved

Bit 0: Bus Interface Voltage Select. When the Feature Connector is enabled, this bit reflects the value of MD8 at power-on.
Logical 1: Selects 3.3V bus interface.
Logical 0: Selects 5V bus interface.

5.4.13 OffsetA Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 20h to Graphics Controller Address Register location 3CE. This register is not used when linear addressing is enabled.

Bits	Function
7-5	Reserved
4-0 or [6-0]	Graphics Frame Buffer Offset for CPU Access

Bits 7-5: Reserved.

Bits 4-0: [6 -0] Graphics Frame Buffer Offset for CPU Access.
These frame buffer offset bits specify which 64K video memory segment is addressable through the standard VGA graphics mode memory access window (A0000-AFFFF). This register can programmed to function for CPU reads from display memory only, or for CPU read/writes from/to display memory. The register can also be programmed to use 64K (bits 4-0 of OffsetA select memory segment) or 16K (bits 6-0 of OffsetA select memory segment) offsets into the display memory. Bits 3, 1 and 0 of the Extended Mode Control Register (3CF.22) control the programming. Reference 3CF.22 for details.

5.4.14 OffsetB Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 21h to Graphics Controller Address Register location 3CE. This register is not used when linear addressing is enabled.

Bits	Function
7-5	Reserved
4-0 or [6-0]	Graphics Frame Buffer Offset for CPU Access

Bits 7-5: Reserved.

Bits 4-0: [6 -0] Graphics Frame Buffer Offset for CPU Access.
These frame buffer offset bits specify which 64K video memory segment is addressable through the standard VGA graphics mode memory access window (A0000-AFFFF). This register can programmed to function for CPU writes to display memory only, or for CPU read/ writes from/to display memory. The register can also be programmed to used 64K (bits 4-0 of OffsetA select memory segment) or 16K (bits 6-0 of OffsetA select memory segment) offsets into display memory. Bits 3, 1 and 0 of the Extended Mode Control Register (3CF.22) control the programming. Reference 3CF.22 for details.

5.4.15 Extended Mode Control Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 22h to Graphics Controller Address Register location 3CE.

Bits	Function
7	Memory Mapped I/O
6	Enable 16-bit Feature Connector Support
5	Enable 132-Column Text Mode
4	Enable 64K BIOS Decode
3	Offset Register Control Bit 2
2	PCI Burst Mode Enable
1	Offset Register Control Bit 1
0	Offset Register Control Bit 0

Bit 7: Enables/disables Memory Mapped I/O for the GUI Engine Register Set.
Logical 1: Enables Memory Mapped I/O at B8F00-B8F24. Bits 3, 2 of 3CF.06 must also be set to 0, 1 respectively to allow proper access to the GUI Engine Register Set.
Logical 0: Disables Memory Mapped I/O. Use I/O addresses to access the GUI Engine Register Set.

Bit 6: Enable 16-bit Feature Connector Support (PCI only)
Logical 1: Enables 16-bit feature connector support.
Logical 0: Disables 16-bit feature connector support.

Bit 5: Enable 132-Column Text Mode.
Logical 1: Enables 132-column text mode.
Logical 0: Standard 80 column text display.

Bit 4: Enable 64K BIOS decode.
Logical 1: Enables 64K video BIOS decode. Decode area is C0000-CFFFF.
Logical 0: Standard 32K video BIOS decode space. Decode area is C0000-C7FFF.

Bit 3: Offset Register Control Bit 2.
Logical 1: Enables register OffsetA as the display memory read segment register and enables register OffsetB as display memory write segment register.
Logical 0: Read/Write operations for register OffsetA and register OffsetB. Register OffsetB must be activated by bit 0 of this register before register OffsetB can be defined as a write only segment register or a read/write segment register.

Bit 2: PCI Burst Mode Enable.
Logical 1: Enables PCI Burst Mode for memory writes.
Logical 2: Disables PCI Burst Mode.

Bit 1: Offset Register Control Bit 1.
Logical 1: Configures OffsetA and OffsetB for 16KB offsets into display memory (bits 6-0 of the offset registers are used to program the address offset).
Logical 0: Configures OffsetA and OffsetB for 64KB offsets into display memory (bits 4-0 of the offset registers are used to program the address offset. Bits 5, 4 are reserved).

Bit 0: Offset Register Control Bit 0:
Logical 1: Activates register OffsetB.
Logical 0: Deactivates register OffsetB.

5.4.16 Hardware Cursor X Position Low Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 23h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor X Position

Bits 7-0: Hardware Cursor X Position. Lower 8 bits of the Hardware Cursor X position. Writing this register activates the Cursor X position change. Bits 2-0 are used to set the inter-character position.

5.4.17 Hardware Cursor X Position High Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 24h to Graphics Controller Address Register location 3CE.

Bits	Function
7	Extended Inter-Character Position
6-3	Reserved
2-0	Hardware Cursor X Position

Bit 7: Extended Inter-Character Position. This bit is used along with bits 2-0 of the Hardware Cursor X Position Low Register to set the inter-character position of the hardware cursor.

Bits 6-3: Reserved.

Bits 2-0: Hardware Cursor X Position. Upper 3 bits of the Hardware Cursor X position. Write this register first and then write the Hardware Cursor X Position Low Register to activate the X position change.

5.4.18 Hardware Cursor Y Position Low Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 25h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor Y Position

Bits 7-0: Hardware Cursor Y Position. Lower 8 bits of the Hardware Cursor Y position. Writing this register activates the Cursor Y position change.

5.4.19 Hardware Cursor Y Position High Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 26h to Graphics Controller Address Register location 3CE.

Bits	Function
7-3	Reserved
2-0	Hardware Cursor Y Position

Bits 7-3: Reserved.

Bits 2-0: Hardware Cursor Y Position. Upper 3 bits of the Hardware Cursor Y position. Write this register first and then write the Hardware Cursor Y Position Low Register to activate the Y position change.

5.4.20 Hardware Cursor/Pop-Up Icon Color 0 Low Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 27h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor/Pop-Up Icon Color 0

Bits 7-0: Hardware Cursor/Pop-Up Icon Color 0. Low byte of Hardware Cursor/Pop-Up Icon Color 0.

5.4.21 Hardware Cursor/Pop-Up Icon Color 0 Mid Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 28h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor/Pop-Up Icon Color 0

Bits 7-0: Hardware Cursor/Pop-Up Icon Color 0. 2nd byte of Hardware Cursor/Pop-Up Icon Color 0.

5.4.22 Hardware Cursor/Pop-Up Icon Color 0 High Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 29h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor/Pop-Up Icon Color 0

Bits 7-0: Hardware Cursor/Pop-Up Icon Color 0. High byte of Hardware Cursor/Pop-Up Icon Color 0. Please note the following when programming color at particular color depths:
Pseudo-color: Load the color value to the Hardware Cursor/Pop-Up Icon Color 0 Low Register. Activate color by writing any value to the Hardware Cursor/Pop-Up Icon Color 0 High Register.
HiColor: Load the color value to the Hardware Cursor/Pop-Up Icon Color 0 Mid Register and Hardware Cursor/Pop-Up Icon Color 0 High Register. The high byte should be the last value written.
True color: Load the color value to all three cursor color 0 registers. The high byte should be the last value written.

5.4.23 Hardware Cursor/Pop-Up Icon Color 1 Low Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Ah to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor/Pop-Up Icon Color 1

Bits 7-0: Hardware Cursor/Pop-Up Icon Color 1. Low byte of Hardware Cursor/Pop-Up Icon Color 1.

5.4.24 Hardware Cursor/Pop-Up Icon Color 1 Mid Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Bh to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor/Pop-Up Icon Color 1

Bits 7-0: Hardware Cursor/Pop-Up Icon Color 1. 2nd byte of Hardware Cursor/Pop-Up Icon Color 1.

5.4.25 Hardware Cursor/Pop-Up Icon Color 1 High Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Ch to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Hardware Cursor/Pop-Up Icon Color 1

Bits 7-0: Hardware Cursor/Pop-Up Icon Color 1. High byte of Hardware Cursor/Pop-Up Icon Color 1. Please note the following when programming the Hardware Cursor/Pop-Up Icon color at particular color depths:
Pseudo-color: Load the color value to the Hardware Cursor/Pop-Up Icon Color 1 Low Register. Activate color by writing any value to the Hardware Cursor/Pop-Up Icon Color 1 High Register.
HiColor: Load the color value to the Hardware Cursor/Pop-Up Icon Color 1 Mid Register and Hardware Cursor/Pop-Up Icon Color 1 High Register. The high byte should be the last value written.
True color: Load the color value to all three cursor color 1 registers. The high byte should be the last value written.

5.4.26 Hardware Cursor Pattern Offset Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Dh to Graphics Controller Address Register location 3CE.

Bits	Function
7-4	Reserved
3, 2	Select Hardware Cursor Pattern
1	Select Hardware Cursor Size
0	Enable Hardware Cursor

Bit 7-4: Reserved.

Bits 3, 2: Select Hardware Cursor Pattern. For a 32x32x2 Hardware Cursor and Pop-up Icon off, bits 3 and 2 may be used to select one of four available patterns.

3	2	Pattern Location
0	0	F:FC00h
0	1	F:FD00h
1	0	F:FE00h
1	1	F:FF00h

For a 64x64x2 Hardware Cursor and Pop-up Icon off, bit 2 may be used to select one of two available patterns. A logical 0 selects the pattern at F800h. A logical 1 selects the pattern at FC00h. Bit 3 should be set to a logical 0. If the Pop-up Icon is on, only one cursor pattern is available (at F800h). For this case, bits 3 and 2 should be set to a logical 0.

Bit 1: Select Hardware Cursor Size.
Logical 1: Selects 32x32x2 cursor.
Logical 0: Selects 64x64x2 cursor.

Bit 0: Enable Hardware Cursor.
Logical 1: Enables Hardware Cursor.
Logical 0: Disables Hardware Cursor.
The hardware cursor is always in the highest available bank of display memory.

5.4.27 Hardware Cursor Y Origin Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Eh to Graphics Controller Address Register location 3CE.

Bits	Function
7-6	Reserved
5-0	Hardware Cursor Y Origin

Bits 7, 6: Reserved.

Bits 5-0: Hardware Cursor Y Origin.
Specifies Y offset from the top-left corner of the cursor pattern. Used for case when part of the Hardware Cursor is off the screen edge. Bit 5 not used for 32x32x2 cursor.

5.4.28 Hardware Cursor X Origin Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 2Fh to Graphics Controller Address Register location 3CE.

Bits	Function
7	Extended Inter-Character Position
6	Reserved
5-0	Hardware Cursor X Origin

Bit 7: Extended Inter-Character Position. This bit is used with bits 2-0 to set the inter-character origin position.

Bit 6: Reserved.

Bits 5-0: Hardware Cursor X Origin.
Specifies X offset from the top-left corner of the cursor pattern. Used for case when part of the Hardware Cursor is off the screen edge. Bit 5 not used for 32x32x2 cursor. Bits 2-0 set inter-character origin position.

5.4.29 Pop-up Icon X Position Low Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 30h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Pop-up Icon X Position

Bits 7-0: Pop-up Icon X Position.
Lower 8 bits of the Pop-up Icon X position. Writing this register activates the X position change. Bits 2-0 determine inter-character position.

5.4.30 Pop-up Icon X Position High Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 31h to Graphics Controller Address Register location 3CE.

Bits	Function
7	Extended Inter-Character Position
6-3	Reserved
2-0	Pop-up Icon X Position

Bit 7: Extended Inter-Character Position. This bit is used along with bits 2-0 of the Pop-Up Icon Low X Register to set inter-character position.

Bits 6-3: Reserved.

Bits 2-0: Pop-up Icon X Position. Upper 3 bits of the Pop-up Icon X position. Write this register first and then write the Pop-up Icon X Position Low register to activate the X position change.

5.4.31 Pop-up Icon Y Position Low Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 32h to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Pop-up Icon Y Position

Bits 7-0: Pop-up Icon Y Position.
Lower 8 bits of the Pop-up Icon Y position. Writing this register activates the Y position change.

5.4.32 Pop-up Icon Y Position High Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 33h to Graphics Controller Address Register location 3CE.

Bits	Function
7-3	Reserved
2-0	Pop-up Icon Y Position

Bits 7-3: Reserved.

Bits 2-0: Pop-up Icon Y Position.
Upper 3 bits of the Pop-up Icon Y position. Write this register first and then write the Pop-up Icon Y Position Low register to activate the Y position change.

5.4.33 Pop-up Icon Color 2 Low Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 3Ah to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Pop-up Icon Color 2

Bits 7-0: Pop-up Icon Color 2.
Low byte of Pop-up Icon Color 2.

5.4.34 Pop-up Icon Color 2 Mid Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 3Bh to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Pop-up Icon Color 2

Bits 7-0: Pop-up Icon Color 2.
2nd byte of Pop-up Icon Color 2.

5.4.35 Pop-up Icon Color 2 High Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 3Ch to Graphics Controller Address Register location 3CE.

Bits	Function
7-0	Pop-up Icon Color 2

Bits 7-0: Pop-up Icon Color 0.
High byte of Pop-up Icon Color 2. Please note the following when programming the Pop-up Icon color at particular color depths:
Pseudo-color: Load the color value to the Pop-up Icon Color 2 Low Register. Activate color by writing any value to the Pop-up Icon Color 2 High Register.
HiColor: Load the color value to the Pop-up Icon Color 2 Mid Register and Pop-up Icon Color 0 High Register. The high byte should be the last value written.
True color: Load the color value to all three cursor color 2 registers. The high byte should be the last value written.

5.4.36 Pop-up Icon Control Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 3Dh to Graphics Controller Address Register location 3CE.

Bits	Function
7-3	Reserved
2	Screen Saver Control
1	Pop-up Icon Size
0	Enable Pop-up Icon

Bits 7-3: Reserved

Bit 2: Screen Saver Control.
Logical 1: Enables screen saver. Screen is blacked out. Only HW cursor will show on the screen.
Logical 0: Disables screen saver.

Bit 1: Pop-up Icon Size.
Logical 1: Selects 128x128x2 Pop-up Icon size. To achieve this size, the 64x64x2 icon is double scanned vertically, and each pixel is replicated horizontally (double dot).
Logical 0: Selects 64x64x2 Pop-up Icon size.

Bit 0: Enable Pop-up Icon.
Logical 1: Enables Pop-up Icon. Pop-up Icon stored at video memory location F800h.
Logical 0: Disables Pop-up Icon.

Note The Pop-up Icon location is always in the highest available bank of display memory.

5.4.37 Scratch Pad Register 0

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 1Ch to CRT Controller Address Register location 3D4.

Bits	Function
7-0	Scratch Pad Bits

Bits 7-0: Scratch Pad Bits.
Scratch pad bits 7-0.

5.4.38 Scratch Pad Register 1

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 1Dh to CRT Controller Address Register location 3D4.

Bits	Function
7-0	Scratch Pad Bits

Bits 7-0: Scratch Pad Bits.
Scratch pad bits 7-0.

5.4.39 Scratch Pad Register 2

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 1Eh to CRT Controller Address Register location 3D4.

Bits	Function
7-0	Scratch Pad Bits

Bits 7-0: Scratch Pad Bits.
Scratch pad bits 7-0.

5.4.40 800x600 Expansion Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 24h to CRT Controller Address Register location 3D4.

Bits	Function
7-4	Reserved
3	Enable Space Dithering Algorithm #2
2	Enable Horizontal Text Mode Expansion for 800x600 Panels
1	Enable Vertical Expansion for 800x600 Panels
0	Enable Horizontal Expansion for 800x600 Panels

Bit 7-4: Reserved.

Bit 3: Enable Space Dithering Algorithm #2.
Logical 1: Enables space dithering algorithm #2.

Note Bit 7 of the Panel Display Control Register must be set to a logical 0 for this setting to take effect.

Logical 0: Disables space dithering algorithm #2.

Bit 2: Enable Horizontal Test Mode Expansion for 800x600 Panels.
Logical 1: Enables text mode expansion for 800x600 panels. This setting forces 10-dot text display for 8 or 9-dot text modes. The 8th dot is triplicated for 8-dot modes. The 9th dot is duplicated for 9-dot modes.

Note Bit 0 of this register must also be set to a logical 1 for this setting to take effect.

Logical 0: Disables text mode expansion for 800x600 panels.

Bit 1: Enable Vertical Expansion for 800x600 Panels.
Logical 1: Enables vertical expansion.
Logical 0: Disables vertical expansion.

Bit 0: Enable Horizontal Expansion.
Logical 1: Enables horizontal expansion. Double dot every 4th pixel.
Logical 0: Disables horizontal expansion.

5.4.41 Device ID Register 1 (read only)

Read Port: 3D5

Index: This register is accessed by writing a value of 28h to CRT Controller Address Register location 3D4.

Bits	Function
7-0	Device ID 1

Bits 7-0: Device ID1. These bits provide a device ID for the 92C178. The value in this register is 17h.

5.4.42 Device ID Register 2 (read only)

Read Port: 3D5

Index: This register is accessed by writing a value of 29h to Graphics Controller Address Register location 3D4.

Bits	Function
7-0	Device ID 2

Bits 7-0: Device ID2. These bits provide a device ID for the 92C178. The value in this register is 80h.

5.4.43 Extended Overflow Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 30h to CRT Controller Address Register location 3D4. Bit 5 of the CRT Extended Control Register (3D5.33) must be a logical 0 in order to access this register.

Bits	Function
7	Reserved
6, 5	Offset Bits 9, 8
4	Line Compare Bit 10
3	Vertical Total Bit 10
2	Vertical Display Enable End Bit 10
1	Vertical Blank Start Bit 10
0	Vertical Retrace Start Bit 10

Bit 7: Reserved.

Bits 6,5: Offset Bits 9, 8.
The lower eight bits of the offset value are located in the CRTC Offset Register (3D5.13). The ten bit value specifies the address width of the display. The value corresponds to the difference between the addresses of two vertically neighboring pixels.

Bit 4: Line Compare Bit 10.
Bit 9 is located in the Maximum Scan Line Register (3D5.09). Bit 8 is located in the Vertical Overflow Register (3D5.07). Bits 7-0 are located in the Line Compare Register (3D5.18). The 11-bit value is used for split screen display.

Bit 3: Vertical Total Bit 10.
Bits 9 and 8 are located in the Vertical Overflow Register (3D4.07). Bits 7-0 are located in the Vertical Total Register (3D5.06). The 11-bit value specifies the total number of displayed and undisplayed scan lines for a given mode.

Bit 2: Vertical Display Enable Bit 10. Bits 9 and 8 are located in the Vertical Overflow Register (3D4.07). Bits 7-0 are located in the Vertical Display Enable End Register. The 11-bit value specifies the last horizontal scan line to be displayed on the screen.

Bit 1: Vertical Blank Start Bit 10. Bit 9 is located in the Maximum Scan Line Register (3D5.09). Bit 8 is located in the Vertical Overflow Register (3D4.07). Bits 7-0 are located in the Vertical Display Enable End Register (3D5.12). The 11-bit value specifies the horizontal scan line at which the data stream to the display is stopped during the vertical retrace period.

Bit 0: Vertical Retrace Start Bit 10. Bits 9 and 8 are located in the Vertical Overflow Register (3D4.07). Bits 7-0 are located in the Vertical Retrace Start Register (3D5.10). The 11-bit value specifies the horizontal scan line count at which the vertical sync pulse is generated.

5.4.44 Starting Address Overflow Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 31h to CRT Controller Address Register location 3D4.

Bits	Function
7	Override Vertical Expansion
6	Interlaced Mode Select
5	Memory Interface Voltage Select
4	Panel Interface Voltage Select
3	Reserved
2-0	Starting Address Overflow Bits 18-16

Bit 7: Override Vertical Expansion. This bit overrides bit 4 of the Panel Display Control Register (3D5.35). Logical 1: Overrides vertical expansion. Use this setting for 1024x768 panels. Logical 0: Does not override vertical expansion. Use this setting for 640x480 panels.

Bit 6: Interlaced Mode Select. Set this bit, along with bit 7 of the Clock Select Register (3C5.12), to a logical 1 to enable interlaced mode.

Bit 5: Memory Interface Voltage Select. Logical 1: Selects 3.3V. Logical 0: Selects 5V.

Bit 4: Panel Interface Voltage Select. Logical 1: Selects 3.3V. Logical 0: Selects 5V.

Bit 3: Reserved.

Bits 2, 0: Starting Address Overflow Bits 18-16. Bit 15-8 are located in the Start Address High Register (3D5.0C). Bits 7-0 are located in the Start Address Low Register (3D5.0D). The 19-bit value specifies the address in display memory which corresponds to the upper left corner of the screen.

5.4.45 Interlaced Odd Frame Horizontal Retrace End Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 32h to CRT Controller Address Register location 3D4.

Bits	Function
7-0	Interlaced Odd Frame Horizontal Retrace End

Bit 7-0: Interlaced Odd Frame Horizontal Retrace End. Specifies the horizontal sync pulse width for the odd frame of an interlaced mode (e.g. 1024x768).

5.4.46 Extended CRT Control Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 33h to CRT Controller Address Register location 3D4.

Bits	Function
7	Select CRT Mode
6	Select LCD Mode
5	Lock LCD Shadow Registers
4	Select 244 Lines/Frame Dual Scan Panel
3	Reserved
2	BLANK# Select
1	Enable Starting Address Double Buffering
0	Force 8 Dot Mode

Bit 7: Select CRT Mode.
Logical 1: Enables CRT Mode display.
Logical 0: Disables CRT Mode display.

Bit 6: Select LCD Mode.
Logical 1: Enables LCD Mode display.
Logical 0: Disables LCD mode display.
Set both bits 7 and 6 to a logical 1 to enable Simultaneous Display. Be sure that the LCD Shadow Registers have been configured correctly and that the correct panel type has been selected before enabling simultaneous display.

Bit 5: Lock LCD Shadow Registers
Logical 1: Locks LCD Shadow Registers. Check the register tables at the beginning of this section for details on which registers are shadowed for 640x480 panels and 1024x768 panels.
Logical 0: Unlocks LCD Shadow Registers.
Bit 5 must be set to a logical 0 to unlock the Extended Overflow Register (3D5.30).

Bit 4: Select 244 Lines/Frame Dual Scan Panel.
Logical 1: Selects 244 lines/frame dual scan panel.
Logical 0: Do not select 244 lines/frame dual scan panel. Other options available for dual scan panels are 240 and 242 lines/frame. Bit 4 of the Panel Select Register (3D5.34) may be used to select 242 lines/frame. The default value of 240 lines/frame is selected if neither the 242 lines/frame or the 244 lines/frame bit is set.

Bit 3: Reserved.

Bit 2: BLANK# Select.
Logical 1: Blanking is enabled at Display Enable End. This setting will eliminate screen borders.
Logical 0: Standard Blanking signal.

Bit 1: Enable Starting Address Double Buffering.
Logical 1: Enables double buffering for the Starting Address High Register (3D5.0C) and Starting Address Low Register (3C5.0D). This setting is useful for applications which need to continually change the starting address (e.g. switching between two images in display memory to create animation effects).
Logical 0: Standard access for 3D5.0C and 3D5.0D.

Bit 0: Force 8 Dot Mode.
Logical 1: Forces 8 Dot Mode for VGA modes which typically use 9 dot display format (modes 0+h, 1+h, 2+h, 3+h, 7h, and 7+h). This allows the entire display to fit on the 640x480 LCD screen.
Logical 0: Selects standard 9 dot display for modes mode 0+h, 1+h, 2+h, 3+h, 7h, and 7+h.

5.4.47 Panel Select Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 34h to CRT Controller Address Register location 3D4.

Bits	Function
7, 6	TFT Panel Type Select
5	Select 1024x768 Panel
4	Select 242 Lines/Frame Dual Scan Panel
3-1	STN Panel Type Select
0	Select TFT Panel

Bits 7, 6: TFT Panel Type Select.

7	6	TFT Panel Type
0	0	9-bit (512 color)
0	1	12-bit (4K color)
1	0	3-bit (8 color)
1	1	18-bit (256K color)

Bit 0 and bit 3 of this register must be set to a logical 1 when selecting a TFT panel. Bit 3 selects single panel. Bit 0 selects TFT panel.

Bit 5: Select 1024x768 Panel.
Logical 1: Selects 1024x768 panel.
Logical 0: Selects 640x480 panel.
800x600 panel size may also be selected. See bit 3 of Panel Output Control Register (3D5.36)

Bit 4: Select 242 Lines/Frame Dual Scan Panel
Logical 1: Selects 242 line/frame dual scan panel.
Logical 0: Do not select 242 lines/frame dual scan panel. Other options available for dual scan panels are 240 and 244 lines/frame. Bit 4 of the Extended CRT Control Register (3D5.33) may be used to select 244 lines/frame. The default value of 240 lines/frame is selected if neither the 242 lines/frame or the 244 lines/frame bit is set.

Bits 3-1: STN Panel Type Select.

Bit 3 (single/ dual)	Bit 2 (color/ mono)	Bit 1 (color depth)	STN Panel Type
0	0	0	Dual Monochrome
0	0	1	Reserved
0	1	0	Dual Color 8-bit
0	1	1	Dual Color 16-bit
1	0	0	Single Monochrome 4-bit
1	0	1	Single Monochrome 8-bit
1	1	0	Single Color 8-bit
1	1	1	Single Color 16-bit

Bit 0: Select TFT/STN Panel.
Logical 1: Selects TFT panel.
Logical 0: Selects STN panel.

5.4.48 Panel Display Control Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 35h to CRT Controller Address Register location 3D4.

Bits	Function
7	Disable Space Dithering Algorithm #1
6	Disable TFT Dithering
5	Enable Auto Centering
4	Enable Vertical Expansion
3	Enable Graphics Mode Reverse Video
2	Enable Text Mode Reverse Video
1	Enable Text Mode Contrast Enhancement
0	Enable Wave Equation Conversion

Bit 7: Disable Space Dithering Algorithm #1.
Logical 1: Disables space dithering algorithm #1. Gives 64 gray shades on a monochrome panel and 256K colors on a color panel.
Logical 0: Enables space dithering algorithm #1. Gives 256 gray shades on a monochrome panel and 16M colors on an STN color panel or 18-bit TFT panel.

Note A second space dithering algorithm is controlled by bit 3 of the 800x600 Expansion Register (3D5.24).

Bit 6: Disable TFT Dithering.
Logical 1: Disables TFT dithering. TFT dithering is effective for 3-, 9-, and 12-bit TFT panels. This bit is not effective for 18-bit TFT panels, since they already deliver 16M colors when space dithering is enabled (bit 7).
Logical 0: Enables TFT dithering.
Bits 6 and 7 should be enabled for maximum color display on 3-, 9-, and 12-bit TFT panels.

Bit 5: Enable Auto Centering (640x480, 800x600, and 1024x768 panels).
Logical 1: Enables Auto Centering.
Logical 0: Disables Auto Centering.

Bit 4[a]: Enable Vertical Expansion (640x480 panels).
Logical 1: Enables Vertical Expansion.
Logical 0: Disables Vertical Expansion.

Bit 3[b]: Enable Graphics Mode Reverse Video.
Logical 1: Enables Graphics Mode Reverse Video.
Logical 0: Disables Graphics Mode Reverse Video.

Bit 2[c]: Enable Text Mode Reverse Video.
Logical 1: Enables Text Mode Reverse Video.
Logical 0: Disables Text Mode Reverse Video.

Bit 1: Enable Text Mode Contrast Enhancement.
Logical 1: Enables Text Mode Contrast Enhancement. Contrast enhancement is achieved by comparing the on screen foreground and background colors with a hardwired color threshold. If the color is above the threshold, it is converted to white. If the color is below the threshold, it is converted to black.
Logical 0: Disables Text Mode Contrast Enhancement.

Bit 0: Enable Wave Equation Conversion.
Logical 1: Enables Wave Equation conversion. The wave equation (Y = 0.3R + 0.59G + 0.11B) is used to convert RGB values determined by the color look up table in the RAMDAC to a grayscale output.
Logical 0: Disables Wave Equation conversion. RGB values used for color display. G value used for mono display.

a. Expansion for 800x600 panels controlled by bits 2-0 of the 800x600 Expansion Register (3D5.24).
b. No effect for TFT. Effective for STN (color or mono) panel.
c. Ibid.

5.4.49 Panel Output Control Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 36h to CRT Controller Address Register location 3D4.

Bits	Function
7,6	Select Shadow Register Set
5	Enable 3 Sets of Shadow Registers
4	Select External RAMDAC
3	Select 800x600 Panel
2	First Line Marker (FLM) Signal Polarity
1	Line Pulse (LP) Signal Polarity
0	Turn Off Shift Clock (SCK) During Blank Period

Bits 7,6: Select Shadow Register Set. Bit 5 must be programmed to a logical 1 to select all sets. If bit 5 is programmed to a logical 0, only the 480 line set is available.

7	6	Shadow Register Set
0	0	Set 1 (default). Vertical and horizontal CRT registers available.
0	1	Set 2. Vertical and horizontal CRT registers available.
1	0	Set 3. Only selected vertical CRT registers available. Horizontal register set same as for 480 line mode.
1	1	Reserved

See Table 5-12 for additional detail.

Bit 5: Enable 3 Sets of Shadow Registers.
Logical 1: Enables all three sets of shadow registers. The shadow register set to be used is selected by programming bits 7, 6 of this register.
Logical 0: Use default 480 line mode register set.

Bit 4: Select External RAMDAC.
Logical 1: Selects external RAMDAC.
Logical 0: Selects internal RAMDAC (default).

Bit 3: Select 800x600 Panel.
Logical 1: Selects 800x600 panel
Logical 0: Do not select 800x600 panel.

Bit 2: FLM Signal Polarity.
Logical 1: Selects negative polarity for signal FLM.
Logical 0: Selects positive polarity for signal FLM.

Bit 1: LP Signal Polarity.
Logical 1: Selects negative polarity for LP.
Logical 0: Selects positive polarity for LP.

Bit 0: Turn Off SCK During Blank Period.
Logical 1: Turn off SCK during the blank period.
Logical 0: Keep SCK on during the blank period.

5.4.50 FLM Adjustment Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 37h to CRT Controller Address Register location 3D4.

Bits	Function
7	Adjustment Direction
6-0	Adjust Signal FLM

Bit 7: Adjustment Direction. Bit 7 selects the adjustment direction for signal FLM. The amount of adjustment is determined by the value of bits 6-0.
Logical 1: Adjust right.
Logical 0: Adjust left.

Bit 6-0: Adjust Signal FLM. Bits 6-0 are used to change the scan line at which FLM becomes active. The default value is 0h (no shift). The range of adjustment is -127 lines to +127 lines.

5.4.51 Vertical Expansion Adjustment Register (for expansion to 640x480 only)

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 38h to CRT Controller Address Register location 3D4.

Bits	Function
7-0	Vertical Expansion Adjustment.

Bits 7-0: Vertical Expansion Adjustment. Bits 7-0 are used to offset the start of the double scan line pattern for vertical expansion. The value indicates the scan line offset at which to start the pattern. The default value is 0h (no offset). The register is used for graphics mode vertical expansion adjustment only.
This register is only effective when vertical expansion is enabled. Bit 4 of the Panel Display Control Register (3D5.35) controls vertical expansion.

5.4.52 Horizontal Centering Adjustment Register (TFT panels only)

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 39h to CRT Controller Address Register location 3D4.

Bits	Function
7-3	Character Adjustment
2-0	Pixel Adjustment

Bits 7-3: Character Adjustment. Bits 7 -3 specify the number of character spaces to the right the display needs to be shifted in order for the given mode to be horizontally centered.

Bits 2-0: Pixel Adjustment. Bits 2-0 specify the number of pixels to the right the display needs to be shifted in order for the given mode to be horizontally centered.
This register is only effective when auto centering is enabled. Bit 5 of the Panel Display Control Register (3D5.35) controls auto centering.

5.4.53 Vertical Centering Adjustment Register

Note May be used for 1024x768, 800x600, and 640x480 TFT panels.

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 3Ah to CRT Controller Address Register location 3D4.

Bits	Function
7-0	Vertical Centering Adjustment

Bits 7-0: Vertical Centering Adjustment. Bits 7-0 specify the number of scan lines the display needs to be shifted down in order for the given mode to be vertically centered.
This register is only effective when auto centering is enabled. Bit 5 of the Panel Display Control Register (3D5.35) controls auto centering.

5.4.54 Horizontal Centering for 1024x768 Panel Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 3Bh to CRT Controller Address Register location 3D4.

Bits	Function
7-0	Character Adjustment

Bits 7-0: Character Adjustment. Bits 7 -0 specify the number of character spaces to the right the display needs to be shifted in order for the given mode to be horizontally centered. This register should be used with 1024x768 panels only.
This register is only effective when auto centering is enabled. Bit 5 of the Panel Display Control Register (3D5.35) controls auto centering.

5.4.55 Modulation Adjustment Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 3Ch to CRT Controller Address Register location 3D4.

Bits	Function
7-0	Modulation Adjustment

Bits 7-0: Modulation Adjustment. Bits 7-0 specify the output condition of signal M to the flat panel. A value of 0h written to this register specifies M will toggle every frame. M may also be programmed to toggle every specified number of scan lines. Allowable values are from 1 -255 scan lines. For example, a value of 03h means M will toggle every third scan line. The default value for this register is 0h.

5.4.56 Power Down Control Register 1

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 44h to CRT Controller Address Register location 3D4.

Bits	Function
7	Enable Power Down Register
6	Select Hardware Deep Sleep Mode
5	Select VGA Activity to Reset Counter Timers
4	Select ACTIVITY input pin to Reset Counter Timers
3	Select Hardware Suspend Mode
2	Select Hardware Standby Mode
1	Force Suspend Mode
0	Force Standby Mode

Bit 7: Enable Power Down Register.
Logical 1: Enables Power Down Register.
Logical 0: Disables Power Down Register.

Bit 6: Select Hardware Deep Sleep Mode.
Logical 1: Selects Deep Sleep Mode.
Logical 0: Do not select Deep Sleep Mode.
SUSPEND (pin 173) is used to engage/ resume this mode.

Bit 5: Select VGA Activity to Reset Counter Timers.
Logical 1: Selects VGA activity to reset the Standby Mode timer and/or Backlight timer.
Logical 0: VGA activity not used as a condition to reset the Standby Mode timer and/or Backlight timer.

Bit 4: Select ACTIVITY Input Pin to Reset Counter Timers.
Logical 1: Selects ACTIVITY (pin 172) to reset the Standby Mode timer and/or Backlight timer.
The ACTIVITY pin toggles to indicate mouse and keyboard activity.
Logical 0: The ACTIVITY pin is not used as a condition to reset the Standby Mode timer and/or Backlight timer.
Bits 5, 4 may both be activated at the same time.

Bit 3: Select Hardware Suspend Mode.
Logical 1: Selects hardware Suspend Mode. Input signal SUSPEND (pin 173) is used to engage Suspend Mode.
Logical 0: Do not select hardware Suspend Mode.

Bit 2: Select Hardware Standby Mode. Logical 1: Selects hardware Standby Mode. Input signal STANDBY (pin 171) is used to engage Standby Mode. Logical 0: Do not select hardware Standby Mode.

Bit 1: Force Suspend Mode. Logical 1: Forces Suspend Mode. To return the 92C178 to normal operations, toggle this bit to a logical 0.

Bit 0: Force Standby Mode. Logical 1: Forces Standby Mode. To return the 92C178 from to normal operations, toggle this bit to a logical 0. Standby and Suspend Modes have no effect if the CRT is on. Backlight off will work with the CRT on, however.

5.4.57 Standby Mode Timeout Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 45h to CRT Controller Address Register location 3D4.

Bits	Function
7	Enable Standby Mode Timeout Register
6, 5	Reserved
4-0	Countdown Setting

Bits 7: Enable Standby Mode Timeout Register. Logical 1: Enables Standby Mode Timeout Register. Logical 0: Disables Standby Mode Timeout Register.

Bits 6, 5: Reserved.

Bits 4-0: Countdown Setting. The range is 0-31 minutes in one minute increments (accuracy is ± 25 seconds).

5.4.58 Power Down Backlight Timeout Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 46h to CRT Controller Address Register location 3D4.

Bits	Function
7	Enable Power Down Backlight Timeout Register
6, 5	Reserved
4-0	Countdown Setting

Bits 7: Enable Power Down Backlight Timeout Register. Logical 1: Enables Power Down Backlight Timeout Register. Logical 0: Disables Power Down Backlight Timeout Register.

Bits 6, 5: Reserved.

Bits 4-0: Countdown Setting. The range is 0-31 minutes in one minute increments (accuracy is ± 25 seconds).

5.4.59 Power Down Control Register 2

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 47h to CRT Controller Address Register location 3D4.

Bits	Function
7-3	Reserved
5	Select SUSPEND Signal Polarity
4	Select STANDBY Signal Polarity
3	Select STANDBY Signal Direction
2	Select Suspend Mode Memory Clock Source
1, 0	INMCK Divide for Standby Mode

Bits 7, 6: Reserved.

Bit 5: Set SUSPEND Signal Polarity to be active high (logical 1) or active low (logical 0). Logical 1: Signal active high. Logical 0: Signal active low.

Bit 4: Set STANDBY Signal Polarity to be active high (logical 1) or active low (logical 0). Logical 1: Signal active high. Logical 0: Signal active low.

Bit 3: Select STANDBY Signal Direction. The default setting for this bit is a logical 0. Logical 1: Signal STANDBY is used as an input to enable Standby Mode. Logical 0: Signal STANDBY is used an output to indicate the condition of the Standby Counter Timer. A logical 1 indicates a timeout condition.

Bit 2: Select Suspend Mode Memory Clock Source.
Logical 1: Selects 14.318MHz system clock as the Suspend Mode memory clock source. The clock is divided down internally to 32KHz.
Logical 0: Selects 32KHz oscillator as Suspend Mode memory clock source.

Bits 1, 0: INMCK Divide for Standby Mode.

1	0	Divide By
0	0	1 (default)
0	1	2
1	0	4
1	1	8

Bit 2 of the Power Down Refresh Control Register must be set to a logical 1 for the INMCK Divide bits to be effective.

5.4.60 Power Down Refresh Control Register

Read/Write Port: 3D5

Index: This register is accessed by writing a value of 48h to CRT Controller Address Register location 3D4.

Bits	Function
7-3	Reserved
2	Enable Slow Refresh for Standby Mode
1, 0	Suspend Mode Refresh Control

Bits 7-3: Reserved.

Bit 2: Enable Slow Refresh for Standby Mode.
Logical 1: Enables slow refresh.
Logical 0: Disables slow refresh.

Bits 1, 0: Suspend Mode Refresh Control.

1	0	Select
0	0	CAS before RAS generated by 92C178 (default)
0	1	DRAM self refresh
1	0	Reserved
1	1	No refresh. DRAM data not saved.

5.5 Clock Synthesizer Register Descriptions

The clock synthesizers registers are accessed by sending a register index value to port 3C4h, followed by data.

5.5.1 Video Clock Group 0 (VCK0) Input Frequency Divider

Write Port: 3C4h

Index: 20h

Bit	Definition
7	Post scale.
6	Reserved.
5-0	Input Frequency Divider Value (D).

Bit 7: Post Scale.
Logical 1: Divide clock output from PLL by two.
Logical 0: Do not divide clock output from PLL by two. (Default)

Bit 6: Reserved

Bits 5-0: Input Frequency Divider Value. This value is designated "D". Default value after power-up is 1Fh.

5.5.2 Video Clock Group 0 (VCK0) VCO Frequency Divider

Write Port: 3C4h

Index: 21h

Bit	Definition
7	High Frequency Select.
6-0	VCO Frequency Divider Value (N).

Bit 7: High Frequency Select
Logical 1: Select for frequencies above 80MHz.
Logical 0: Select for frequencies of 80MHz or less. (Default)

Bits 6-0: VCO Frequency Divider Value. This value is designated "N". Default value after power-up is 6Dh.

5.5.3 Video Clock Group 1 (VCK1) Input Frequency Divider

Write Port: 3C4h

Index: 22h

Bit	Definition
7	Post scale.
6	Reserved.
5-0	Input Frequency Divider Value (D).

Bit 7: Post Scale.
Logical 1: Divide clock output from PLL by two.
Logical 0: Do not divide clock output from PLL by two. (Default)

Bit 6: Reserved

Bits 5-0: Input Frequency Divider Value. This value is designated "D". Default value after power-up is 17h.

5.5.4 Video Clock Group 1 (VCK1) VCO Frequency Divider

Write Port: 3C4h

Index: 23h

Bit	Definition
7	High Frequency Select.
6-0	VCO Frequency Divider Value (N).

Bit 7: High Frequency Select
Logical 1: Select for frequencies above 80MHz.
Logical 0: Select for frequencies of 80MHz or less. (Default)

Bits 6-0: VCO Frequency Divider Value. This value is designated "N". Default value after power-up is 5Bh.

5.5.5 Video Clock Group 2 (VCK2) Input Frequency Divider

Write Port: 3C4h

Index: 24h

Bit	Definition
7	Post scale.
6	Reserved.
5-0	Input Frequency Divider Value (D).

Bit 7: Post Scale.
Logical 1: Divide clock output from PLL by two.
Logical 0: Do not divide clock output from PLL by two. (Default.)

Bit 6: Reserved

Bits 5-0: Input Frequency Divider Value. This value is designated "D". Default value after power-up is 23h.

5.5.6 Video Clock Group 2 (VCK2) VCO Frequency Divider

Write Port: 3C4h

Index: 25h

Bit	Definition
7	High Frequency Select.
6-0	VCO Frequency Divider Value (N).

Bit 7: High Frequency Select
Logical 1: Select for frequencies above 80MHz.
Logical 0: Select for frequencies of 80MHz or less. (Default)

Bits 6-0: VCO Frequency Divider Value. This value is designated "N". Default value after power-up is 58h.

5.5.7 Video Clock Group 3 (VCK3) Input Frequency Divider

Write Port: 3C4h

Index: 26h

Bit	Definition
7	Post scale.
6	Reserved.
5-0	Input Frequency Divider Value (D).

Bit 7: Post Scale.
Logical 1: Divide clock output from PLL by two.
Logical 0: Do not divide clock output from PLL by two. (Default.)

Bit 6: Reserved

Bits 5-0: Input Frequency Divider Value. This value is designated "D". Default value after power-up is 18h.

5.5.8 Video Clock Group 3 (VCK3) VCO Frequency Divider

Write Port: 3C4h

Index: 27h

Bit	Definition
7	High Frequency Select.
6-0	VCO Frequency Divider Value (N).

Bit 7: High Frequency Select
Logical 1: Select for frequencies above 80MHz.
Logical 0: Select for frequencies of 80MHz or less. (Default)

Bits 6-0: VCO Frequency Divider Value. This value is designated "N". Default value after power-up is 45h.

5.5.9 Memory Clock Input Frequency Divider

Write Port: 3C4h

Index: 28h

Bit	Definition
7, 6	Reserved.
5-0	Frequency Divider Value (D).

Bits 7,6: Reserved

Bits 5-0: Frequency Divider Value. This value is designated "D". Default value after power-up is 10h.

5.5.10 Memory Clock VCO Frequency Divider

Write Port: 3C4h

Index: 29h

Bit	Definition
7	Reserved.
6-0	VCO Frequency Divider Value (N).

Bit 7: Reserved.

Bits 6-0: VCO Frequency Divider Value. This value is designated "N". Default value after power-up is 2Ah.

5.5.11 Programming Video Clock and Memory Clock Frequencies

The video clock group is selected by setting bits 3,2 (see table) of the Miscellaneous Function Control Register (3C2).

Bit 3	Bit 2	VCK Clock Group
0	0	Video Clock Group 0
0	1	Video Clock Group 1
1	0	Video Clock Group 2
1	1	Video Clock Group 3

Equations for VCK and MCK frequency selection follow.

5.5.11.1 Equations for VCK and MCK Frequency Selection

The output frequency of the selected video clock group is determined by the following equation:

$$Fv = \frac{(14.318MHz \times N/D)}{(P+1)}$$

Where:

- Fv is the video clock output for the given video clock group
- N is the video clock VCO divider value
- D is the video clock input clock divider value
- P is the post scale

The output frequency of the selected video clock group is determined by the following equation:

$$Fm = \frac{14.318MHz \times N}{(int(D/4) \times 4)}$$

Where:

- Fv is the memory clock output
- N is the memory clock VCO divider value
- D is the memory clock input clock divider value.

Note In order to reduce frequency error, D for the memory clock should be divisible by four.

5.6 Overlay Control Registers

5.6.1 Overlay Control Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 40h to Graphics Controller Address Register location 3CE.

Bits	Function
7, 6	Color Key Control
5	DAC Color Mode Control
4 - 2	Input Data Color Mode
1, 0	Overlay Select

Bit 7, 6: Color Key Comparison Select. Bits 1 and 0 determine the Color Key equation when overlay with color key selected.
1 0 Color Key Equation
0 0 Overlay will occur when pixel data = color key
0 1 Overlay will occur when pixel data < color key
1 0 Overlay will occur when pixel data > color key
1 1 Reserved

Bit 5: DAC Color Mode Control.
Logical 1: When the overlay condition is true, the DAC will switch to the same color mode as the incoming data from the feature connector. When the overlay condition is false, the DAC will remain in the currently selected graphics mode.
Note: The color mode for the incoming feature connector data is defined by bits 4-2 of this register.
Logical 0: The DAC color mode will not switch for a true overlay condition.

Bit 4-2: Input Data Color Mode.
2 1 0 Color Mode
0 0 0 8-bit/pixel using CLUT
0 0 1 8-bit/pixel grayscale
0 1 0 8-bit RGB (3:3:2 format)
0 1 1 Reserved
1 0 0 15-bit RGB (5:5:5 format)
1 0 1 16-bit RGB (5:6:5 format)
1 1 0 Reserved
1 1 1 Reserved

Note For RGB (3:3:2) format, R=P7-P5, G=P4-P2, B=P1-P0.
For RGB (5:5:5) format, R=P14-P10, G=P9-P5, B=P4-P0.
For RGB (5:6:5) format, R=P15-P10, G=P9-P5, B=P4-P0.
Where P[x] is a given pixel data signal on the feature connector.

Note 8-bit feature connector option: For 15 and 16-bit RGB modes, data is clocked in at the rising and falling edge of DCLK. For all other modes, data is clocked in at the rising edge of DCLK.

Bits 1,0: Overlay Select. Selects overlay mode type.
1 0 Overlay Mode
0 0 Overlay disabled
0 1 Overlay using EVIDEO
1 0 Overlay with Color Key and EVIDEO
1 1 Overlay with Color Key

5.6.2 Color Key Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 41h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	8-bits of Color Key

Bits 7-0: 8-bits of Color Key. 8-bits of the color key value.

5.6.3 Color Key Mask Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 42h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	8-bits of Color Key Mask

Bits 7-0: 8-bits of Color Key. 8-bits of the color key mask. Each bit corresponds to a pixel on the screen. Pixel display is from Most Significant Bit to Least Significant Bit. A logical 1 causes the given pixel to be masked. Please note the following when programming the color key mask at particular color depths:
Pseudo-color: Load the color key mask to Color Key Mask Register 0.

5.6.4 Overlay Window Horizontal Start Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 45h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	Overlay Window Horizontal Start

Bits 7-0: Overlay Window Horizontal Start. Bits 10-3 of the overlay window horizontal start value. Bits 2-0 located in the Overlay Window Horizontal Pixel Alignment Register.

5.6.5 Overlay Window Horizontal End Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 46h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	Overlay Window Horizontal End

Bits 7-0: Overlay Window Horizontal Start. Bits10-3 of the overlay window horizontal start value. Bits 2-0 located in the Overlay Window Horizontal Pixel Alignment Register.

5.6.6 Overlay Window Horizontal Pixel Alignment Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 47h to Graphics Controller Address Register location 3CE.

Bits	Function
7	Reserved
6-4	Bits 2-0 of Overlay Window Horizontal End
3	Reserved
2-0	Bits 2-0 of Overlay Window Horizontal Start

Bit 7: Reserved.

Bits 6-4: Bits 2-0 of Overlay Window Horizontal End

Bit 3: Reserved.

Bits 2-0: Bits 2-0 of Overlay Window Horizontal Start

5.6.7 Overlay Window Vertical Start Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 48h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	Overlay Window Vertical Start

Bits 7-0: Overlay Window Vertical Start. Lower 8-bits of the overlay window vertical start value. Bits 8 and 9 are located in the Overlay Window Vertical Overflow Register.

5.6.8 Overlay Window Vertical End Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 49h to Graphics Controller Address Register location 3CE.

Bits	Function
7 - 0	Overlay Window Vertical End

Bits 7-0: Overlay Window Vertical End. Lower 8-bits of the overlay window vertical end value. Bits 8 and 9 are located in the Overlay Window Vertical Overflow Register.

5.6.9 Overlay Window Vertical Overflow Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 4Ah to Graphics Controller Address Register location 3CE.

Bits	Function
7-4	Reserved
3, 2	Bits 8 and 9 of Overlay Vertical Window End
1, 0	Bits 8 and 9 of Overlay Vertical Window Start

Bits 7-4: Reserved.

Bits 3, 2: Overlay Window Vertical End. Upper two bits of overlay window vertical end value.

Bits 1, 0: Overlay Window Vertical Start. Upper two bits of overlay window vertical end value.

5.6.10 Genlock Control Register

Read/Write Port: 3CF

Index: This register is accessed by writing a value of 4Bh to Graphics Controller Address Register location 3CE.

Bits	Function
7	Enable VSYNC Genlock
6	Enable HSYNC Genlock
5-3	Horizontal Total Adjust for HSYNC Genlock
2-0	Horizontal Sync Adjust for HSYNC Genlock

Bit 7: Enable VSYNC Genlock.
Logical 1: Enables VSYNC Genlock. VSYNC becomes an input to the 92C178 and is used to genlock the 92C178 to an external video source.
Logical 0: Disables VSYNC genlock.

Bit 6: Enable HSYNC Genlock.
Logical 1: Enables HSYNC genlock. HSYNC becomes an input to the 92C178 and is used to genlock the 92C178 to an external video source.
Logical 0: Disables HSYNC genlock.
To activate HSYNC genlock and VSYNC genlock at the same time, program bits 7,6 to a logical 1.

Bits 5-3: Horizontal Total Adjust for HSYNC Genlock. Allows adjustment of the Horizontal Total as follows:

5	4	3	Adjustment (VCLK)
0	0	0	No adjustment
0	0	1	-4
0	1	0	-3
0	1	1	-2
1	0	0	-1
1	0	1	+1
1	1	0	+2
1	1	1	+3

Bits 2-0: Horizontal Sync Adjust for HSYNC Genlock. Allows adjustment of Horizontal Sync Start (relative to BLANK#) as follows:

2	1	0	Adjustment (VCLK delay)
0	0	0	No adjustment
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

5.7 PCI Configuration Space Description

Table 5-15 shows the header region of the 92C178's PCI configuration space. An explanation of each of the registers within the header follows the table.

Table 5-15 Configuration Space Layout

Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision	08h
BIST	Header Type	Latency Timer	Cache Line Size	0h
Base Address Registers				10h 14h 18h 1Ch 20h 24h
Reserved				28h
Reserved				2Ch
Expansion ROM Base Address				30h
Reserved				34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch

A description of each of the PCI Configuration Space Registers follows. For clarity, the registers have been grouped by function type. Five categories are listed: Device Identification, Device Control, Device Status, Other Functions, and Base Address.

5.7.1 Device Identification

5.7.1.1 Vendor ID Register (read only)

Byte location within the Configuration Space Header: 00h-01h

Bits	Function
15-0	Vendor ID Code

Bits 15-0: Vendor ID Code. The Vendor ID code identifies OPTi as the manufacturer of the 92C178. This code is assigned by the PCI SIG. The assigned Vendor ID code for OPTi is 1045h.

5.7.1.2 Device ID Register (read only)

Byte location within the Configuration Space Header: 02h-03h

Bits	Function
15-0	Device ID Code

Bits 15-0: Device ID Code. The Device ID code identifies the 92C178. This code is assigned by OPTi. The Device ID code for OPTi is C178h.

5.7.1.3 Revision ID Register (read only)

Byte location within the Configuration Space Header: 08h

Bits	Function
7-0	Revision ID Code

Bits 7-0: Revision ID Code. The Revision ID code indicates the revision number of the 92C178.

5.7.1.4 Header Type Register (read only)

Byte location within the Configuration Space Header: 0Eh

Bits	Function
7	Single/Multi-function Device
6-0	Configuration Space Layout

Bit 7: Single/Multi-function Device. This bit is set to a logical 0 which indicates a single function device.

Bits 6-0: Configuration Space Layout. Defines layout for bytes 10h and up of the PCI configuration space header. The 92C178 supports a 00h Header Type.

5.7.1.5 Class Code Register (read only)

Byte location within the Configuration Space Header: 09h - 11h

Bits	Function
23-16	Base Class Code
15-8	Sub-Class Code
7-0	Programming Interface Identifier

Bits 23-16: Base Class Code. Defines type of function the 92C178 performs. The Base Class Code Value is 03h, which identifies the 92C178 as a Display Controller.

Bits 15-8: Sub-Class Code. Defines the Display Controller type for 92C178. The Sub-Class Code value is 00h, which identifies the 92C178 as a VGA Compatible Controller or 8514 Compatible Controller.

Bits 7-0: Programming Interface Identifier. Defines the programming interface for the 92C178. The Programming Interface Identifier value is 00h, which identifies the programming interface as that of a VGA Compatible Controller.

5.7.2 Device Control

5.7.2.1 Command Register

Byte location within the Configuration Space Header: 04h - 05h

Bits	Function
15-7	Reserved
6	Parity Error Response
5	VGA Palette Snoop
4	Reserved
3	Special Cycles
2	Bus Master
1	Memory Space
0	I/O Space

When a value of 0h is written to this register, the 92C178 will not respond to any PCI bus accesses except for Configuration Space accesses. Definitions of the individual bits within the Command Register follow:

Bits 15-7: Reserved. Returns a logical 0 when read.

Bit 6: Parity Error Response. This bit is set to a logical 0. A logical 0 means the 92C178 will ignore any parity errors it detects and continue normal operations.

Bit 5: VGA Palette Snoop. Enables/Disables palette snooping.
Logical 1: Enables palette snooping.
Logical 0: Disables palette snooping.

Bit 4: Reserved. Returns a logical 0 when read.

Bit 3: Special Cycles. Special Cycle control. This bit is set to a logical 0. A logical 0 means the 92C178 will ignore all Special Cycle operations.

Bit 2: Bus Master. Since the 92C178 is not a bus master, this bit is set to a logical 0. A logical 0 disables the 92C178 from generating PCI accesses.

Bit 1: Memory Space. Enables/Disables the 92C178's response to memory accesses.
Logical 1: Enables response to memory accesses.
Logical 0: Disables response to memory accesses (default after RESET#).

Bit 0: I/O Space. Enables/Disables the 92C178's response to I/O accesses.
Logical 1: Enables response to I/O accesses.
Logical 0: Disables response to I/O accesses (default after RESET#).

5.7.3 Device Status

5.7.3.1 Command Register

Byte location within the Configuration Space Header: 06h - 07h

Bits	Function
15-11	Reserved
10-9	DEVSEL# Timing
8	Reserved
7	Fast Back-to-Back Capable
6-0	Reserved

Bit 15-11: Reserved. Returns a logical 0 when read.

Bit 10-9: DEVSEL# Timing. These bits are set to 01b and are read only. The value indicates that DEVSEL# will be asserted a maximum of two clock cycles after the address phase.

Bit 8: Reserved. Returns a logical 0 when read.

Bit 7: Fast Back-to-Back Capable. This bit is set to a logical 0. A logical 0 indicates the 92C178 does not support Fast Back-to-Back transactions which are not to the same agent.

Bit 6-0: Reserved. Returns a logical 0 when read.

5.7.4 Other Functions

The following registers in this functional group are reserved:

- Cache Line Size Register - byte location 0Ch in the Configuration Space Header
- Latency Timer Register - byte location 0Dh in the Configuration Space Header
- BIST Register - byte location 0Fh in the Configuration Space Header
- MIN_GNT Register - byte location 3Eh in the Configuration Space Header
- MAX_LAT Register - byte location 3Fh in the Configuration Space Header

All of the above registers return 00h when read.

The following interrupt registers are also in this functional group.

5.7.4.1 Interrupt Line Register

Byte location within the Configuration Space Header: 3Ch

Bits	Function
7-0	Interrupt Line Routing Information

Bits 7-0: Interrupt Line Routing Information. Value in this register indicates which system interrupt pin the 92C178's interrupt pin is connected to. POST software will write the routing information to the Interrupt Line Register as the system is initialized and configured. The value in this register depends on the system architecture.

5.7.4.2 Interrupt Pin Register (read only)

Byte location within the Configuration Space Header: 3Dh

Bits	Function
7-0	Interrupt Pin Information

Bits 7-0: Interrupt Pin Information. The value in this register indicates which interrupt pin the 92C178 uses. For 92C178, the value in this register is 01h, which corresponds to INTA#.

5.7.5 Base Address Registers

The following Base Address Register locations are reserved:

- Base Address Location 18h - Reserved
- Base Address Location 1Ch - Reserved
- Base Address Location 20h - Reserved
- Base Address Location 24h - Reserved

Definitions of the remaining Base Address Register locations follow:

5.7.5.1 Base Address Register Location 10h

Bits	Function
31-2	I/O Space Base Address
1	Reserved
0	I/O Space Indicator

Bits 31-16: Bits 31-16: Hardwired to logical 0.

Bits 15-12: These bits are writable. Gives 4K address space.

Bits 11-2: Hardwired to logical 0.

Bit 1: Reserved. Returns a logical 0 when read.

Bit 0: I/O Space Indicator. This bit is hardwired to a logical 1. A logical 1 indicates this is the base address for an I/O space.

5.7.5.2 Base Address Register Location 14h

Bits	Function
31-4	Memory Space Base Address
3	Prefetchable
2-1	Type
0	Memory Space Indicator

Bits 31-22: Bits 31-22: These bits are writable. Gives 4M address space.

Bits 21-4: Hardwired to logical 0.

Bit 3: Prefetchable. This bit is a logical 0 for the 92C178. A logical 0 indicates the video memory space is not prefetchable.

Bits 2-1: Type. These bits are set to 00b for the 92C178. This value indicates the defined 4M memory space may be located anywhere within the 32-bit address space.

Bit 0: Memory Space Indicator. This bit is hardwired to a logical 0. A logical 0 indicates this is the base address for an memory space.

5.7.5.3 Expansion ROM Base Address Register

Byte location within the Configuration Space Header: 30h - 33h

Bits	Function
31-11	Expansion ROM Base Address
10-1	Reserved
0	Address Decode Enable

Bits 31-22: Bits 31-22: These bits are writable. Gives 4M address space.

Bits 21-11: Logical 0.

Bits 10-1: Reserved. These bits will return a logical 0 value when read.

Bit 0: Address Decode Enable. A logical 1 enables access to the expansion ROM base address. Note: Bit 1 in the Command Register must also be set to a logical 1 to enable access to the expansion ROM base address.

6.0 Electrical Specification

6.1 DC Specifications

Table 6-1 DC Drive Characteristics and Buffer Power Source Information - Preliminary

Pin Number	Pin Name	I/O	Power Source of Buffer	Iol/Ioh (mA)	Notes
1-3	MD26-MD24	I/O	MVDD	8/-8	
4	WE3#	O	MVDD	8/-8	
5-6	MD23-MD22	I/O	MVDD	8/-8	
7	MVDD	--	--	--	DRAM interface power
8-13	MD21-MD16	I/O	MVDD	8/-8	
14	WE2#	O	MVDD	8/-8	
15	GND	--	--	--	Digital ground
16-24	MD15-MD8	I/O	MVDD	8/-8	
25	WE1#	O	MVDD	8/-8	
26	RAS0#	O	MVDD	8/-8	
27	RAMCNF/ CKEYW	I/O	MVDD	8/-8	
28	CAS#	O	MVDD	8/-8	
29	GND	--	--	--	Digital ground
30-37	MD7-MD0	I/O	MVDD	8/-8	
38	WE0#	O	MVDD	8/-8	
39	MVDD	--	--	--	DRAM interface power
40-42	MA0-MA2	O	MVDD	8/-8	
43	GND	--	--	--	Digital ground
44-50	MA3-MA9	O	MVDD	8/-8	
51	AGNDM	--	--	--	Analog gound for MCLK
52	MLF	--	AVDDM	--	--
53	AVDDM	--	--	--	Analog power for VCLK
54	CVDD	--	--	--	VGA core power
55-61	LA23-LA17: ISA A23-A17: VL Reserved: PCI	I	HVDD	--	TTL level input buffer
62-65	SA16-SA13: ISA A17-A13:VL Reserved: PCI	I	HVDD	--	TTL level input buffer
66	GND	--	--	--	Digital ground
67-75	SA12-SA4: ISA A12-A4: VL Reserved: PCI	I	HVDD	--	TTL level input buffer

Table 6-1 DC Drive Characteristics and Buffer Power Source Information - Preliminary (cont.)

Pin Number	Pin Name	I/O	Power Source of Buffer	Iol/Ioh (mA)	Notes
76	SA3: ISA A3: VL PAR: PCI	I/O	HVDD	8/-8	
77	SA2: ISA A2: VL STOP#: PCI	I/O	HVDD	8/-8	
78-79	SA1-SA0: ISA BE2#, BE0#: VL C/BE2#, C/BE0#: PCI	I	HVDD	--	TTL level input buffer
80	HVDD	--	--	--	VGA core power
81	Reserved: ISA BE3#: VL C/BE3#: PCI	I	HVDD	--	TTL level input buffer
82	SBHE#: ISA BE1#: VL C/BE1#: PCI	I	HVDD	--	TTL level input buffer
83	BALE: ISA ADS#: VL FRAME#: PCI	I	HVDD	--	TTL level input buffer
84	IOR#: ISA W/R#: VL Reserved: PCI	I	HVDD	--	TTL level input buffer
85	IOW#: ISA ID1/P0: VL, PCI	I/O	HVDD	8/-8	
86	MRD#: ISA M/IO#: VL IDSEL: PCI	I	HVDD	--	TTL level input buffer
87	MWR#: ISA VL#/P1: VL P1: PCI	I/O	HVDD	8/-8	
88	Reserved: ISA D/C#: VL Reserved: PCI	I	HVDD	8/-8	
89	GND	--	--	--	Digital ground
90	Reserved: ISA RDYRTN#: VL IRDY#: PCI	I	HVDD	--	TTL level input buffer
91	Reserved: ISA P2: VL, PCI	I/O	HVDD	8/-8	
92	ATBUS#: ISA ATBUS#/P3: VL, PCI	I/O	HVDD	8/-8	
93	CPUCLK	I	HVDD	--	TTL level input buffer
94	CVDD	--	--	--	VGA core power

Table 6-1 DC Drive Characteristics and Buffer Power Source Information - Preliminary (cont.)

Pin Number	Pin Name	I/O	Power Source of Buffer	Iol/Ioh (mA)	Notes
95	S46E8: ISA S46E8/P4: VL, PCI	I/O	HVDD	8/-8	
96	MCS16#: ISA LBS16#/P5: VL P5: PCI	I/O	HVDD	8/-8	
97	IOCS16#: ISA LDEV#: VL DEVSEL#: PCI	O	HVDD	16/-16	
98	IOCHRDY: ISA RDY#: VL TRDY#: PCI	O	HVDD	16/-16	
99	Reserved: ISA A24: VL Reserved: PCI	I	HVDD	--	TTL level input buffer
100	IRQ: ISA A25: VL INTA#: PCI	I/O	HVDD	8/-8	
101	GND	--	--	--	Digital ground
102	ZWS#: ISA P6: VL, PCI	I/O	HVDD	8/-8	
103	EROM#: ISA EROM#/P7: VL P7: PCI	I/O	HVDD	8/-8	
104	Reserved: ISA D31: VL AD31: PCI	I/O	HVDD	8/-8	
105-106	Reserved: ISA D30-D29: VL AD30-AD29: PCI	I/O	HVDD	8/-8	
107	HVDD	--	--	--	Bus interface power
108-117	Reserved: ISA D28-D19: VL AD28-AD19: PCI	I/O	HVDD	8/-8	
118	GND	--	--	--	Digital ground
119-121	Reserved: ISA D18-D16: VL AD18-AD16	I/O	HVDD	8/-8	
122	HVDD	--	--	--	Bus interface power
123-130	SD15-SD8: ISA D15-D8: VL AD15-AD8: PCI	I/O	HVDD	8/-8	
131	GND	--	--	--	Digital ground

Table 6-1 DC Drive Characteristics and Buffer Power Source Information - Preliminary (cont.)

Pin Number	Pin Name	I/O	Power Source of Buffer	Iol/Ioh (mA)	Notes
132	SDBUS16: ISA SDBUS16/ECLK: VL, PCI	I	HVDD	--	TTL level input buffer
133	VPLF	--	AVDDV	--	
134	AVDDV	--	--	--	Analog voltage for VCLK
135	VLF	I/O	AVDDV	--	
136	AGNDV	--	--	--	Analog ground for VCLK
137-144	SD7-SD0: ISA A7-A0: VL AD7-AD0: PCI	I/O	HVDD	8/-8	
145	HVDD	--	--	--	Bus interface power
146	AEN: ISA CPURST#/EVIDEO: VL EVIDEO: PCI	I/O	MVDD	8/-8	
147	RESET: ISA RESET#: VL, PCI	I	MVDD	--	TTL level input buffer
148	REFRSH#: ISA ID0/ESYNC: VL, PCI	I	HVDD	--	TTL level input buffer
149	HVDDSEL: ISA HVDDSEL/BLANK#: VL, PCI	I/O	HVDD	8/-8	
150	GND	--	--	--	Digital gournd
151	XCLK	I	MVDD	--	High speed input buffer
152	CVDD	--	--	--	VGA core power
153	RVDD	--	--	--	RAM (from DAC) power
154	VREF	I	VAA	--	Analog input
155	FADJ	I	VAA	--	Analog input
156	GND	--	--	--	Digital ground
157	B	O	VAA	--	Analog output
158	G	O	VAA	--	Analog output
159	R	O	VAA	--	Analog output
160	VGNDA	--	--	--	Analog ground for DAC
161	VSYNC	I/O	CVDD	8/-8	
162	HSYNC	I/O	CVDD	8/-8	
163	VAA	--	--	--	Analog power for DAC
164	INOSC	I	MVDD	--	TTL level input buffer
165	GND	--	--	--	Digital ground
166	PWDPAN	O	PVDD	8/- 8	
167	PANBIAS	O	PVDD	8/-8	
168	PANLGT	O	PVDD	8/-8	

Table 6-1 DC Drive Characteristics and Buffer Power Source Information - Preliminary (cont.)

Pin Number	Pin Name	I/O	Power Source of Buffer	Iol/Ioh (mA)	Notes
169	PVDD	–	–	–	Panel interface power
170	PWRCLK	O	MVDD	8/-8	
171	STANDBY	I/O	MVDD	8/-8	
172	ACTIVITY	I	PVDD	–	TTL level input buffer
173	SUSPEND	I	MVDD	–	TTL level input buffer
174-179	LD0-LD5	O	PVDD	8/-8	
180	GND	–	–	–	Digital ground
181-184	LD6-LD7,UD0-UD1	O	PVDD	8/-8	
185	PVDD	–	–	–	Panel interface power
186-191	UD2-UD7	O	PVDD	8/-8	
192-193	TFT16-TFT17	O	PVDD	8/-8	
194	GND	–	–	–	Digital ground
195	SCK	O	PVDD	16/-16	
196	M	O	PVDD	16/-16	
197	LP	O	PVDD	8/-8	
198	FLM	O	PVDD	8/-8	
199	DTMG	O	PVDD	16/-16	
200	CVDD	–	–	–	VGA core power
201	OE#/RAS1#	O	MVDD	8/-8	
202	MVDD	–	–	–	Memory interface power
203-205	MD31-MD29	I/O	MVDD	8/-8	
206	GND	–	–	–	Digital ground
207-208	MD28-MD27	I/O	MVDD	8/-8	

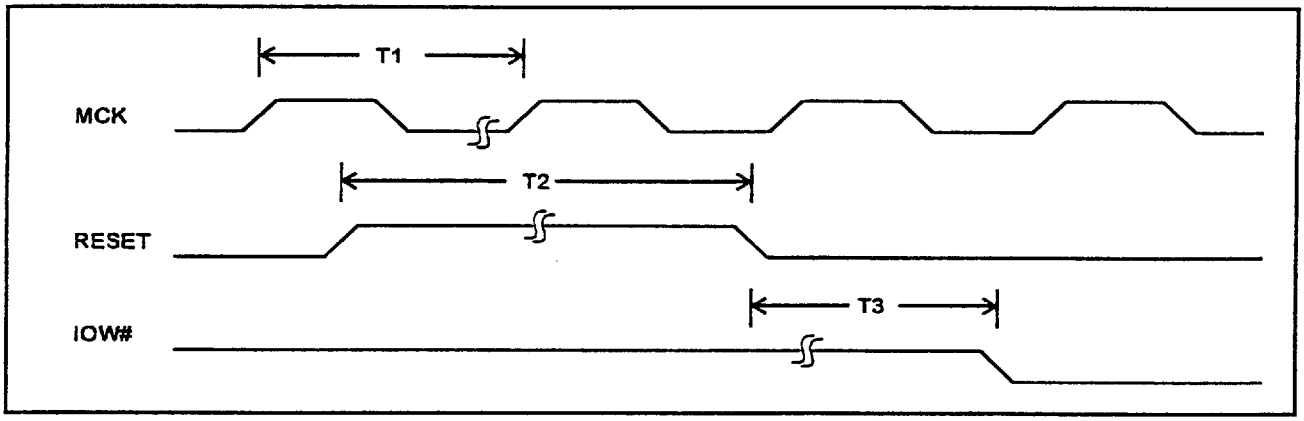
6.2 Internal DAC Specifications

Table 6-2 Internal DAC Specifications

Symbol	Parameter	Min.	Typical	Max.	Units	Notes
	DAC Resolution	8	8	8	bits	
IL	Integral Linearity Error	–	–	1/2	LSB	
DL	Differential Linearity Error	–	–	1/2	LSB	
	White Level Relative to Black	–	14.0	–	mA	VREF = 1.22V RSET = 690Ωs
	LSB Size	–	55	–	µA	VREF = 1.22V RSET = 690Ωs
RSET	FADJ Resistor Value	–	690	–	ohms	50Ω load
RL	Output Load	–	50	–	ohms	
VREF	Voltage Reference	–	1.22	–	volts	

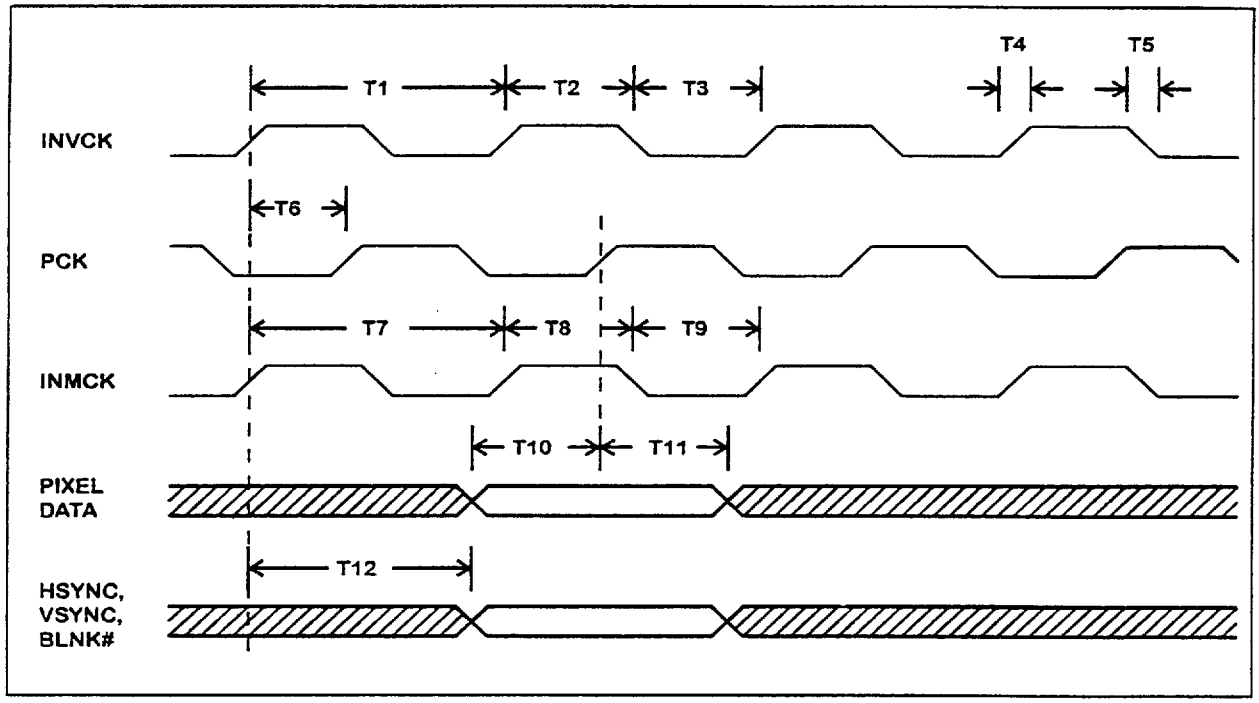
6.3 AC Timing Characteristics

Figure 6-1 Clock and Reset Timing



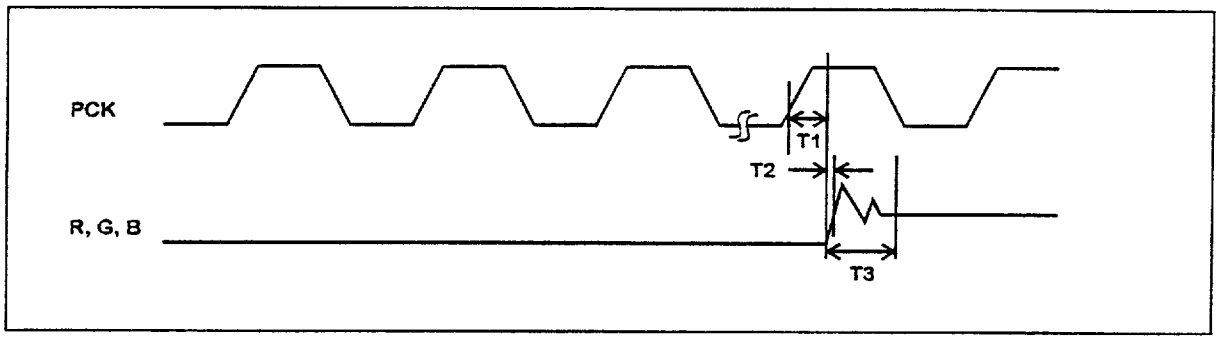
Symbol	Description
T1	50MHz
T2	16Ti
T3	16Ti

Figure 6-2 Clock and Video Timing



Symbol	Description	Min (ns)	Max (ns)
T1	INVCK Period	14	
T2	INVCK High	5	
T3	INVCK Low	5	
T4	INVCK Rise Time		2
T5	INVCK Fall Time		2
T6	PCK to INVCK Delay	7	
T7	INMCK Period	20	
T8	INMCK High	9	
T9	INMCK Low	9	
T10	Pixel Data Setup to PCK	4	
T11	Pixel Data Hold from PCK	8	
T12	HSYNC, VSYNC to INVCK Delay		

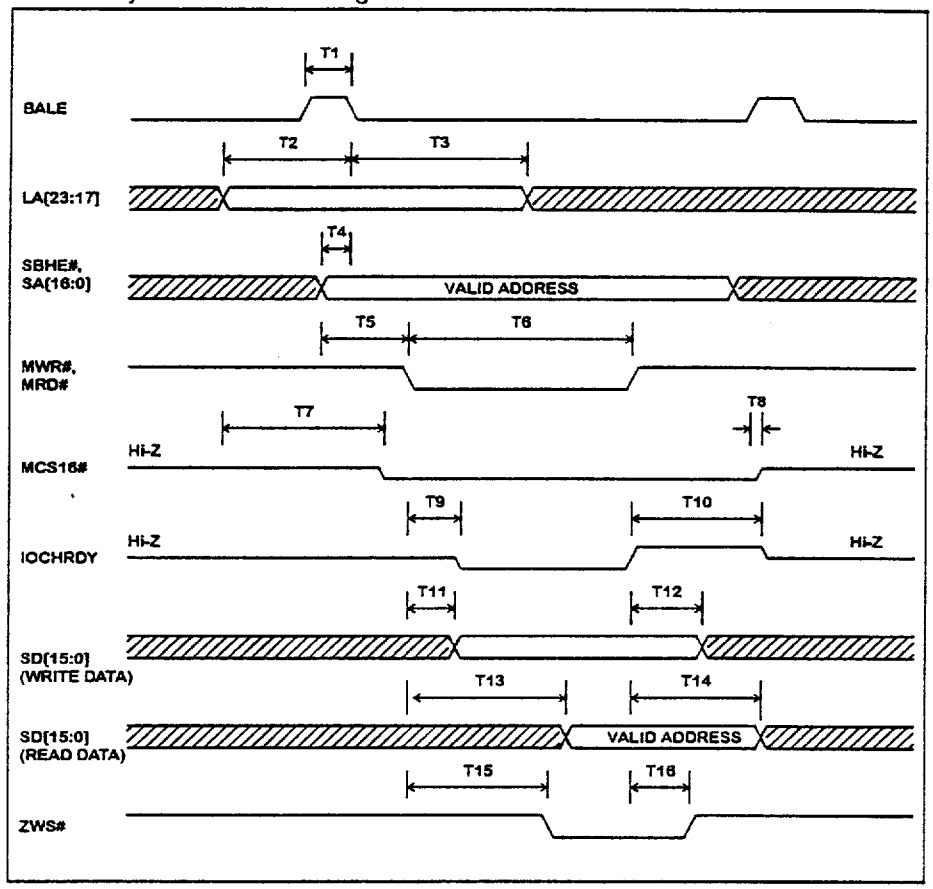
Figure 6-3 RAMDAC Timing (Analog Outputs)



Symbol	Description	Min (ns)	Typ (ns)	Max (ns)
T1	Analog Output Delay	–	6	TBD
T2	Analog Output Rise/Fall Time[a]	–	3/8	TBD
T3	INVCK Low	–	12	TBD

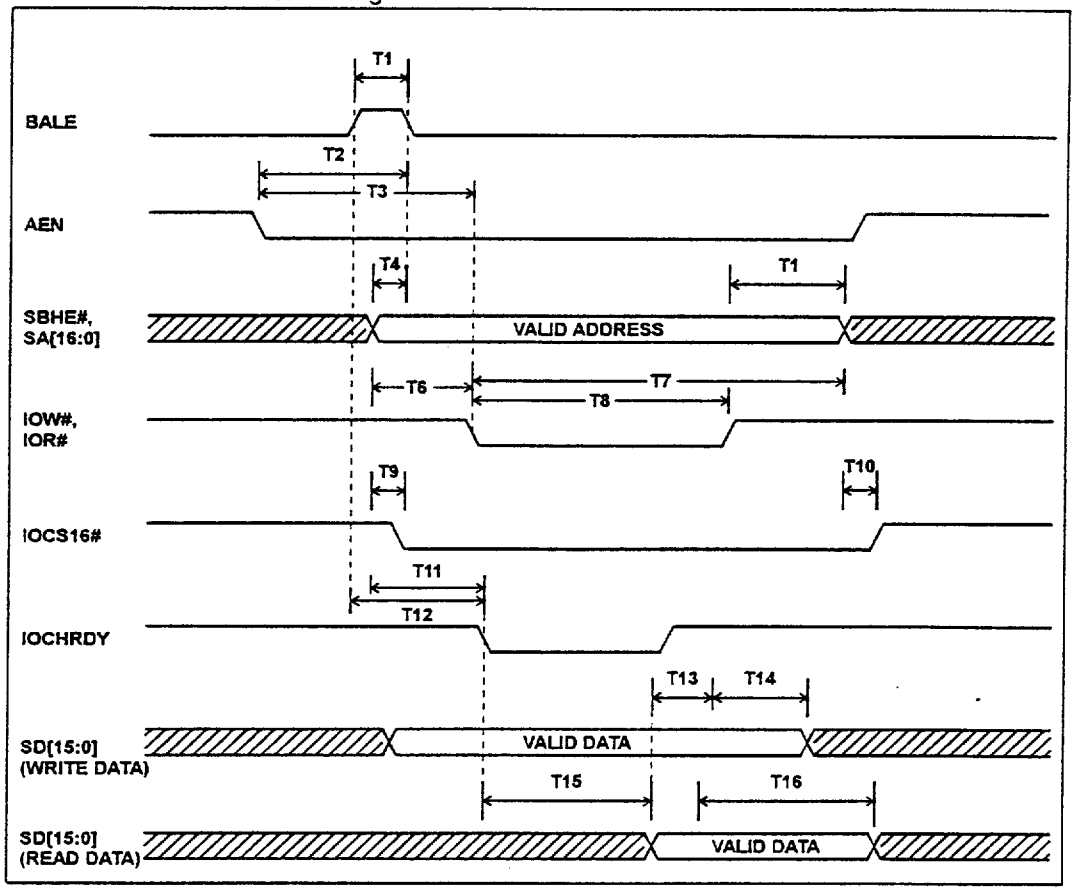
a. Defined as 10% to 90% of final value.

Figure 6-4 ISA-Bus Memory Read/Write Timing



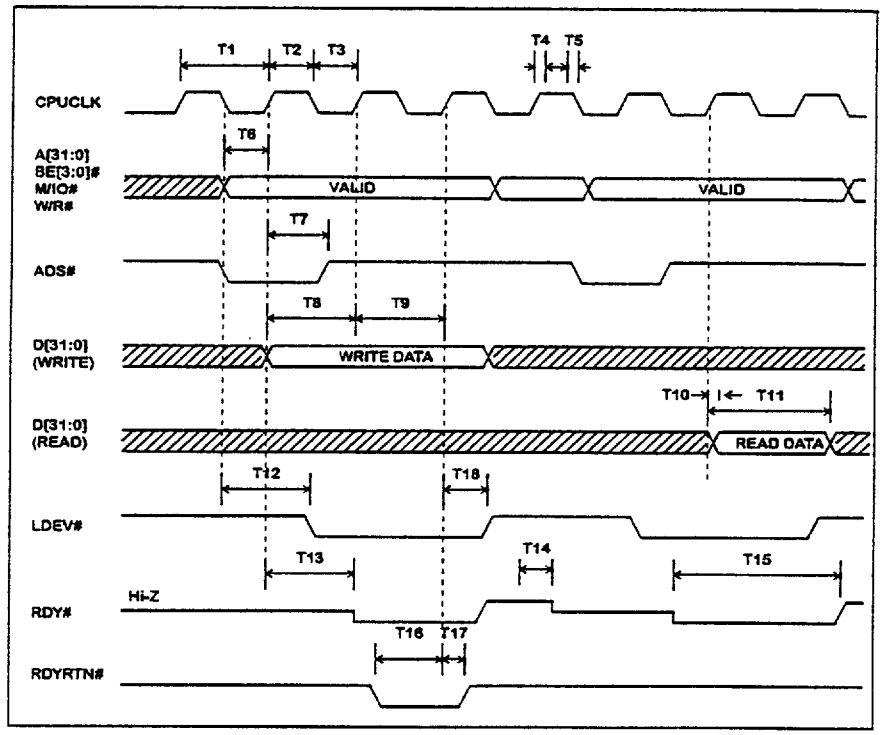
Symbol	Description	Min (ns)	Max (ns)
T1	BALE Pulse Width	30	
T2	LA[23:17] Valid to BALE Low	80	
T3	BALE Low to LA[23:17] Invalid	30	
T4	SA[16:0]Setup to BALE Low	20	
T5	SA[16:0], SBHE# Setup to MWR#, MRD#	30	
T6	MWR#, MRD# Pulse Width	80	
T7	LA[23:17] Vaiid to MCS16# Low		45
T8	MCS16# Tristate to Next Active BALE		40
T9	IOCHRDY Low from MWR#, MRD# Low		30
T10	IOCHRDY High to Tristate after MWR#, MRD# High		30
T11	MWR# Low to Write Data Valid		25
T12	Write Data Hold after MWR# High	15	
T13	Read Data Valid after MRD# Low		45
T14	Read Data Hold after MRD# High		45
T15	MWR#, MRD# Low to ZWS# Low		20
T16	ZWS# Hold After MWR#, MRD# Tristate	15	

Figure 6-5 ISA-Bus I/O Read/Write Timing



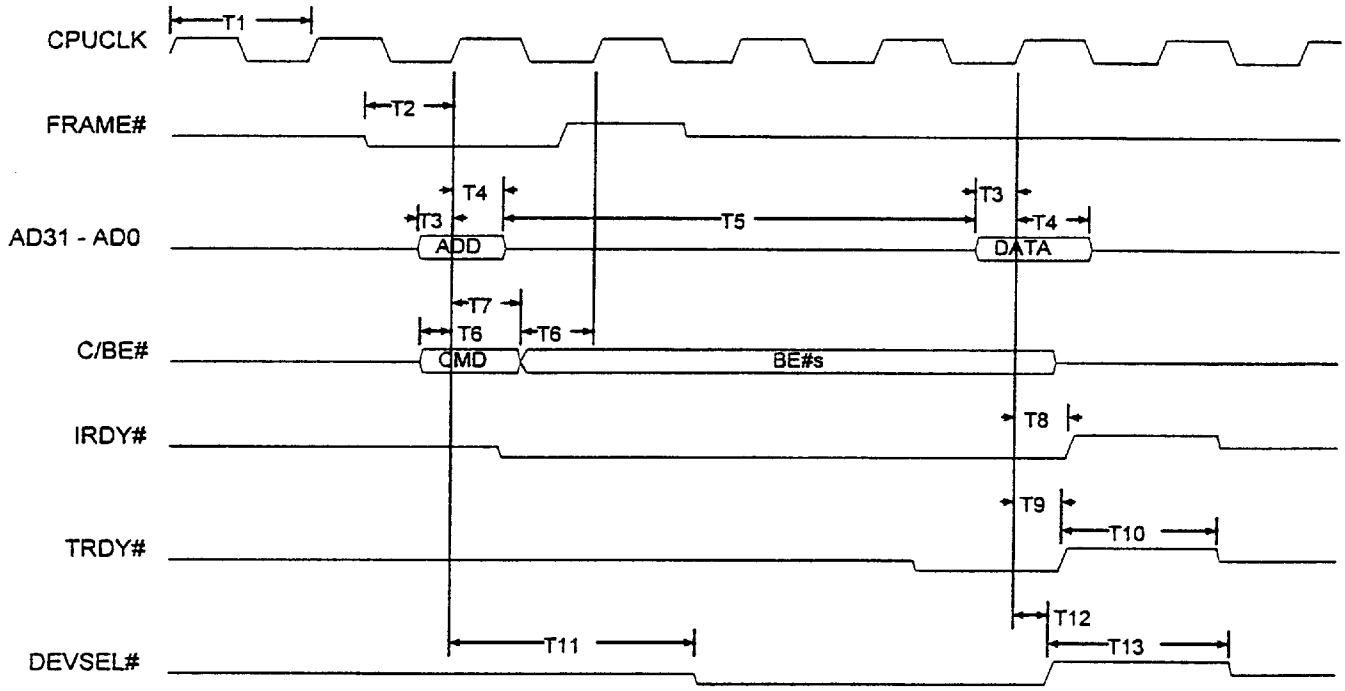
Symbol	Description	Min (ns)	Max (ns)
T1	BALE High Pulse Width	30	
T2	AEN Low to BALE Low	75	
T3	AEN Setup to IOW#, IOR# Low	20	
T4	A[16:0], SBHE# Setup to ALE Low	20	
T5	IOR#, IOW# High before AEN High	10	
T6	SA[16:0], SBHE# Setup before IOR#, IOW# Low	65	
T7	SA[16:0], SBHE# Hold after IOR#, IOW# Low	115	
T8	IOR#, IOW# Pulse Width	100	
T9	SA[16:0], SBHE# Valid to IOCS16# Active		25
T10	IOCS16# Invalid to Address Invalid	20	
T11	SA[16:0], SBHE# Valid to IOCHRDY Active		95
T12	BALE High to IOCHRDY Active		100
T13	Data Setup to IOW# High	20	
T14	Data Hold to IOW# High	10	
T15	Read Data Valid to IOR# Low		220
T16	Read Data Hold to IOR# High	10	

Figure 6-6 VL-Bus Interface Timing



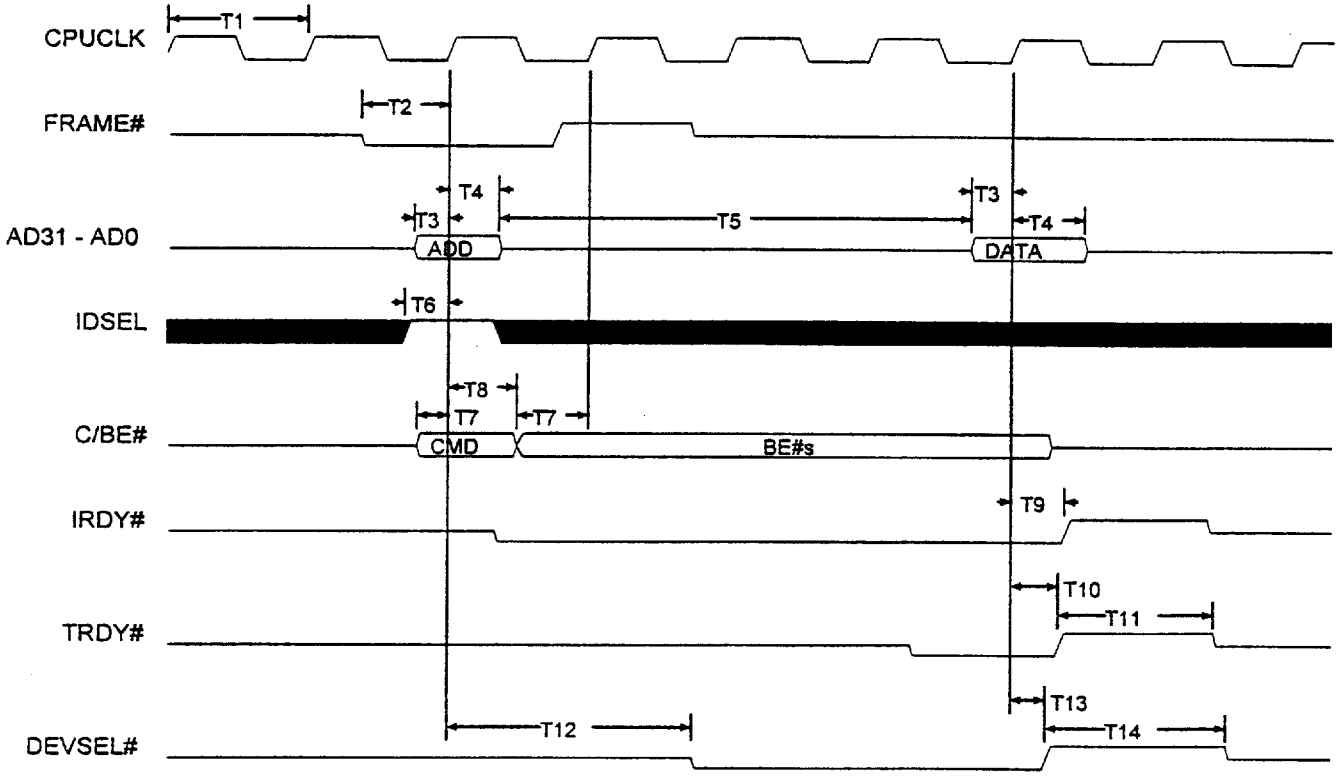
Symbol	Description	Min (ns)	Max (ns)
T1	CPUCLK Period	30	
T2	CPUCLK High	13	
T3	CPUCLK Low	13	
T4	CPUCLK Rise Time	2	
T5	CPUCLK Fall Time	2	
T6	ADS#, A[31:0]#, BE[3:0]#, M/IO#, W/R# to CPUCLK Setup Time	6	
T7	ADS#, A[31:0]#, BE[3:0]#, M/IO#, W/R# from CPUCLK Hold Time	5	
T8	D[31:0] to CPUCLK Setup Time	10	
T9	D[31:0] from CPUCLK Hold Time	5	
T10	CPUCLK to D[31:0] Output		15
T11	CPUCLK to D[31:0] Tristate	5	
T12	A[31:2], BE[3:0]#, M/IO#, W/R#, to LDEV# Low		20
T13	ADS# Low, CPUCLK to RDY# Low		14
T14	CPUCLK to RDY# Hi-Impedance	5	
T15	RDY# Low to High	20	
T16	RDYRTN# to CPUCLK Setup before ADS# Low	6	
T17	RDYRTN# from CPUCLK Hold before ADS# Low	3	
T18	LDEV# Delay from CPUCLK		20

Figure 6-7 Basic Read/Write Operation (PCI)



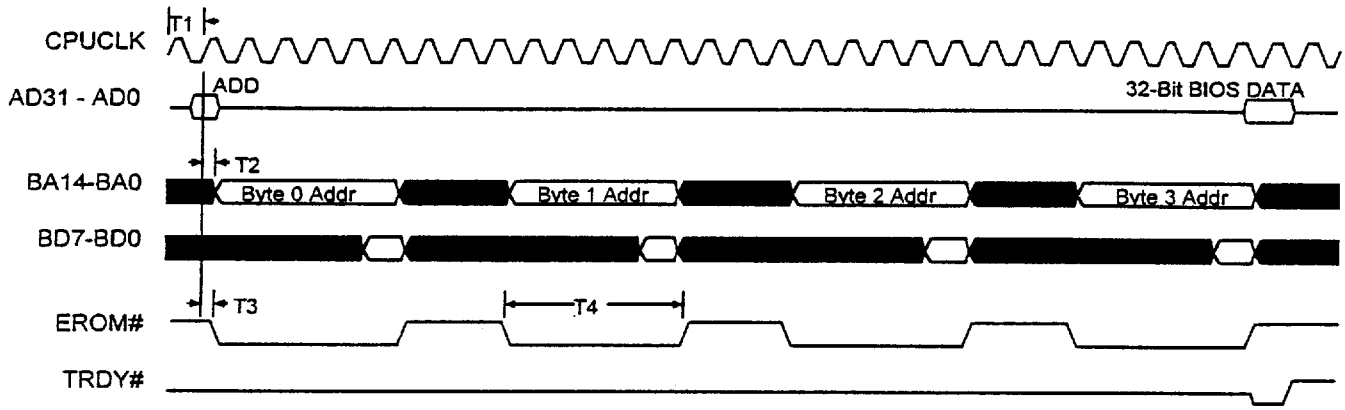
Symbol	Description	Min (ns)	Max (ns)
T1	CPUCLK Period	30	
T2	FRAME# setup to CPUCLK	7	
T3	Address/Data setup to CPUCLK	7	
T4	Address/Data hold from CPUCLK	0	
T5	Address Phase to Data Phase		4T
T6	Bus Command setup to CPUCLK	7	
T7	Bus Command hold from CPUCLK	0	
T8	IRDY# hold from CPUCLK	0	
T9	TRDY# delay from CPUCLK	2	
T10	TRDY# high before HI-Z	1T	
T11	Address Phase to DEVSEL#		2T
T12	DEVSEL# delay from CPUCLK	2	
T13	DEVSEL# delay from CPUCLK	1T	

Figure 6-8 Configuration Read/Write Operation (PCI)



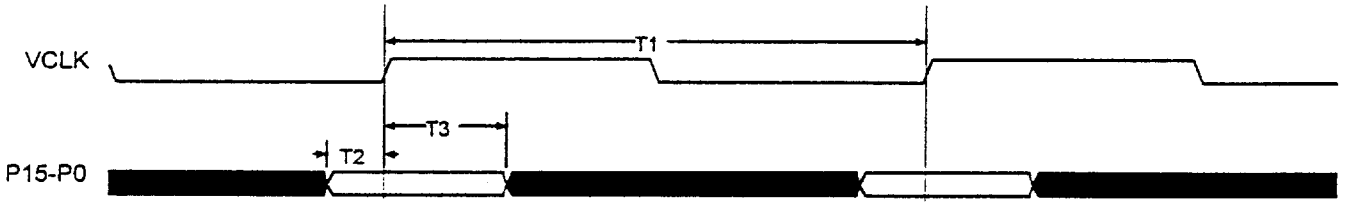
Symbol	Description	Min (ns)	Max (ns)
T1	CPUCLK Period	30	
T2	FRAME# setup to CPUCLK	7	
T3	Address/Data setup to CPUCLK	7	
T4	Address/Data hold from CPUCLK	0	
T5	Address Phase to Data Phase		4T
T6	IDSEL setup to CPUCLK	7	
T7	Bus Command setup to CPUCLK	7	
T8	Bus Command hold from CPUCLK	0	
T9	IRDY# hold from CPUCLK	0	
T10	TRDY# delay from CPUCLK	2	
T11	TRDY# high before HI-Z	1T	
T12	Address Phase to DEVSEL#		2T
T13	DEVSEL# delay from CPUCLK	2	
T14	DEVSEL# high before HI-Z	1T	

Figure 6-9 BIOS Access Operation (PCI)



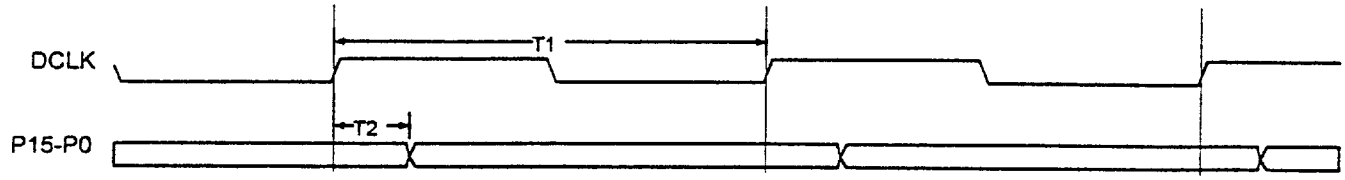
Symbol	Description	Min (ns)	Max (ns)
T1	CPUCLK Period	30	
T2	Byte Address delay from CPUCLK		6T
T3	EROM# delay from CPUCLK		6T
T4	EROM# active	160	

Figure 6-10 Pixel Data In Timing



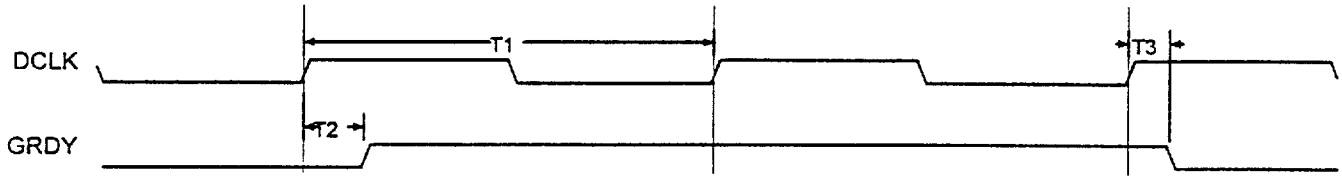
Symbol	Description	Min (ns)	Max (ns)
T1	VCLK Period	26.6	
T2	Pixel Data setup to VCLK	8	
T3	Pixel Data hold from VCLK	1.2	

Figure 6-11 Pixel Data Out Timing



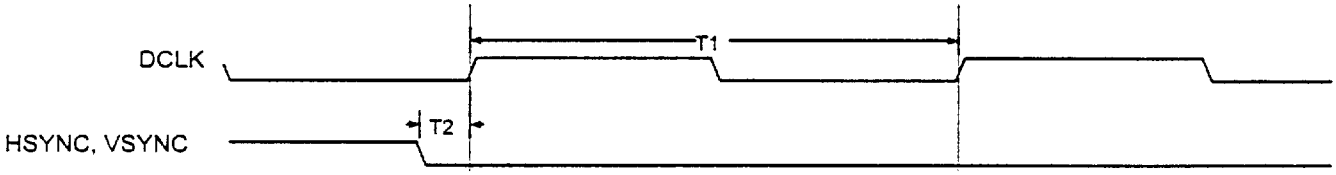
Symbol	Description	Min (ns)	Max (ns)
T1	DCLK Period	26.6	
T2	Pixel data delay from DCLK	5	

Figure 6-12 GRDY Timing



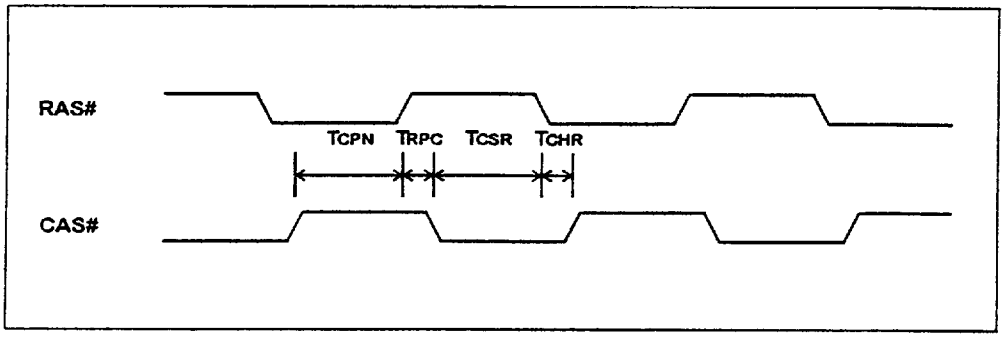
Symbol	Description	Min (ns)	Max (ns)
T1	DCLK Period	26.6	
T2	GRDY delay from DCLK	5	
T3	GRDY inactive from DCLK	5	

Figure 6-13 Genlock Timing



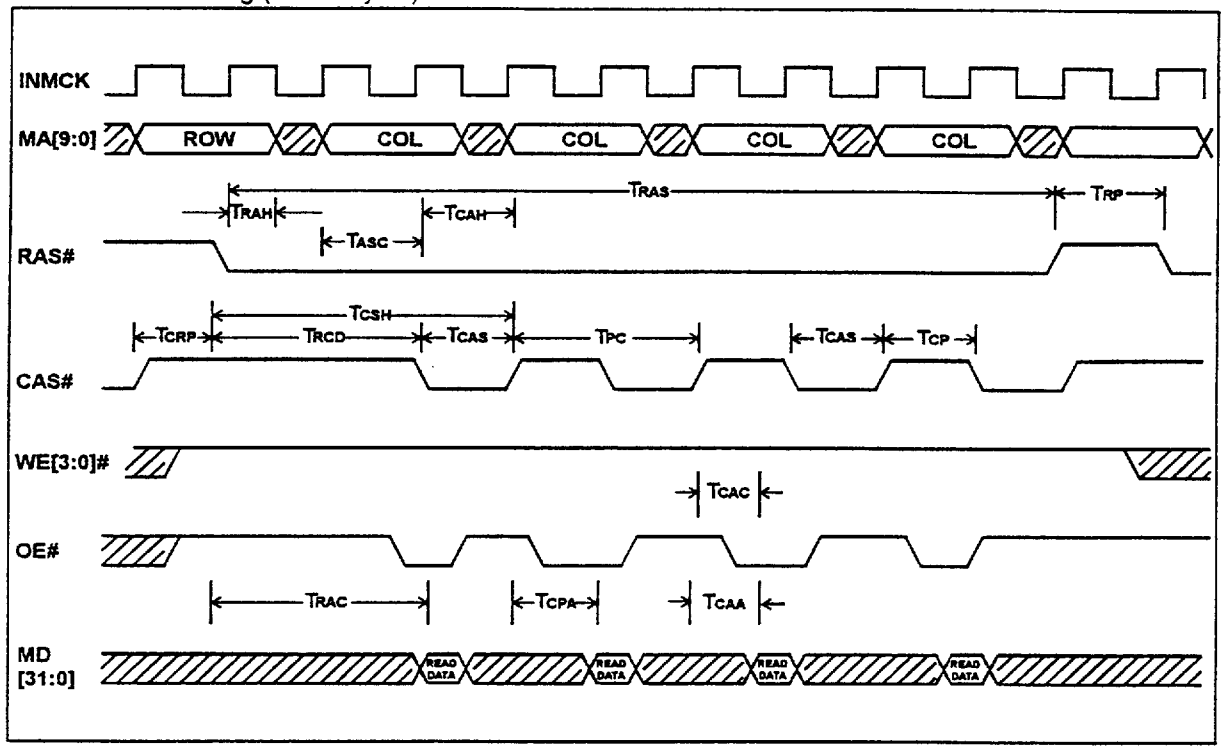
Symbol	Description	Min (ns)	Max (ns)
T1	DCLK Period	26.6	
T2	Sync setup to DCLK	5	

Figure 6-14 CAS Before RAS DRAM Timing



Symbol	Description	Min (ns)
INMCK	1/T	
TCPN	CAS# Precharge Time	T + 3.5
TRPC	RAS# High to CAS High Precharge	T + 4
TCSR	CAS# before RAS Setup Time	2T - 1.5
TCHR	CAS# before RAS Hold Time	3T + 6

Figure 6-15 DRAM Timing (Read Cycle)

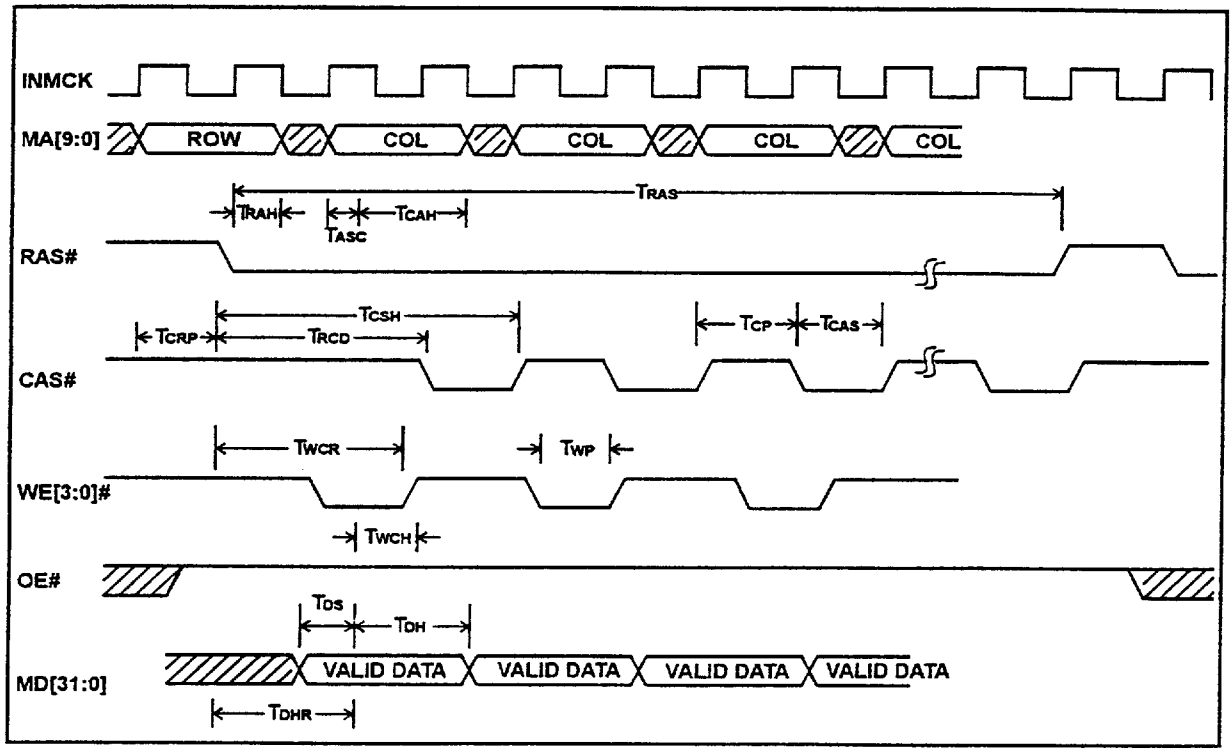


NOTE Display Memory Fast Page Mode Parameters

Symbol	Description	Min (ns)	Max (ns)
TRAH	Row Address Hold Time	T-4.5	
TASC	Column Address Setup	T-1	
TCAH	Column Address Hold Time	T-1	
TRAS	RAS# Pulse Width	5T-8	
TRP	RAS# Precharge Time	4T+1	
TCRP	CAS# to RAS# Precharge Time	4T+1	
TRCD	RAS# to CAS# Delay Time	2T-1.5	
TCSH	CAS# Hold Time	3T+2	
TCAS	CAS# Pulse Width	T+3.5	
TPC	CAS# Cycle Time	2T+3	
TCP	CAS# Precharge Time	T-4.5	
TRAC	Data Access Time from RAS#		3.5T
TCAC	Data Access Time from CAS#		T
TCPA	Data Access Time from CAS# Precharge		2T
TCAA	Data Access Time from Column Address		2T

NOTE INMCK = 1/T MHz.

Figure 6-16 DRAM Timing (Write Cycle)



Symbol	Description	Min (ns)	Max (ns)
TRAH	Row Address Hold Time	T-4.5	
TASC	Column Address Setup	T-1	
TCAH	Column Address Hold Time	T-1	
TRAS	RAS# Pulse Width	3T+1.9	
TCRP	CAS# to RAS# Precharge Time	3T+2	
TCSH	CAS# Hold Time from RAS#	3T+2	
TRCD	RAS# to CAS# Delay Time	2T-1.5	
TCP	CAS# Precharge Time	T-4.5	
TCAS	CAS# Pulse Width	T+3.5	
TWP	Write Pulse Width	2T+1	
TWCH	Write Pulse Hold Time from CAS#	T+7.5	
TDS	Data Setup Time to CAS#	T+3.5	
TDH	Data Hold Time to CAS#	T-1	
TDHR	Data Hold Time to RAS#	T-1	
TWCR	Write Pulse Hold Time from RAS#	5T+5	

NOTE INMCK = 1/T MHz.

Figure 6-17 LCD Panel Power Sequencing

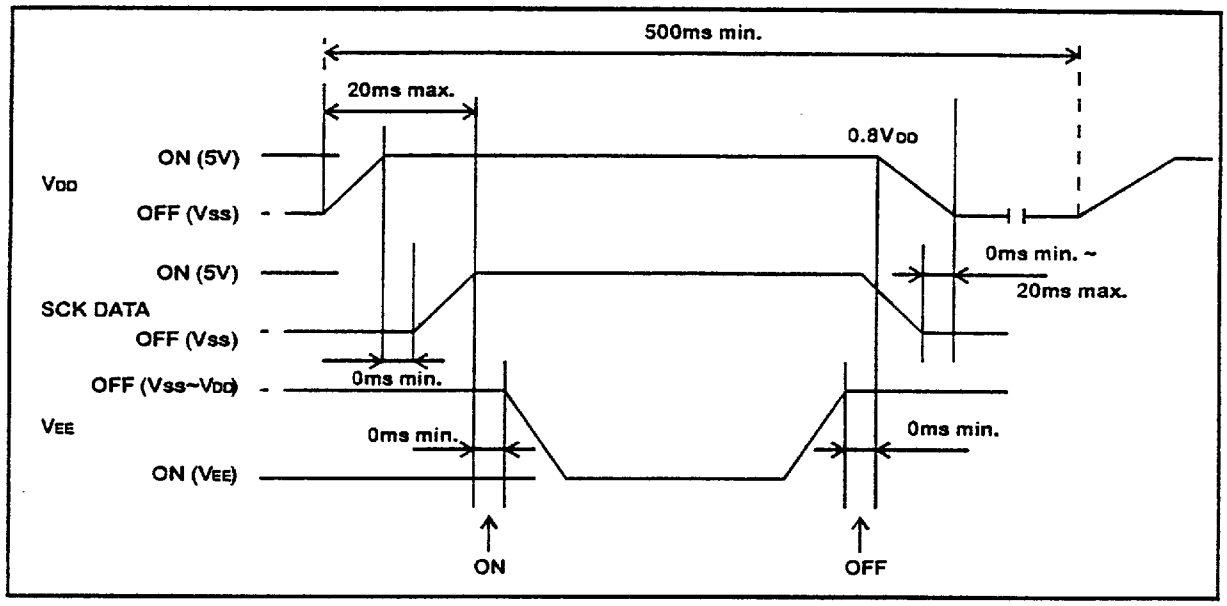


Figure 6-18 Single Panel Monochrome 4-Bit LCD Functional Timing (640x480)

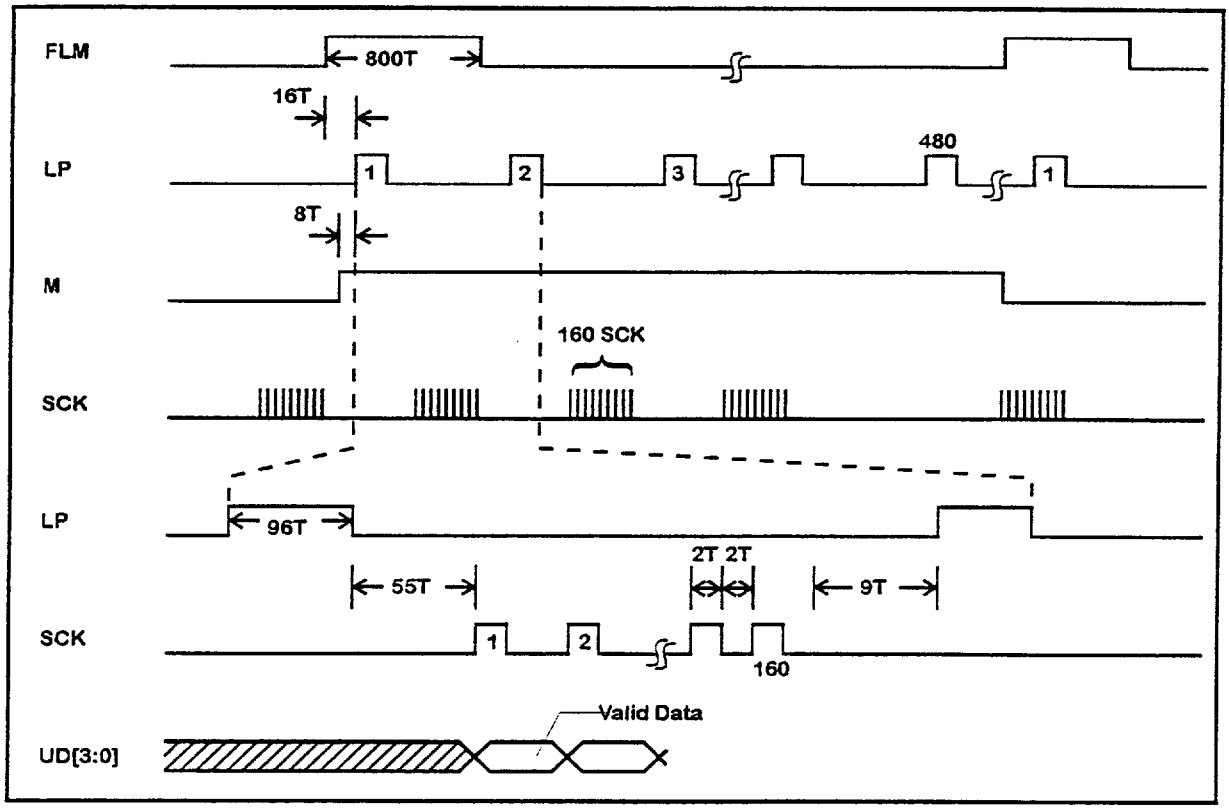


Figure 6-19 Single Panel Monochrome 8-Bit LCD Functional Timing (640x480)

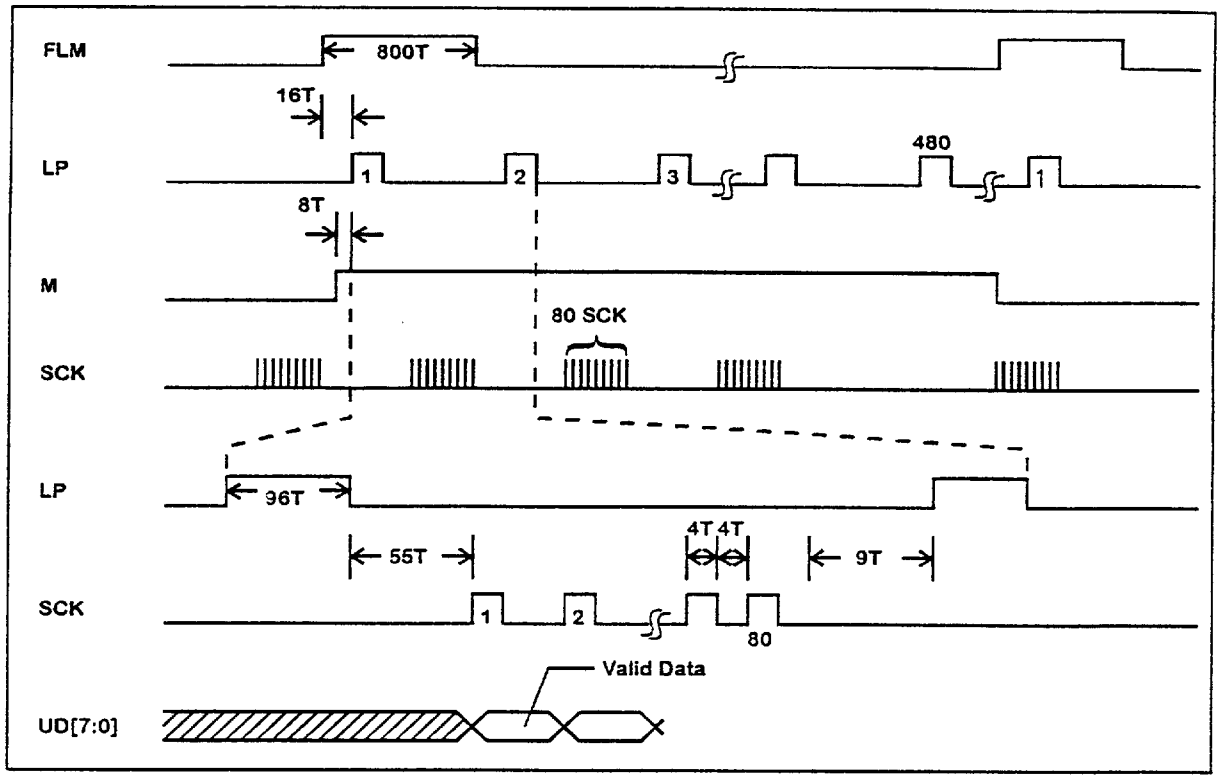


Figure 6-20 Dual Panel Monochrome 8-Bit LCD Functional Timing (640x480)

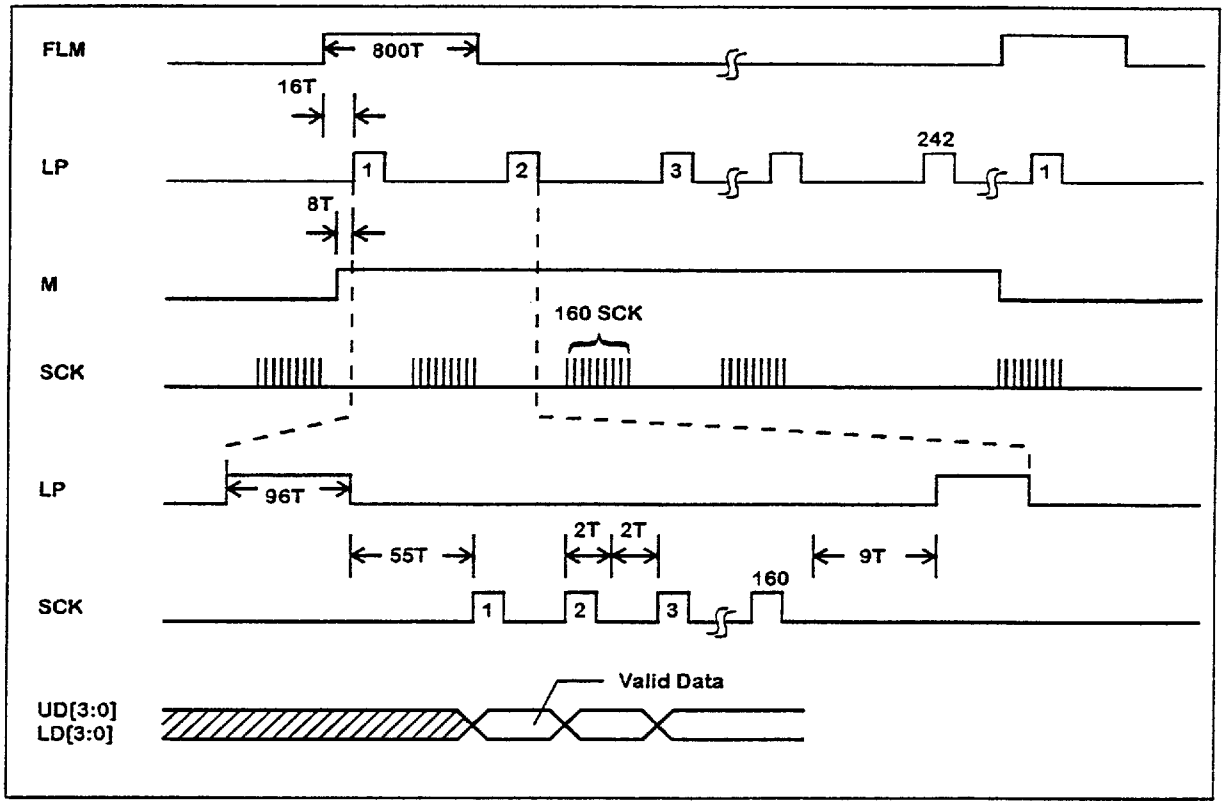


Figure 6-21 Dual Panel Monochrome 16-Bit LCD Functional Timing (1024x768)

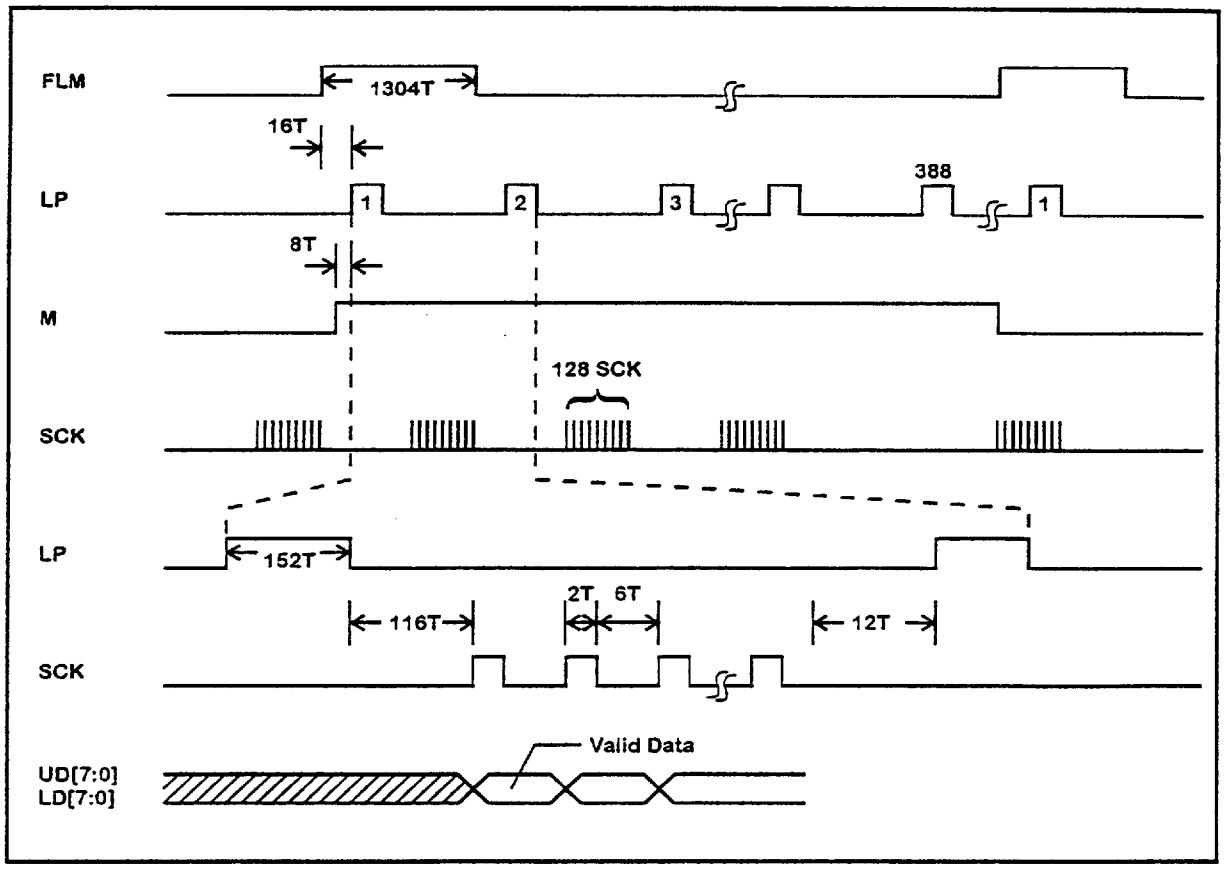
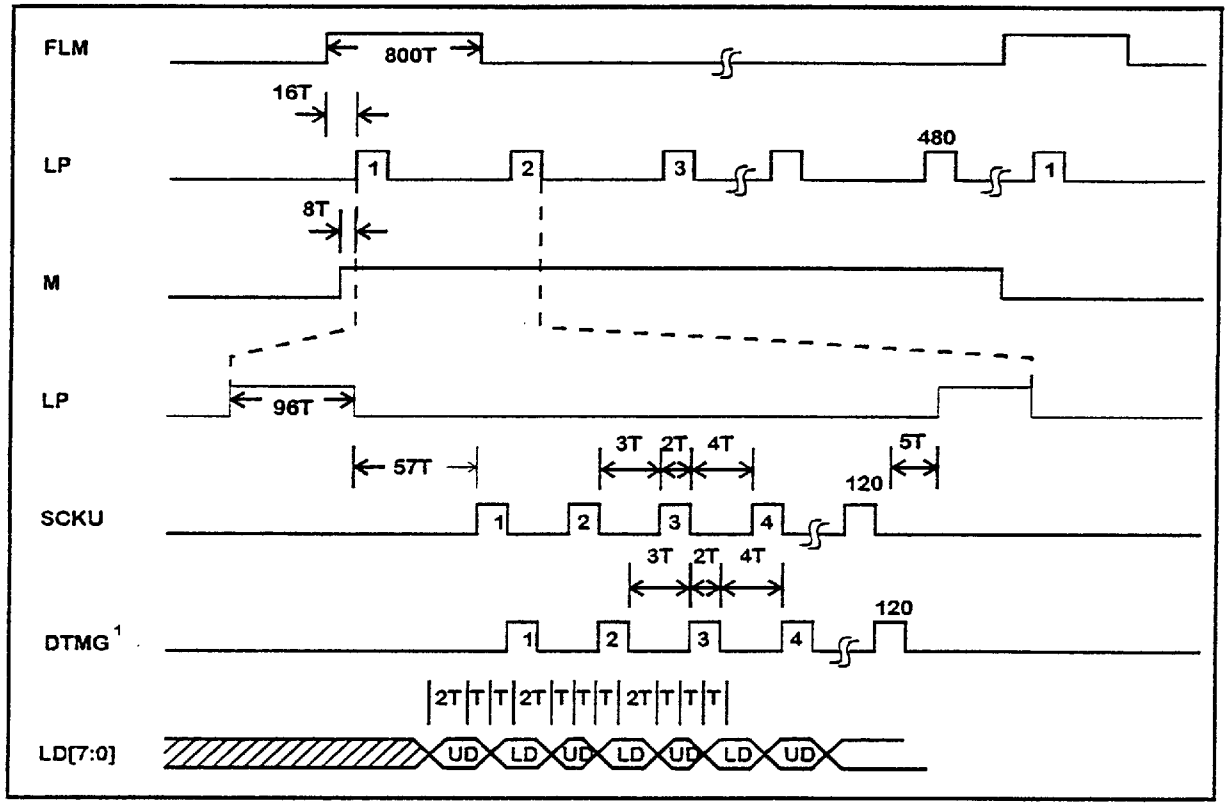


Figure 6-22 Single Panel Color STN 8-Bit LCD Functional Timing (640x480)



[1]Signal DTMG used as shift clock low for single panel 8-bit STN color panel.

Figure 6-23 Single Panel Color STN 16-Bit LCD Functional Timing (640x480)

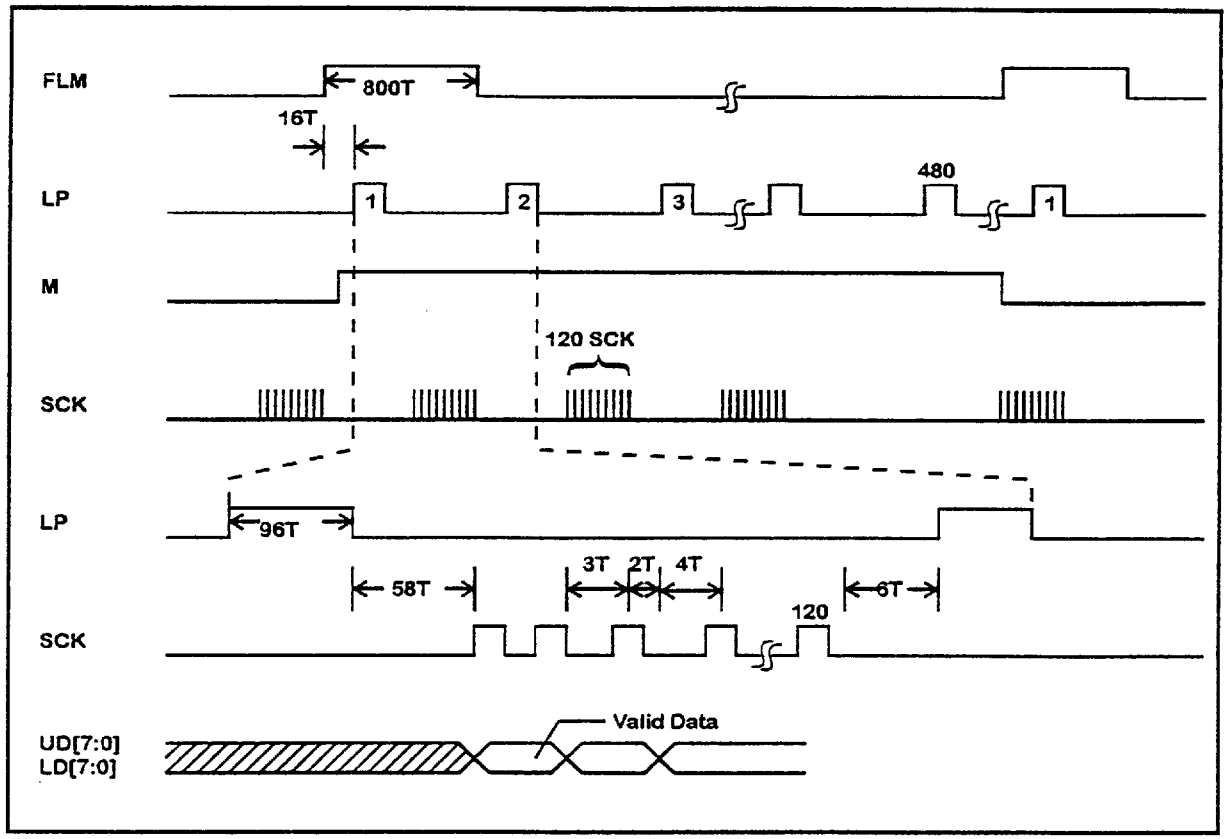


Figure 6-24 Dual Panel Color STN 8-Bit LCD Functional Timing (640x480)

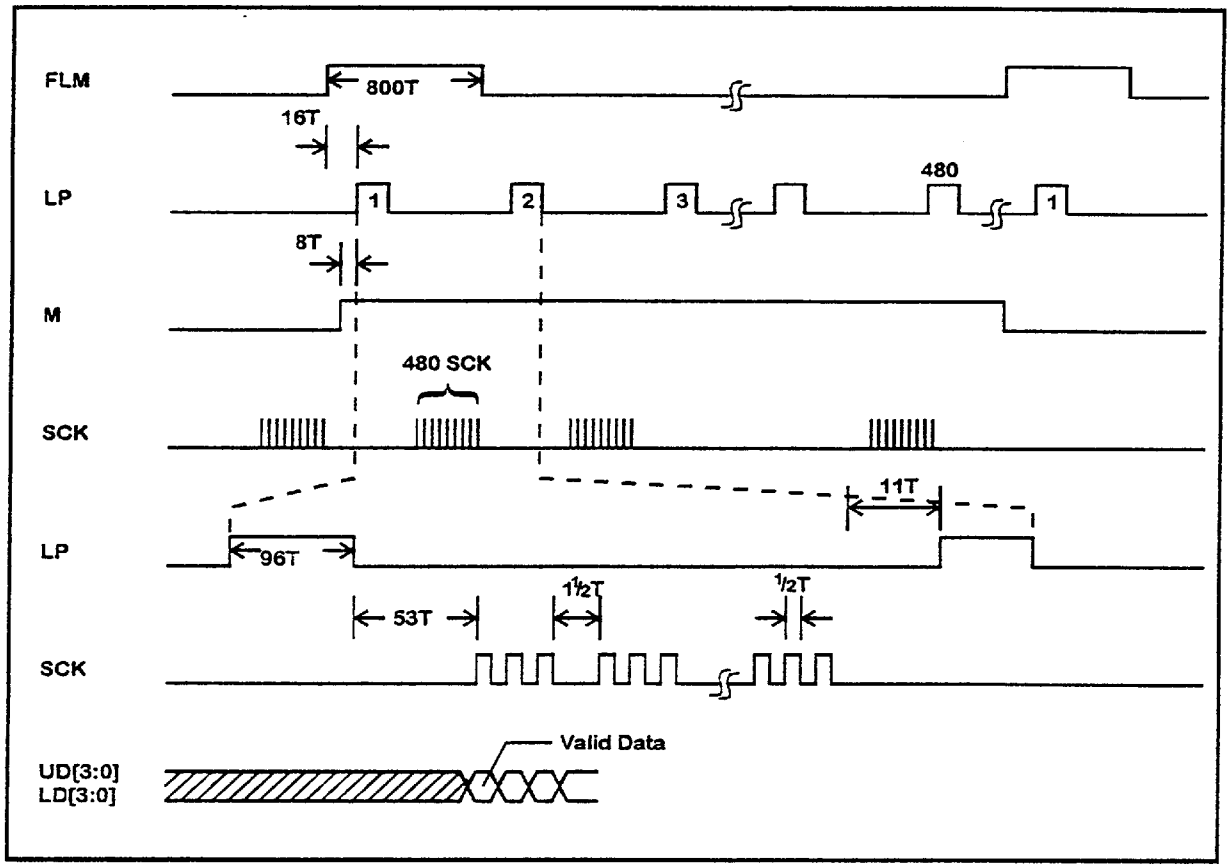


Figure 6-25 Dual Panel Color STN 16-Bit LCD Functional Timing (640x480)

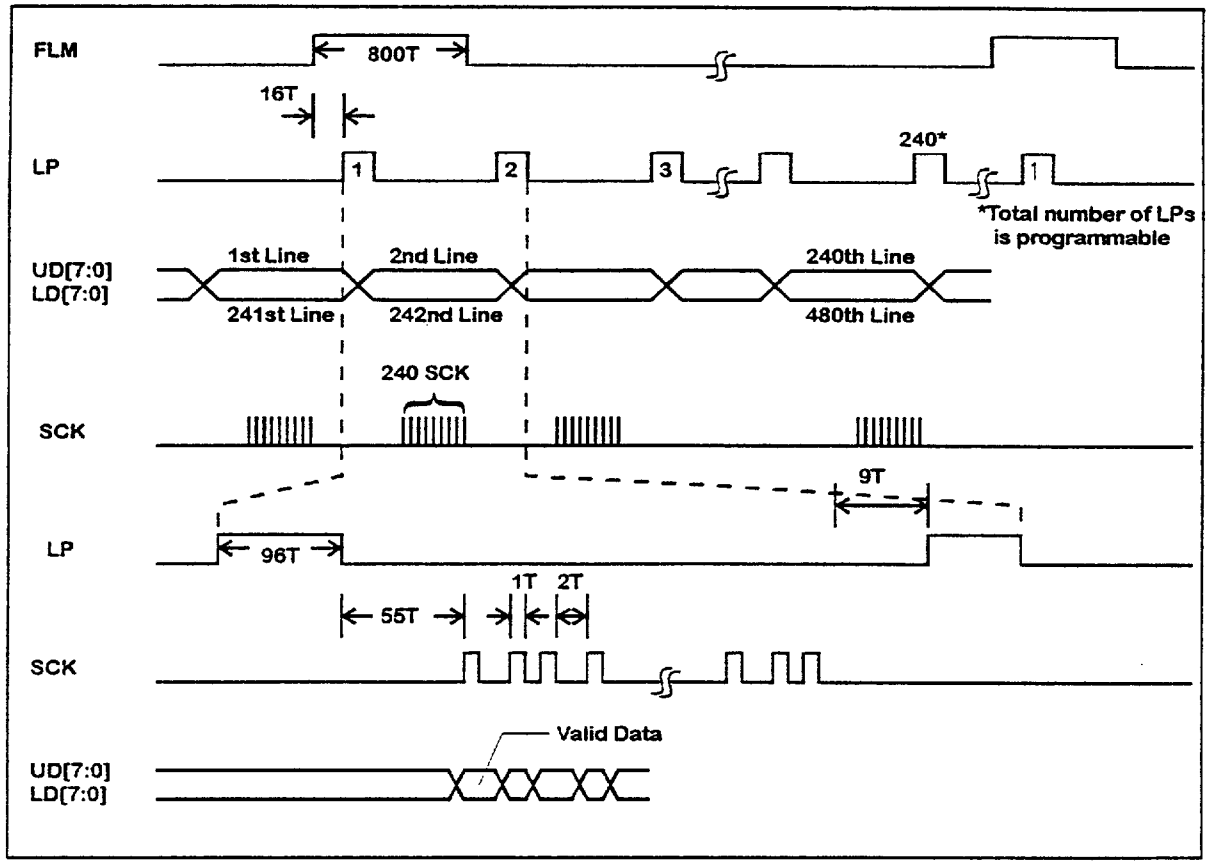


Figure 6-26 Dual Panel Color STN 16-Bit LCD Functional Timing (800x600)

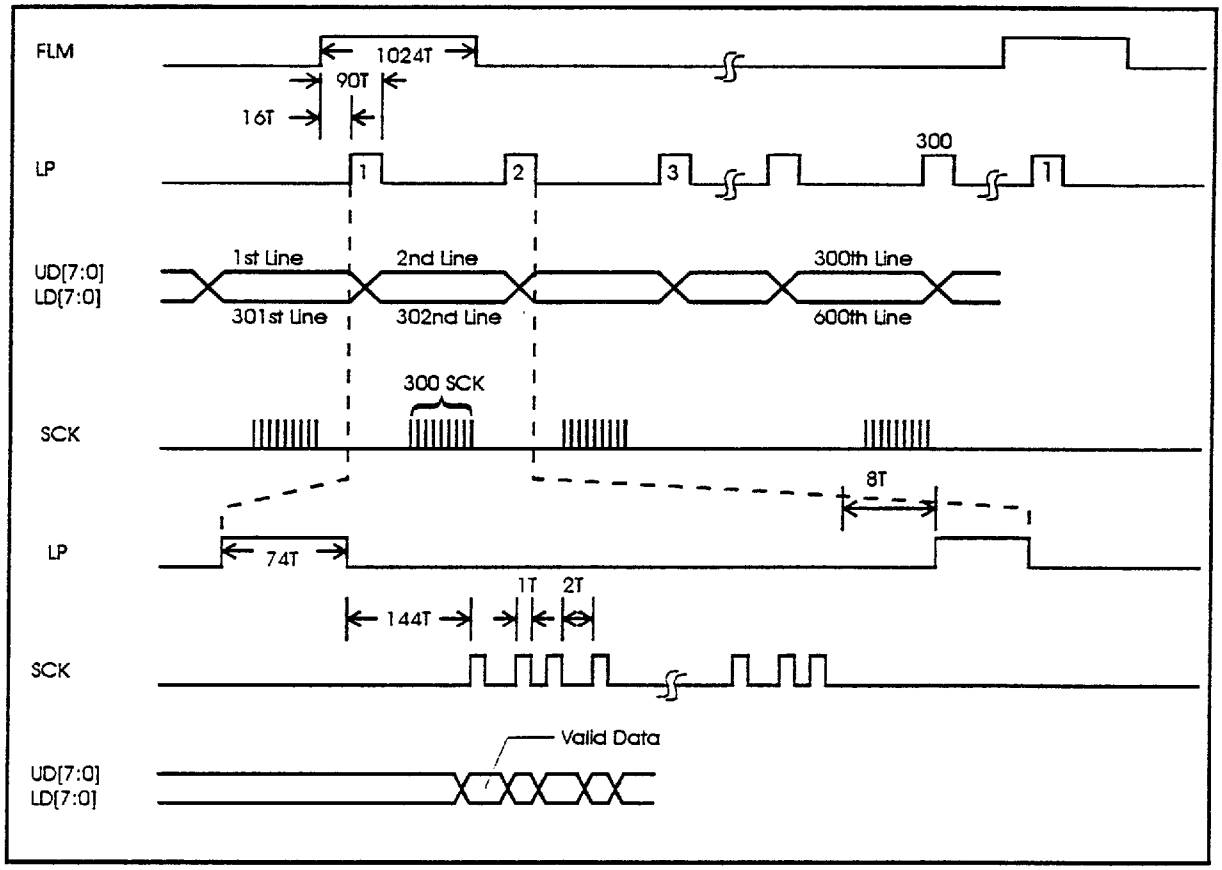


Figure 6-27 Single Panel Color TFT LCD Functional Timing (640x480)

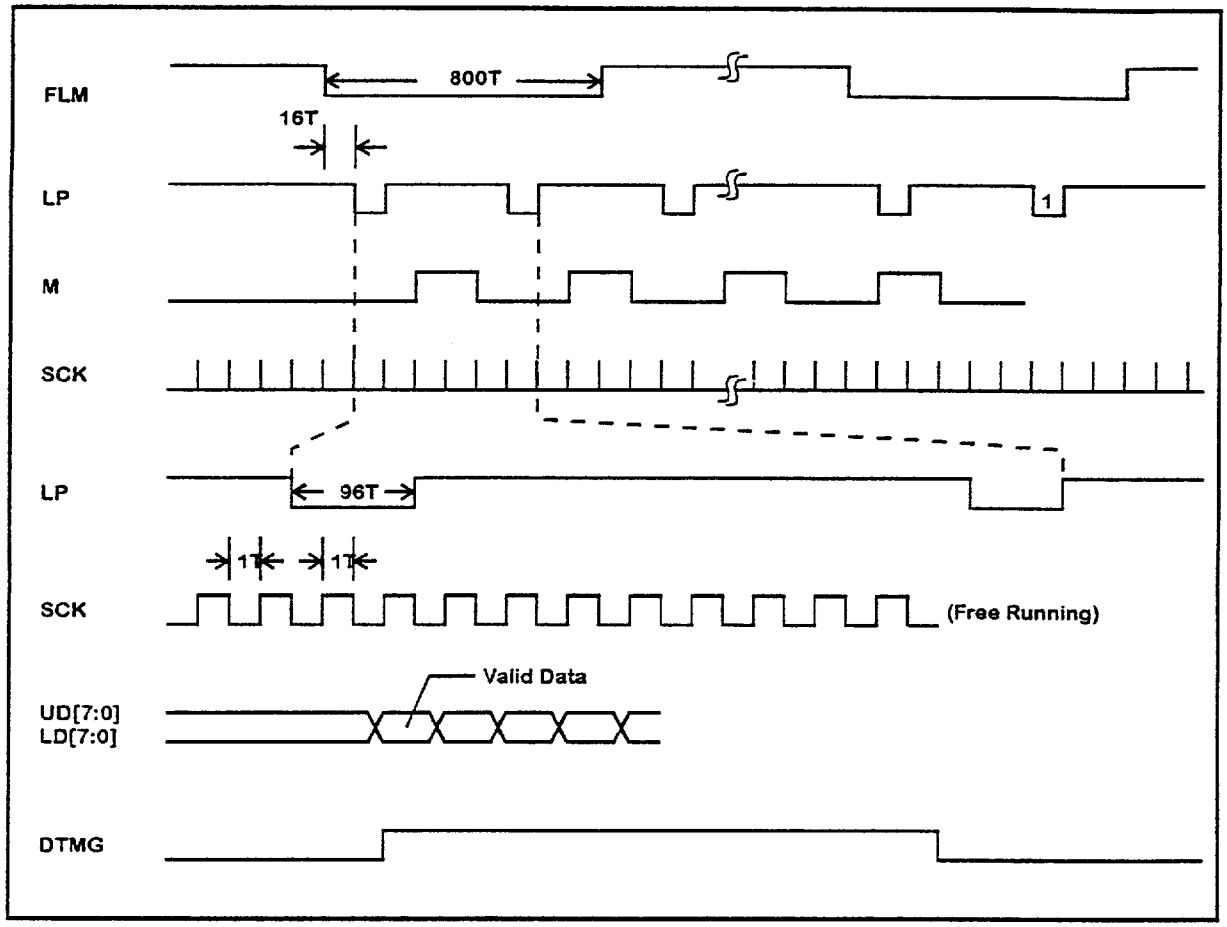


Figure 6-28 Single Panel Color TFT LCD Functional Timing (800x600)

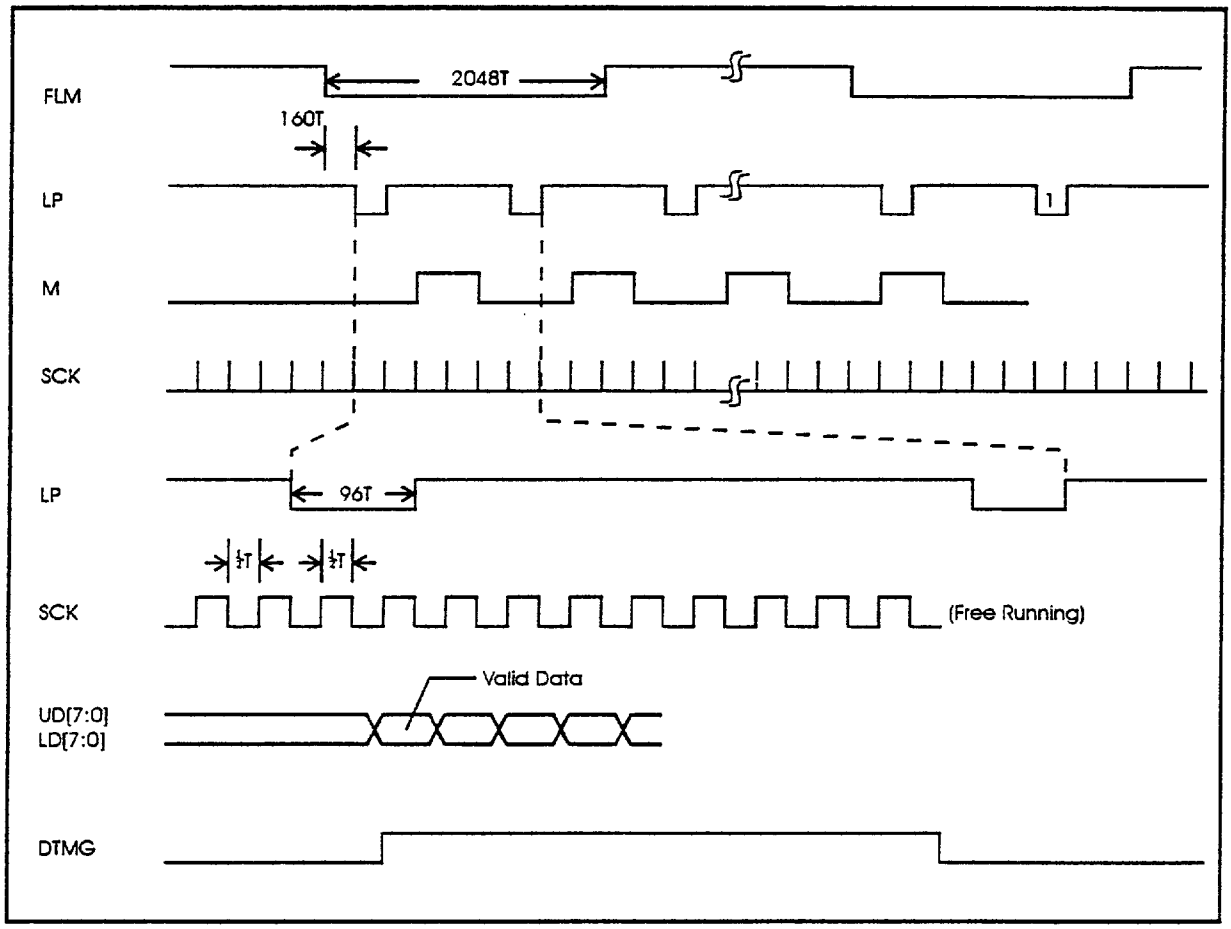
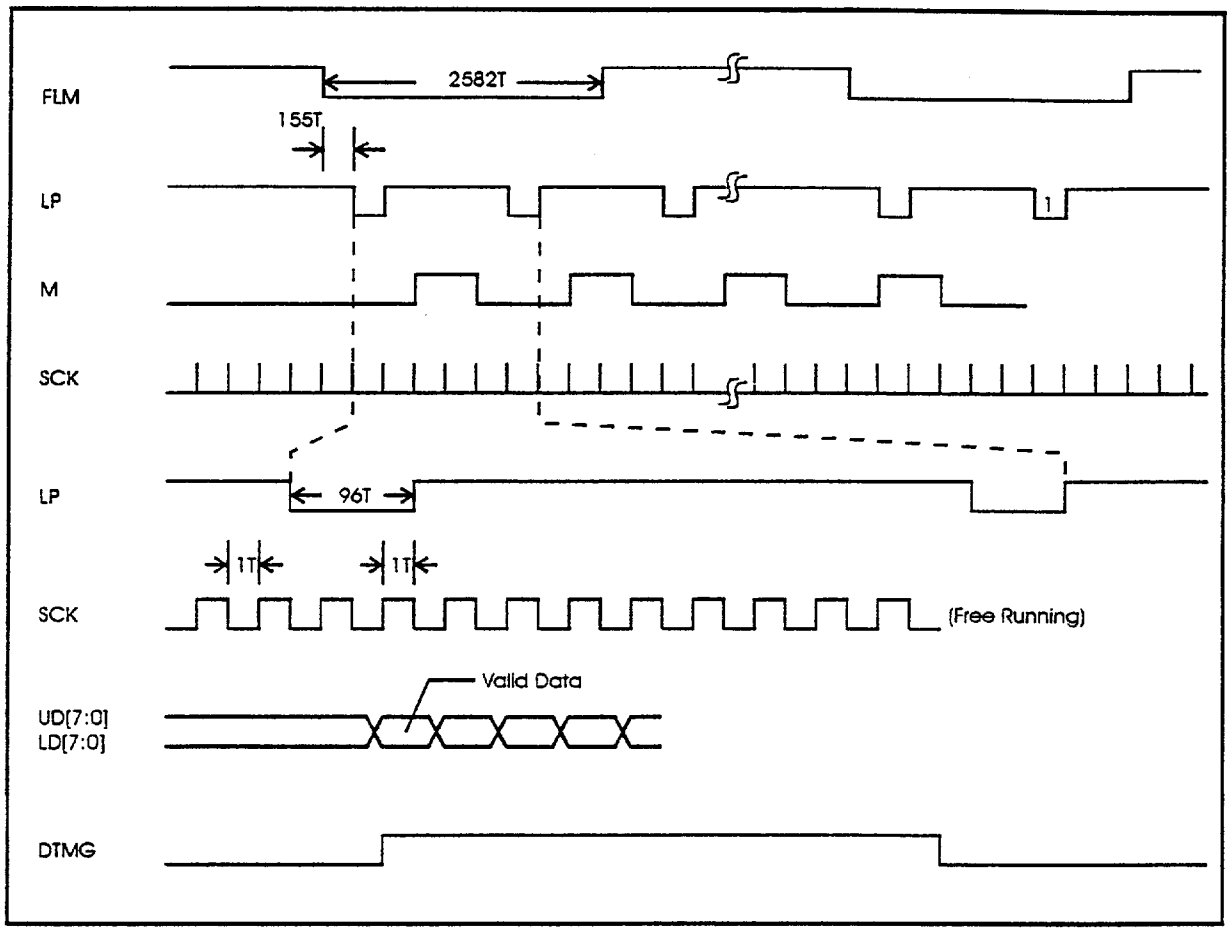
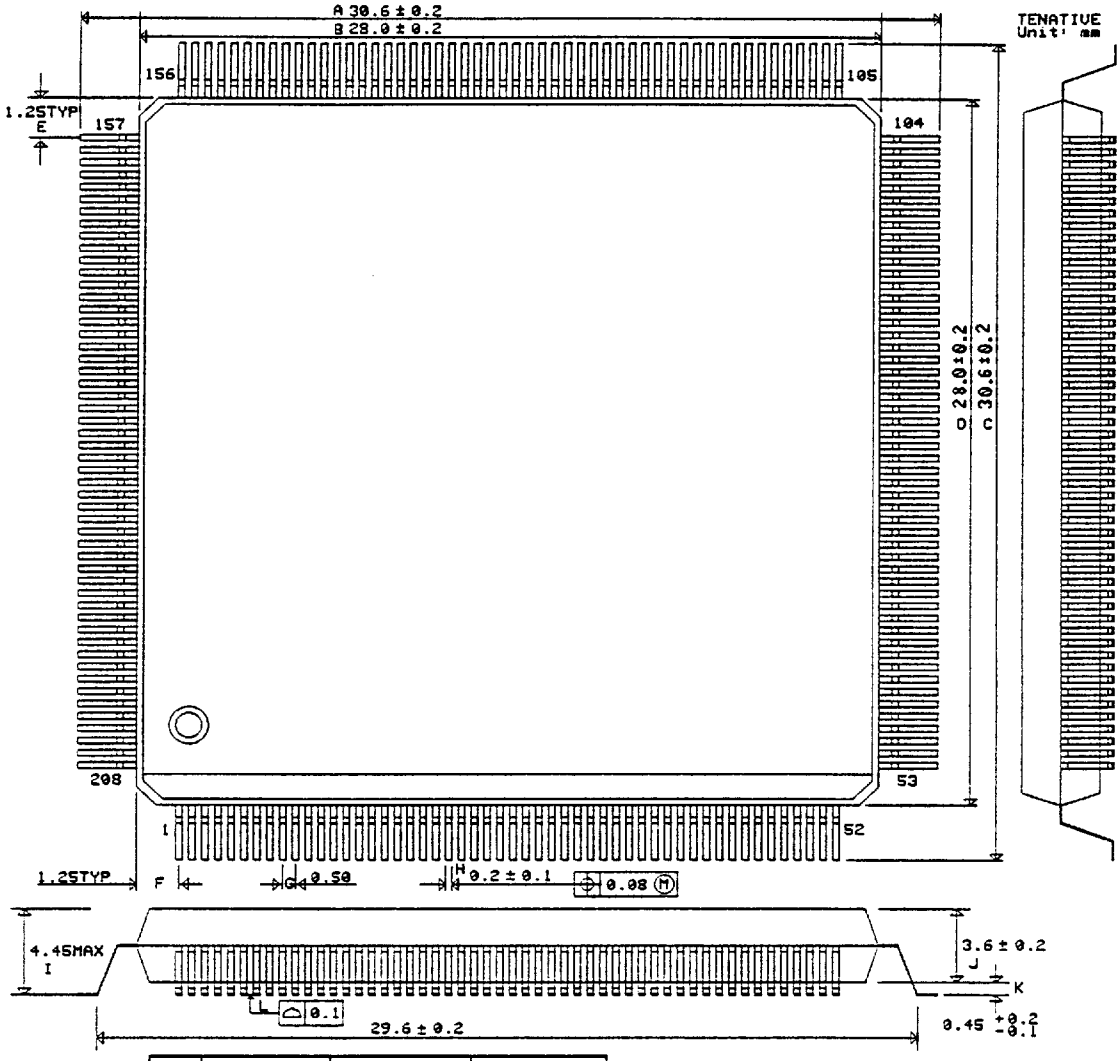


Figure 6-29 Single Panel Monochrome TFT LCD Functional Timing (1024x768)



7.0 Mechanical Package

Figure 7-1 92C178 Mechanical Package



DIM	MILLIMETERS		INCHES		DESCRIPTION
	MIN	MAX	MIN	MAX	
A	30.4	30.8	1.197"	1.213"	Maximum Width LEAD TO LEAD
B	27.8	28.2	1.094"	1.110"	Maximum Width PACKAGE ENVELOPE
C	30.4	30.8	1.197"	1.213"	Maximum Height LEAD TO LEAD
D	27.8	28.2	1.094"	1.110"	Maximum Height PACKAGE ENVELOPE
E	1.25 TYP		.0495" TYP		LEAD CENTER TO PERP. LEAD PLANE
F	1.25 TYP		.0495" TYP		LEAD CENTER TO PERP. LEAD PLANE
G	0.5		.0197"		LEAD TO LEAD CENTER SPACING
H	0.1	0.3	.004"	.012"	LEAD WIDTH
I	——	4.45	——	.175"	PACKAGE HEIGHT LEAD PLANE TO TOP
J	3.4	3.8	.134"	.150"	MAXIMUM THICKNESS PACKAGE ENVELOPE
K	0.35	0.65	.0138"	.0256"	LEAD PLANE TO PACKAGE BOTTOM
L	——	0.1	——	.004"	LEAD PLANE SKEW
M	0.1	0.25	.004"	.01"	LEAD THICKNESS
N	0.3	0.7	.012"	.028"	LEAD FOOTPRINT

Appendix A. Accessing the BBS

The OPTi BBS offers a wide range of useful files and utilities to our customers, from Evaluation PCB Schematics to HPGL/ PostScript format Databooks that you can copy directly to your laser printer. The only requirements for accessing and using the BBS is a modem and an honest response to our questionnaire.

A.1 Paging the SYSOP

Currently, Paging the SYSOP is not a valid choice for the OPTi BBS. Once a full-time SYSOP is created, then there will be hours available for paging the SYSOP and getting immediate help.

For now, you must send [C] Comments to the SYSOP with any questions or problems you are experiencing. They will be answered promptly.

NOTE Each conference has its own Co-SYSOP (the application engineer responsible for that product line), so specific conference questions can be addressed that way, but general, BBS-wide, questions should be sent to the SYSOP from the [0] - Private E-Mail conference.

A.2 System Requirements

The OPTi BBS will support any PC modem up to 14,400 baud, with 8 bits, no parity, and 1 stop bit protocol. The baud rate, handshaking, and system type will automatically be detected by the OPTi BBS.

A.3 Calling In/Hours of Operation

The OPTi BBS phone number is (408) 980-9774. The BBS is on-line 24 hours a day, seven days a week. Currently there is only one line, but as traffic requires additional lines will be installed.

A.4 Logging On for the First Time

To log on to the BBS for the first time,

1. Call (408) 980-9774 with your modem.
2. Enter your first name.
3. Enter your last name.
4. Verify that you have typed your name correctly.
5. Select a password (write it down).
6. Reenter the password to verify spelling.
7. You must then answer the questionnaire that follows.

After you have answered the questionnaire, you are given Customer rights. To change your profile (security level, password, etc.), you must send a [C]omment to the SYSOP explaining why.

After you have logged on for the first time, each subsequent log on will bypass the questionnaire and put you directly at the bulletin request prompt. As bulletins will be added on a regular basis in the future, it is recommended that you read the new bulletins on a regular basis.

A.5 Log On Rules and Regulations

- As a FULLUSER you can download from any conference.
- You will be limited to 45 minutes per day of access time (note that once a download has started, it will finish, even if the daily time limit is exceeded). If you have not entered any keystrokes after 5 minutes, you will automatically be logged off.
- You can upload to the Customer Upload Conference[1] only. This area is used for our customers/contacts to send data to OPTi. You will not be able to download any files from this area.

A.6 Using the BBS

This section will describe how to use the BBS on a daily basis.

The BBS is divided into Conferences that are specific to a product (for example, the Viper Desktop Chipset), or an application group (for example, the Field Application Conference is used by OPTi Field Application Engineers to send data to their contacts in the field). As a general rule, the files in the application specific areas will be for specific application and may contain a password. If a file is password protected, and you know you need that file, you must contact your OPTi sales representative for the password.

The files in the Product Conferences are released data that can be used for evaluating the OPTi product line.

To access a feature of the BBS, you should type the letter in brackets that precedes each menu item. This document places the appropriate letter in brackets whenever you are told to access a feature.

A.6.1 Reading Bulletins

The OPTi BBS will present you with a set of bulletins each time you log on that are global bulletins applying to OPTi in general. In addition to these, each Product Conference will have its own set of bulletins that apply to that product. These bulletins will announce new product information, documentation updates, and bug fixes and product alerts.

1. See Section A.6.5 for more information on uploading.

It is recommended that you read any new bulletins on a regular basis to keep up to date on the OPTi product line.

A.6.2 Sending/Receiving Messages

The Message Menu can be used to send and receive messages from OPTi employees, or other BBS users. The Message menu can also be used to attach files for the receiver to download after they read the message. This method will be used often to send customer specific files to OPTi customers.

Messages to the SYSOP depend upon the conference you are in. Each Product Conference sends Comments and Messages to the SYSOP to the Application Engineer responsible for that conference.

A.6.3 Finding Information

To find information on the OPTi BBS, you must use the [J] Join a Conference option and then list all of the conferences available. They are arranged by product number and name.

Once you are in the correct conference, you should read all applicable bulletins and messages. Then you can [L] List all the files that are available from the File Menu.

A.6.4 Downloading Files From OPTi

The easiest way to download files from OPTi, is to [L] List the files from the File Menu, the [M] Mark and files you want from the list. After you have marked all the files you need, you can [D] Download all the marked files and then logoff automatically.

A.6.5 Uploading Files To OPTi

There are two ways to upload a file to OPTi. The first is similar to the download option. You should [J] Join the Customer Upload Conference (this is the only conference that allows uploads from users) and [U] Upload the file to this conference.

If you are sending the file to a specific person, you should use the Message Menu to [E] Enter a new message to that person and then [A] Attach the file to the message. This way, the person receiving the message can download the file to his or her system without leaving behind a file that will not be used by anyone else on the BBS.

A.6.6 Logging Off

Once you have completed your visit to the OPTi BBS, you must say [G] Goodbye.

A.6.7 Logging Back on Again

To log back on to the BBS,

1. Call (408) 980-9774 with your modem.
2. Enter your first name.
3. Enter your last name.
4. Verify that you have typed your name correctly.
5. Enter your password.

You will not have to answer the questionnaire after the initial log-on. You will also be in the conference you were in when you last logged-on.

A.7 The Menus

There are four major menus that OPTi customers will use, the Main Menu, the File Menu, the Bulletin Menu and the Message Menu.

NOTE The following menus are for the Customer Profile (FULLUSER) only, if your user profile has been changed, you may see slightly different menus.

Figure A-1 The Main Menu

```
MAIN MENU:
[ J ] Join a conference                    [ F
[ M ] Message menu                         [ B
[ C ] Comments to the sysop                [ U
[ Y ] Your settings                        [ G

Conf: "[0] - Private E-Mail", time on 0,
MAIN MENU: [J F M B C P U Y G] ?
```

Figure A-2 The Bulletin Menu

```
+-------------------------------------------------------------------+
|                          Bulletin Menu                            |
|                          _____________                            |
|  [1] - Sample Bulletin 1 Title                                    |
|                                                                   |
|  [2] - Sample Bulletin 2 Title                                    |
|                                                                   |
+-------------------------------------------------------------------+
Bulletins updated: NONE
Enter bulletin # [1..3], [R]elist menu, [N]ew, [ENTER] to quit? [ ]
```

Figure A-3 The File Menu

```
FILE MENU:
[ Q ] Quit to main menu                [ J ] Join a conference
[ L ] List available files             [ U ] Upload a file(s)
[ D ] Download a file(s)               [ S ] Scan for Files
[ E ] Edit marked list                 [ G ] Goodbye & logoff
[ M ] Message menu

Conf: "[0] - Private E-Mail", time on 1, with 44 remaining.
FILE MENU: [Q J L U D S E G M] ?
```

Figure A-4 The Message Menu

```
MESSAGE MENU:
[ Q ] Quit to the main menu            [ J ] Join a conference
[ R ] Read messages                    [ S ] Scan messages
[ E ] Enter a new message              [ K ] Kill a message
[ C ] Check for personal mail          [ F ] File menu
[ G ] Goodbye & logoff

Conf: "[0] - Private E-Mail", time on 2, with 44 remaining.
MESSAGE MENU: [Q J R S E K C F G] ?
```

A.7.1 Menu Selections

- [B] Bulletin MenuMenu(s): main
  Access the Bulletin Menu.
- [C] Check for personal mailMenu(s): message
  See if you have any mail.
- [C] Comments to the sysopMenu(s): main
  Leave a private comment for the SYSOP.
- [D] Download a file(s)Menu(s): file
  Download a file from the BBS to your computer. If you have marked files it will display these files. If you have not marked any files, it will ask you for a file name. The file must be present in the current conference for you to be able to enter its name.
- [E] Edit Marked ListMenu(s): file
  Change the entries that you have selected as Marked for downloading.
- [E] Enter a new messageMenu(s): message
  Send a new message to someone on the BBS.
- [F] File MenuMenu(s): main, message
  Access the File Menu.
- [G] Goodbye and logoffMenu(s): main, message, file
  Logoff the system.
- [J] Join a ConferenceMenu(s): main, message, file
  Change conferences (product areas).
- [K] Kill a messageMenu(s): message
  Delete a message.
- [L] List available filesMenu(s): file
  List the files in the current conference. Note that most conferences have sub-categories of files (Schematics, JOB, etc.) that you will be asked for (or you can press enter the list all of the categories).
- [M] Message MenuMenu(s): main, file
  Access the Message Menu.
- [Q] Quit to Main MenuMenu(s): message, file
  Leave current menu and return to the Main Menu.
- [R] Read MessagesMenu(s): message
  Read messages in the current conference or all conferences.

- [S] Scan for FilesMenu(s): file
  Scan for particular files (by name, or extension, etc.).
- [S] Scan messagesMenu(s): message
  Search for message by specific qualifier (date, sender etc.).
- [U] Upload a file(s)Menu(s): file
  Send a file from your computer to OPTi. This can only be done in the Customer Upload Conference.
- [U] Userlog ListMenu(s): main
  Lists the user database, in order of logon. This is useful if you are sending a message and are looking for the spelling of a persons name.
- [Y] Your settingsMenu(s): main
  Show you settings and allow you to make changes. These include password, name, address, etc.