National Semiconductor

93L425A
1024 x 1-Bit Static Random Access Memory

General Description

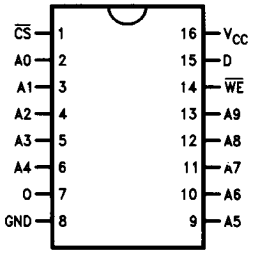
The 93L425A is a 1024-bit read write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

Features

- New design to replace old 93425/93L425
- Improved ESD thresholds
- Alpha hard without die coat
- Commercial address access time
  93L425A 25 ns max
- Features TRI-STATE® output
- Power dissipation decreases with increasing temperature

Connection Diagram

16-Pin DIP



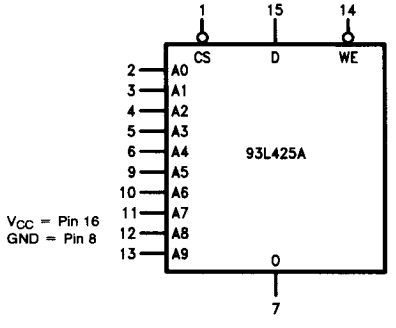
TL/D/10004–1

Top View

Order Number 93L425ADC or 93L425APC
See NS Package Number J16A* or N16E*

Optional Processing QR = Burn-In
*For most current package information, contact product marketing.

Logic Symbol



TL/D/10004–3

Pin Names

$\overline{CS}$	Chip Select (Active LOW)
A0–A9	Address Inputs
$\overline{WE}$	Write Enable Input (Active LOW)
D	Data Input
O	Data Output

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Note 1)	−0.5V to V_{CC}
Input Current (DC)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Note 2)	−0.5V to 5.5V
Lead Temperature (Soldering, 10 sec.)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC}) Commercial	5.0V ±5%
Case Temperature (T_C) Commercial	0°C to +75°C

DC Characteristics over operating temperature ranges (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −5.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 16 mA			0.45	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5, & 6)	2.1			V
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5, & 6)			0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V		−180	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 4.5V		1.0	40	μA
I_{IHB}	Input Breakdown Current	V_{CC} = Max, V_{IN} = V_{CC}			1.0	mA
V_{IC}	Input Diode Clamp Voltage	V_{CC} = Max, I_{IN} = −10 mA		−1.0	−1.5	V
I_{OZH}	Output Current (HIGH Z)	V_{CC} = Max, V_{OUT} = 2.4V			50	μA
I_{OZL}		V_{CC} = Max, V_{OUT} = 0.5V			−50	μA
I_{OS}	Output Current Short Circuit to Ground (Note 7)	V_{CC} = Max (Note 7)			−100	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs = GND, Output Open			65	mA

AC Electrical Characteristics (Note 6) V_{CC} = 5.0 ±5%, GND = 0V, T_C = 0°C to + 75°C

Symbol	Parameter	Conditions	Min	Max	Units
READ TIMING					
t_{ACS}	Chip Select Access Time	*Figures 3a, 3b*		15	ns
t_{ZRCS}	Chip Select to HIGH Z			15	ns
t_{AA}	Address Access Time (Note 8)			25	ns
WRITE TIMING					
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*Figure 4*	20		ns
t_{WSD}	Data Setup Time Prior to Write		5		ns
t_{WHD}	Data Hold Time after Write		5		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		5		ns
t_{WHA}	Address Hold Time after Write		5		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		ns
t_{ZWS}	Write Enable to Output Disable			15	ns
t_{WR}	Write Recovery Time			15	ns

Note 1: Either input voltage limit or input current limit is sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V, T_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels V_{IH} = 0.45V (V_{OL} Max) and V_{IH} = 2.4V (V_{OH} Min).

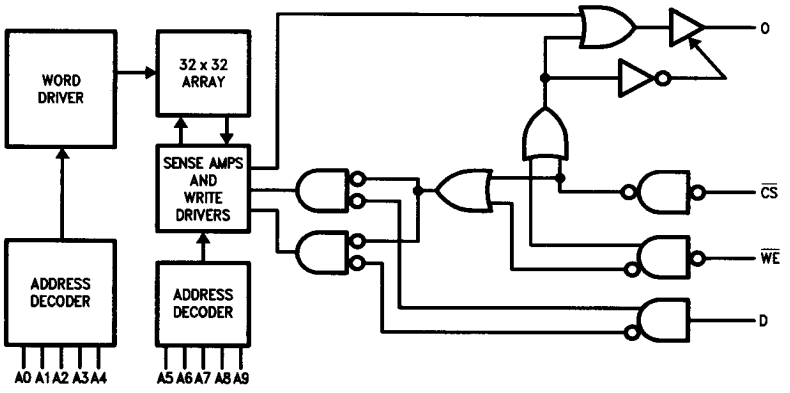
Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

Logic Diagram



TL/D/10004–2

Functional Description

The 93L425A is a fully decoded 1024-bit read write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address A0–A9.

One Chip Select ($\overline{CS}$) input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories the fast chip select access time permits direct address decoding without an increase in overall memory access time.

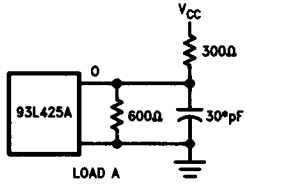
The read and write functions of the 93L425A are controlled by the state of the active LOW Write Enable $\overline{WE}$ input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at A0 through A9. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output O.

The 93L425A has a three-state output which provides an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-up provides drive capability for high capacitive loads while the high impedance state allows optimization of word expansion in bus organized systems.

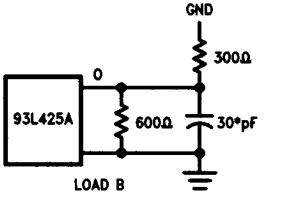
Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	H	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write 0
L	L	H	HIGH Z	Write 1
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level: 2.4V
L = LOW Voltage Level: 0.45V
X = Don't Care HIGH or LOW
HIGH Z = High-Impedance



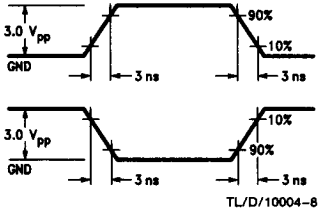
TL/D/10004-4



TL/D/10004-5

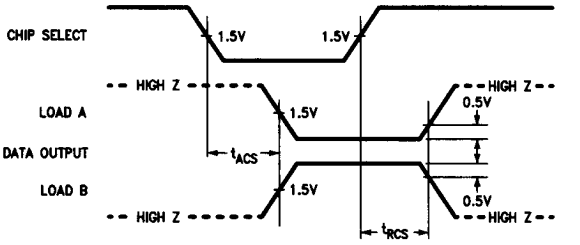
Note: Load A is used for all production testing.
*Includes jig and probe capacitance.

FIGURE 1. AC Test Output Load



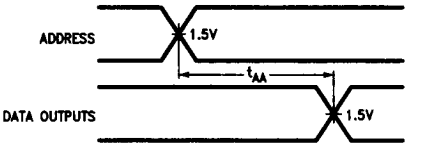
TL/D/10004-8

FIGURE 2. AC Test Input Levels



TL/D/10004-6

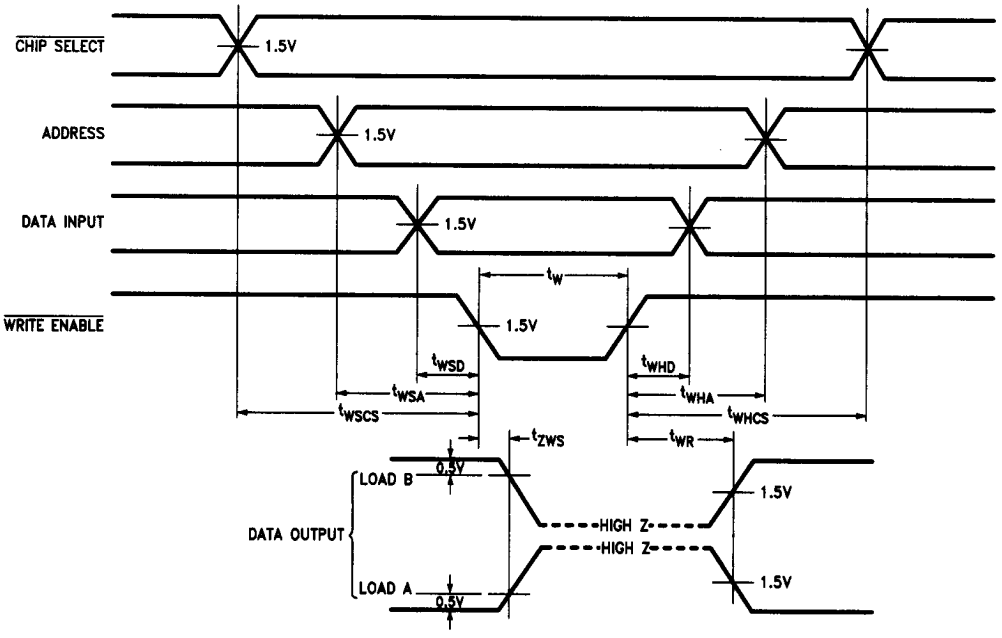
3a. Read Mode Propagation Delay from Chip Select



TL/D/10004-7

3b. Read Mode Propagation Delay from Address

FIGURE 3. Read Mode Timing



TL/D/10004–9

Note 1: Timing Diagram represents one solution which results in an optimum cycle time Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0V–0V.

FIGURE 4. Write Mode Timing