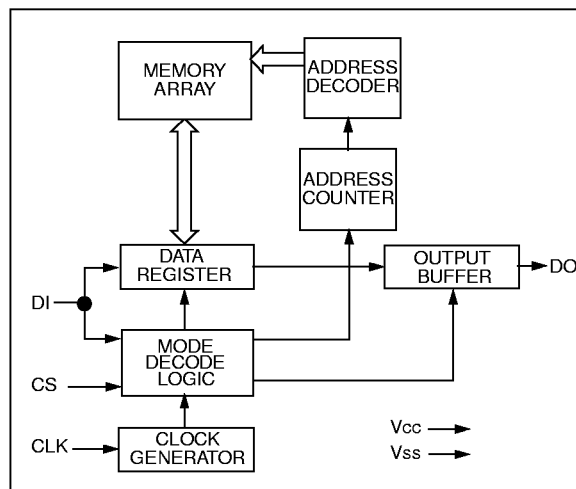


4K 2.5V Microwire® Serial EEPROM

FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
 - 1 mA active current (typical)
 - 1 μ A standby current (maximum)
- 512 x 8 bit organization (93LC66A)
- 256 x 16 bit organization (93LC66B)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial interface
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP/SOIC and 8-pin TSSOP packages
- Available for the following temperature ranges:
 - Commercial (C): 0°C to +70°C
 - Industrial (I): -40°C to +85°C

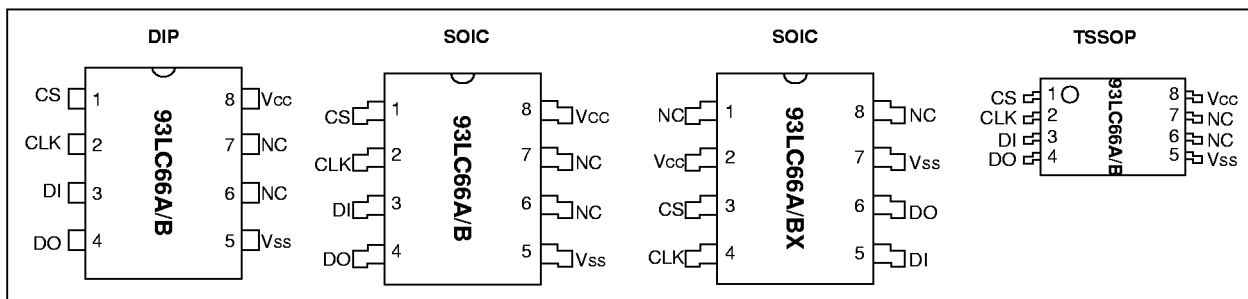
BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 93LC66A/B are 4K-bit, low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 (93LC66A) or x16 bits (93LC66B). Advanced CMOS technology makes these devices ideal for low power nonvolatile memory applications. The 93LC66A/B is available in standard 8-pin DIP, surface mount SOIC, and TSSOP packages. The 93LC66AX/BX are only offered in a 150-mil SOIC package.

PACKAGE TYPE



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC}7.0V
 All inputs and outputs w.r.t. V_{SS}-0.6V to V_{CC} +1.0V
 Storage temperature-65°C to +150°C
 Ambient temp. with power applied.....-65°C to +125°C
 Soldering temperature of leads (10 seconds)+300°C
 ESD protection on all pins4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
NC	No Connect
VCC	Power Supply

TABLE 1-2 DC AND AC ELECTRICAL CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted		Commercial (C): V _{CC} = +2.5V to +6.0V Industrial (I): V _{CC} = +2.5V to +6.0V		T _{amb} = 0°C to +70°C T _{amb} = -40°C to +85°C	
Parameter	Symbol	Min.	Max.	Units	Conditions
High level input voltage	VIH1	2.0	V _{CC} +1	V	2.7V ≤ V _{CC} ≤ 6.0V (Note 2)
	VIH2	0.7 V _{CC}	V _{CC} +1	V	V _{CC} < 2.7V
Low level input voltage	VIL1	-0.3	0.8	V	V _{CC} > 2.7V (Note 2)
	VIL2	-0.3	0.2 V _{CC}	V	V _{CC} < 2.7V
Low level output voltage	VoL1	—	0.4	V	I _{OL} = 2.1 μA; V _{CC} = 4.5V
	VoL2	—	0.2	V	I _{OL} = 100 μA; V _{CC} = V _{CC} Min.
High level output voltage	VoH1	2.4	—	V	I _{OH} = -400 μA; V _{CC} = 4.5V
	VoH2	V _{CC} - 0.2	—	V	I _{OH} = -100 μA; V _{CC} = V _{CC} Min.
Input leakage current	II	-10	10	μA	V _{IN} = V _{SS} to V _{CC}
Output leakage current	ILO	-10	10	μA	V _{OUT} = V _{SS} to V _{CC}
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7	pF	V _{IN} /V _{OUT} = 0 V (Notes 1 & 2) T _{amb} = +25°C, FCLK = 1 MHz
Operating current	I _{CC} read	—	1 500	mA μA	FCLK = 2 MHz; V _{CC} = 6.0V FCLK = 1 MHz; V _{CC} = 3.0V
	I _{CC} write	—	1.5	mA	
Standby current	I _{CCS}	—	1	μA	CS = V _{SS} ; DI = V _{SS}
Clock frequency	FCLK	—	2	MHz	V _{CC} > 4.5V
			1	MHz	V _{CC} < 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	T _{CSS}	50	—	ns	Relative to CLK
Chip select hold time	T _{CSH}	0	—	ns	Relative to CLK
Chip select low time	T _{CSL}	250	—	ns	
Data input setup time	T _{DIS}	100	—	ns	Relative to CLK
Data input hold time	T _{DIH}	100	—	ns	Relative to CLK
Data output delay time	T _{PD}	—	400	ns	CL = 100 pF
Data output disable time	T _{CZ}	—	100	ns	CL = 100 pF (Note 2)
Status valid time	T _{SV}	—	500	ns	CL = 100 pF
Program cycle time	T _{WC}	—	6	ms	ERASE/WRITE mode
	T _{EC}	—	6	ms	ERASE mode
	T _{WL}	—	15	ms	WRITE mode
Endurance	—	1M	—	cycles	25°C, V _{CC} = 5.0V, Block Mode (Note 3)

Note 1: This parameter is tested at T_{amb} = 25°C and FCLK = 1 MHz.

Note 2: This parameter is periodically sampled and not 100% tested.

Note 3: This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which may be obtained on our website.

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock (CLK) is used to synchronize the communication between a master device and the 93LC66A/B. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is low (device deselected). If CS is high, but a START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for a START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a START condition the specified number of clock cycles (respectively low to high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (Table 2-1 and Table 2-2). CLK and DI then become don't care inputs waiting for a new START condition to be detected.

2.3 Data In (DI)

Data In (DI) is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out (DO) is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/ $\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/ $\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

TABLE 2-1 INSTRUCTION SET FOR 93LC66A

Instruction	SB	Opcode	Address									Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/BSY)	12
ERAL	1	00	1	0	X	X	X	X	X	X	X	—	(RDY/BSY)	12
EWDS	1	00	0	0	X	X	X	X	X	X	X	—	HIGH-Z	12
EWEN	1	00	1	1	X	X	X	X	X	X	X	—	HIGH-Z	12
READ	1	10	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	20
WRITE	1	01	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/BSY)	20
WRAL	1	00	0	1	X	X	X	X	X	X	X	D7 - D0	(RDY/BSY)	20

TABLE 2-2 INSTRUCTION SET FOR 93LC66B

Instruction	SB	Opcode	Address								Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/ $\overline{\text{BSY}}$)	11
ERAL	1	00	1	0	X	X	X	X	X	X	—	(RDY/ $\overline{\text{BSY}}$)	11
EWDS	1	00	0	0	X	X	X	X	X	X	—	HIGH-Z	11
EWEN	1	00	1	1	X	X	X	X	X	X	—	HIGH-Z	11
READ	1	10	A7	A6	A5	A4	A3	A2	A1	A0	—	D15 - D0	27
WRITE	1	01	A7	A6	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/ $\overline{\text{BSY}}$)	27
WRAL	1	00	0	1	X	X	X	X	X	X	D15 - D0	(RDY/ $\overline{\text{BSY}}$)	27

3.0 FUNCTIONAL DESCRIPTION

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/BUSY status during a programming operation. The READY/BUSY status can be verified during an ERASE/WRITE operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the HIGH-Z state on the falling edge of the CS.

3.1 START Condition

The START bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (ERASE, ERAL, EWDS, EWEN, READ, WRITE, and WRAL). As soon as CS is high, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcodes, addresses, and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

3.2 Data In (DI) Data Out (DO)

It is possible to connect the Data In (DI) and Data Out (DO) pins together. However, with this configuration, if A0 is a logic-high level, it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

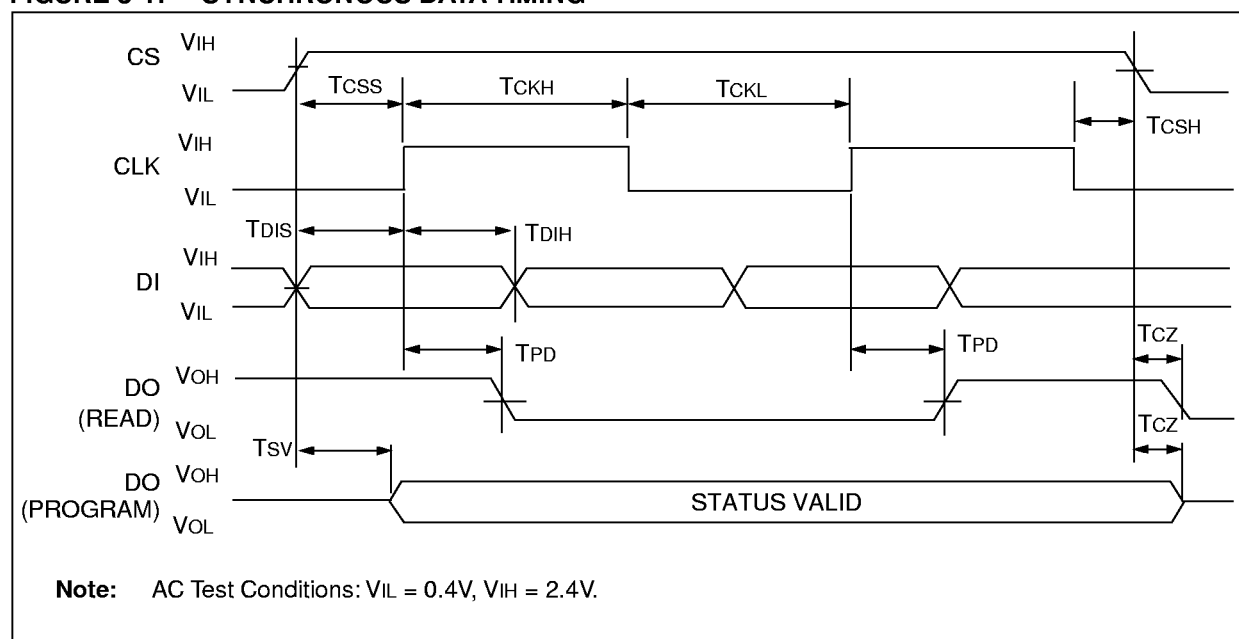
3.3 Data Protection

During power-up, all programming modes of operation are inhibited until VCC has reached a level greater than 2.2V. During power-down, the source data protection circuitry acts to inhibit all programming modes when VCC has fallen below 2.2V at nominal conditions.

The ERASE/WRITE Disable (EWDS) and ERASE/WRITE Enable (EWEN) commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

FIGURE 3-1: SYNCHRONOUS DATA TIMING



3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical “1” state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the $\text{READY}/\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical “0” indicates that programming is still in progress. DO at logical “1” indicates that the register at the specified address has been erased and the device is ready for another instruction.

3.5 Erase All (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical “1” state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the $\text{READY}/\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}) and before the entire ERAL cycle is complete.

FIGURE 3-2: ERASE TIMING

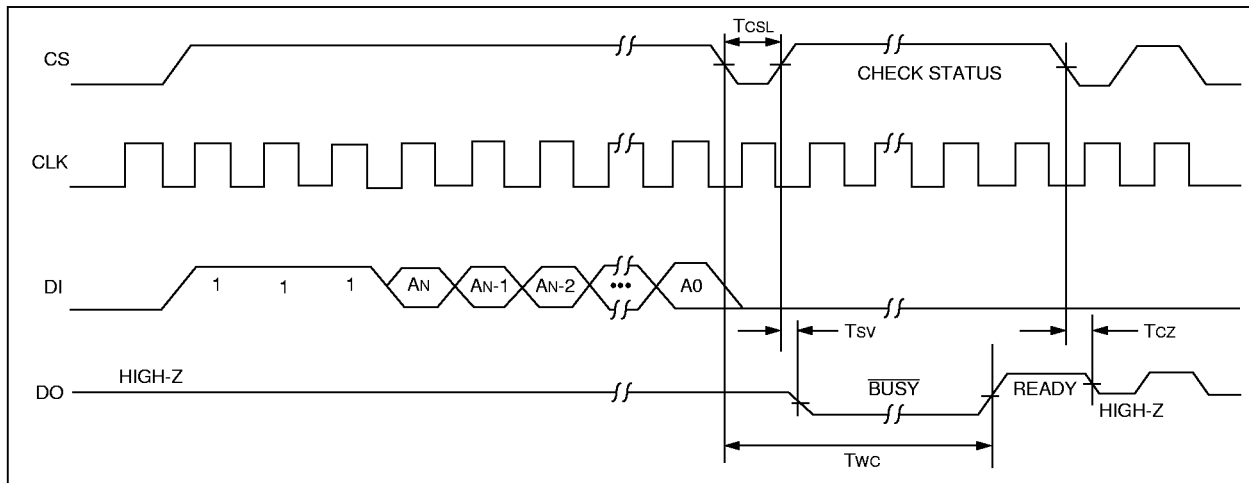
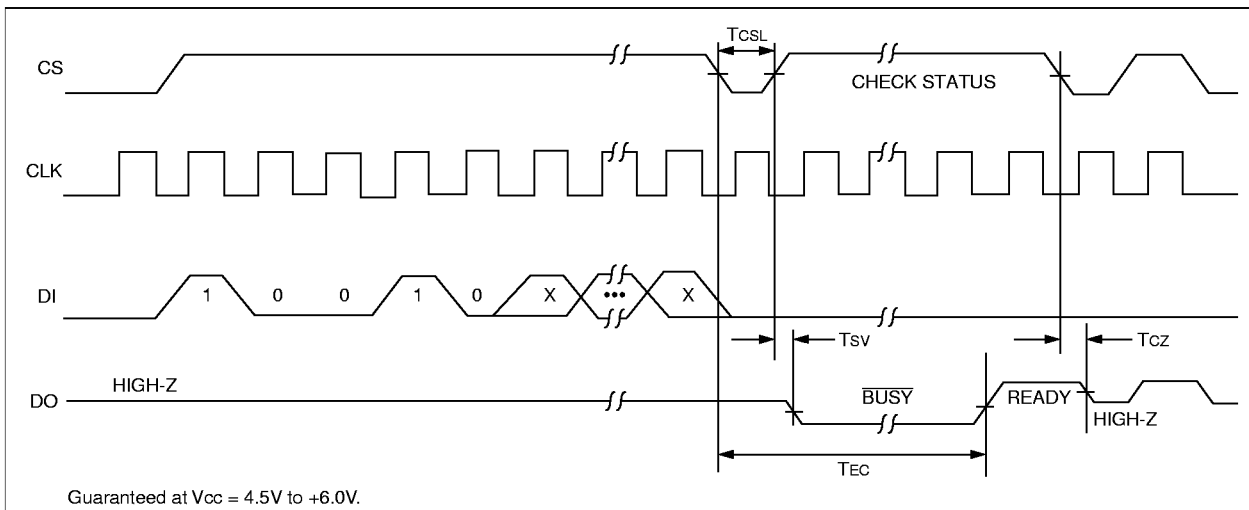


FIGURE 3-3: ERAL TIMING



3.6 ERASE/WRITE Disable and Enable (EWDS/EWEN)

The 93LC66A/B powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an ERASE/WRITE Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWDS and EWEN instructions.

3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (93LC66A) or 16-bit (93LC66B) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 3-4: EWDS TIMING

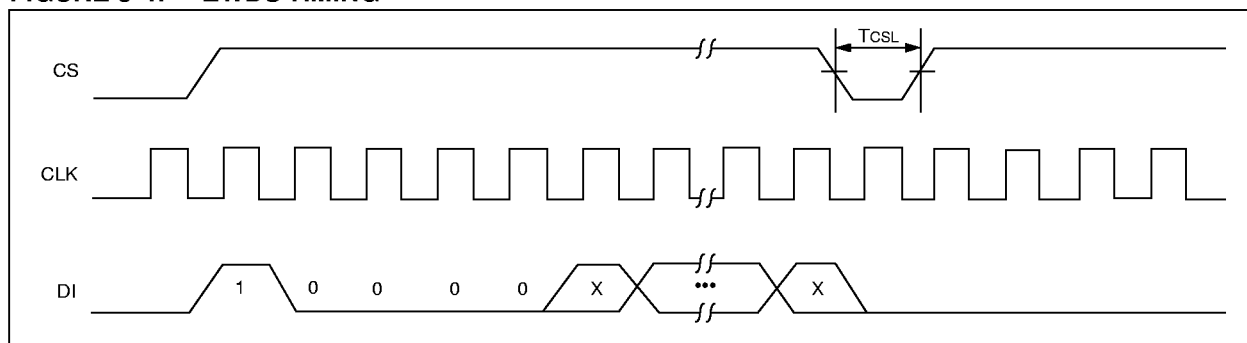


FIGURE 3-5: EWEN TIMING

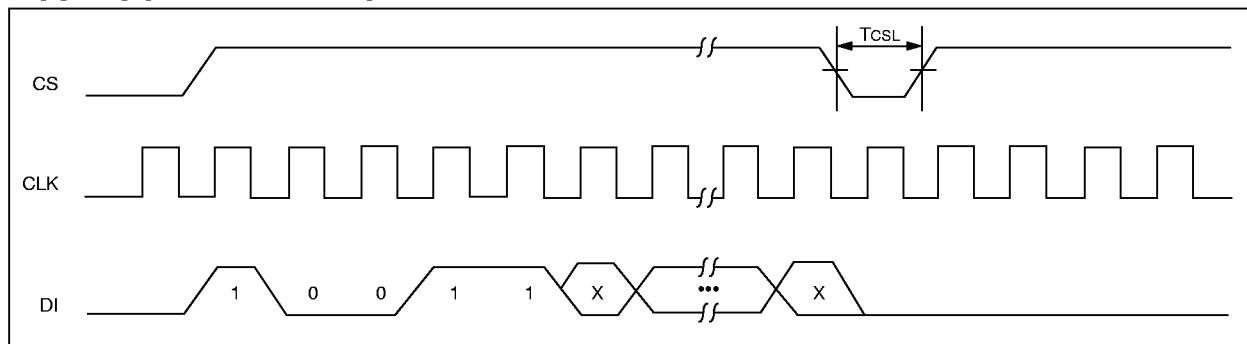
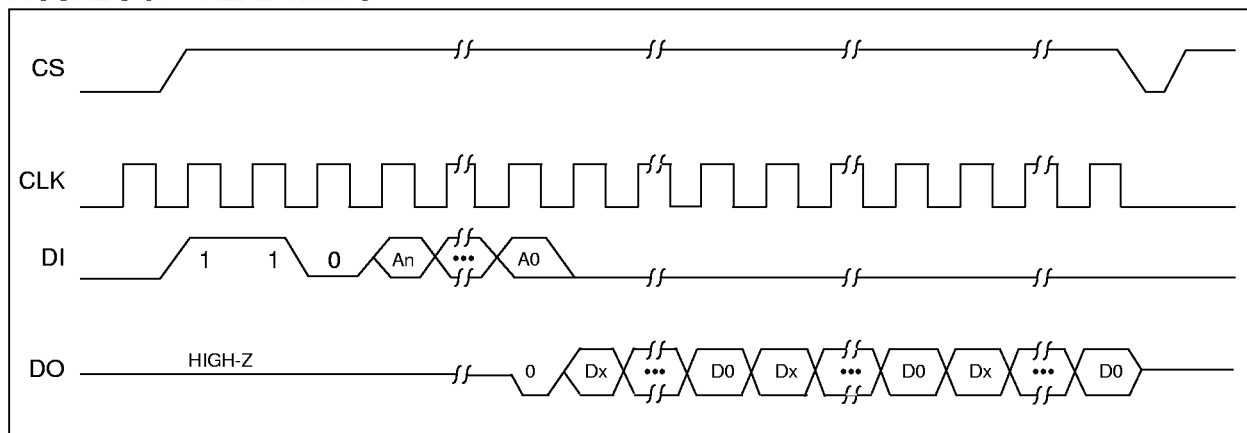


FIGURE 3-6: READ TIMING



3.8 WRITE

The WRITE instruction is followed by 8 bits (93LC66A) or 16 bits (93LC66B) of data which are written into the specified address. After the last data bit is put on the DI pin, the falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the $\overline{\text{READY}}/\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (T_{CSL}) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

3.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

The DO pin indicates the $\overline{\text{READY}}/\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}).

FIGURE 3-7: WRITE TIMING

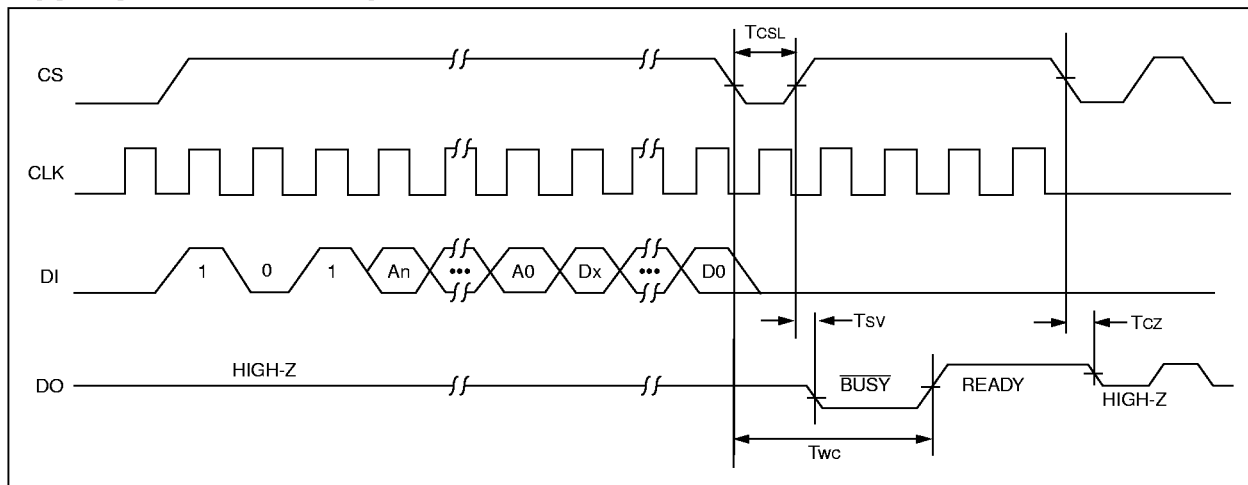
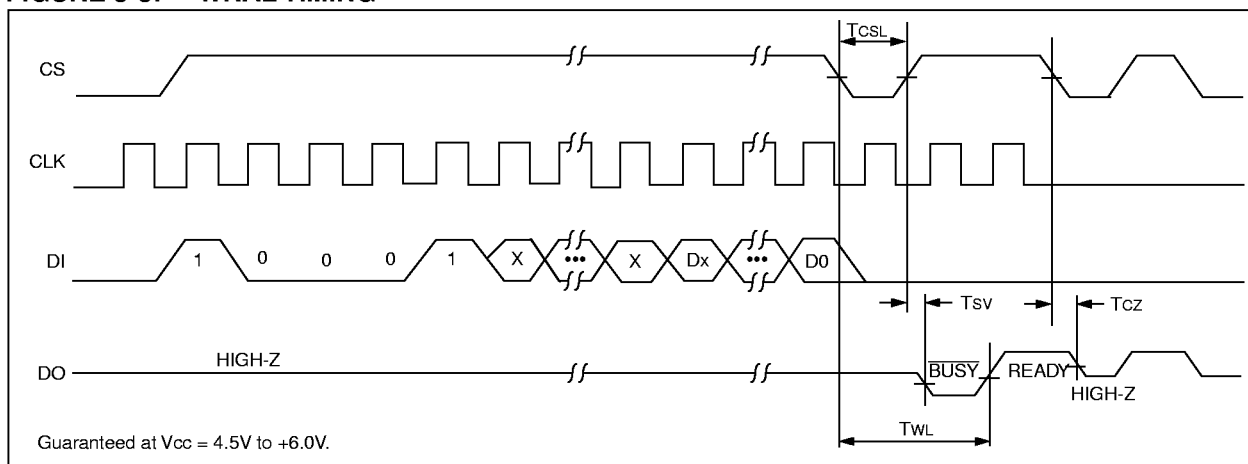


FIGURE 3-8: WRAL TIMING



93LC66A/B

NOTES:

NOTES:

93LC66A/B

NOTES:

93LC66A/B PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

93LC66A/B —	/P	Package:	P = Plastic DIP (300 mil Body), 8-lead
			SN = Plastic SOIC (150 mil Body), 8-lead
		Temperature Range:	SM = Plastic SOIC (208 mil Body), 8-lead
			ST = TSSOP, 8-lead
		Temperature Range:	Blank = 0 °C to +70 °C
			I = -40 °C to +85 °C
		Device:	93LC66A 4K Microwire Serial EEPROM (x8)
			93LC66AT 4K Microwire Serial EEPROM (x8) Tape and Reel
		Device:	93LC66AX 4K Microwire Serial EEPROM (x8) in alternate pinout (SN only)
			93LC66AXT 4K Microwire Serial EEPROM (x8) in alternate pinout, Tape and Reel (SN only)
		Device:	93LC66B 4K Microwire Serial EEPROM (x16)
			93LC66BT 4K Microwire Serial EEPROM (x16) Tape and Reel
		Device:	93LC66BX 4K Microwire Serial EEPROM (x16) in alternate pinout (SN only)
			93LC66BXT 4K Microwire Serial EEPROM (x16) in alternate pinout, Tape and Reel (SN only)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

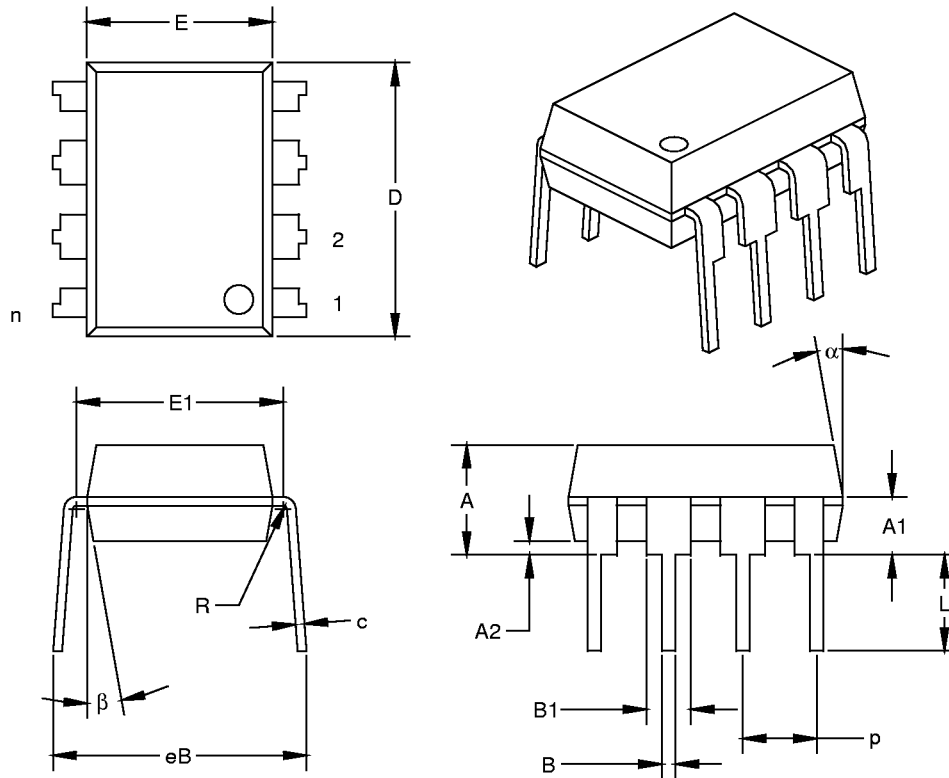
1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)



MICROCHIP

Packaging Diagrams and Parameters

Package Type: K04-018 8-Lead Plastic Dual In-line (P) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		8			8	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.014	0.018	0.022	0.36	0.46	0.56
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.006	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.140	0.150	0.160	3.56	3.81	4.06
Top of Lead to Seating Plane	A1	0.060	0.080	0.100	1.52	2.03	2.54
Base to Seating Plane	A2	0.005	0.020	0.035	0.13	0.51	0.89
Tip to Seating Plane	L	0.120	0.130	0.140	3.05	3.30	3.56
Package Length	D‡	0.355	0.370	0.385	9.02	9.40	9.78
Molded Package Width	E‡	0.245	0.250	0.260	6.22	6.35	6.60
Radius to Radius Width	E1	0.267	0.280	0.292	6.78	7.10	7.42
Overall Row Spacing	eB	0.310	0.342	0.380	7.87	8.67	9.65
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

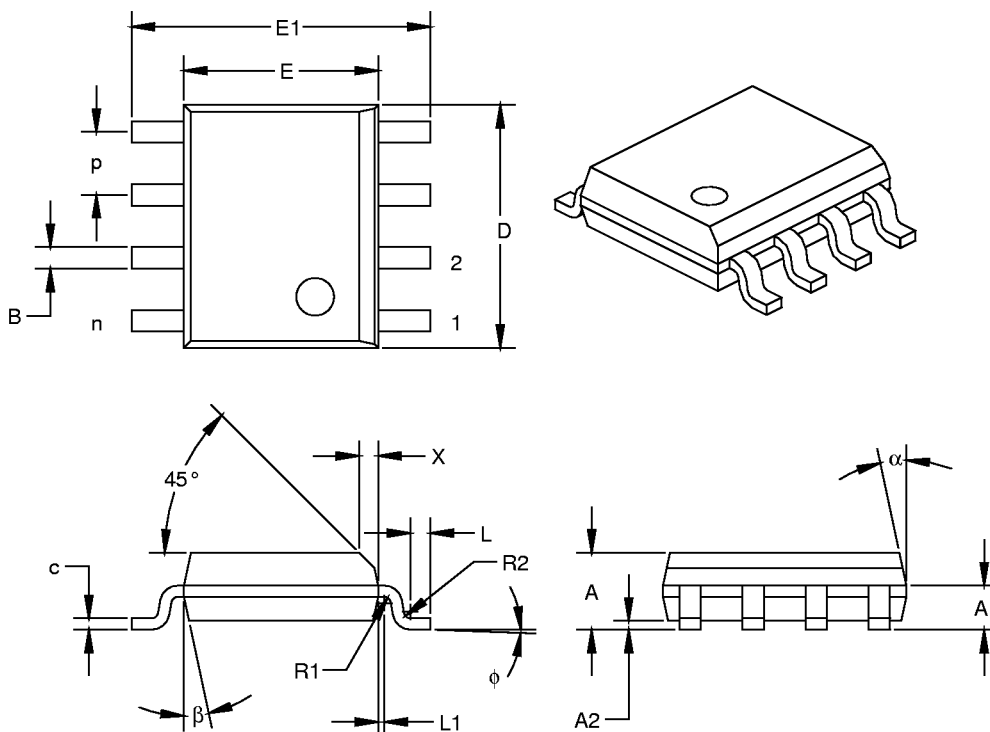
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-001 BA

Packaging Diagrams and Parameters

Package Type: K04-057 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		8			8	
Overall Pack. Height	A	0.054	0.061	0.069	1.37	1.56	1.75
Shoulder Height	A1	0.027	0.035	0.044	0.69	0.90	1.11
Standoff	A2	0.004	0.007	0.010	0.10	0.18	0.25
Molded Package Length	D [‡]	0.189	0.193	0.196	4.80	4.89	4.98
Molded Package Width	E [‡]	0.150	0.154	0.157	3.81	3.90	3.99
Outside Dimension	E1	0.229	0.237	0.244	5.82	6.01	6.20
Chamfer Distance	X	0.010	0.015	0.020	0.25	0.38	0.51
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.009	0.010	0.19	0.22	0.25
Lower Lead Width	B [†]	0.014	0.017	0.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

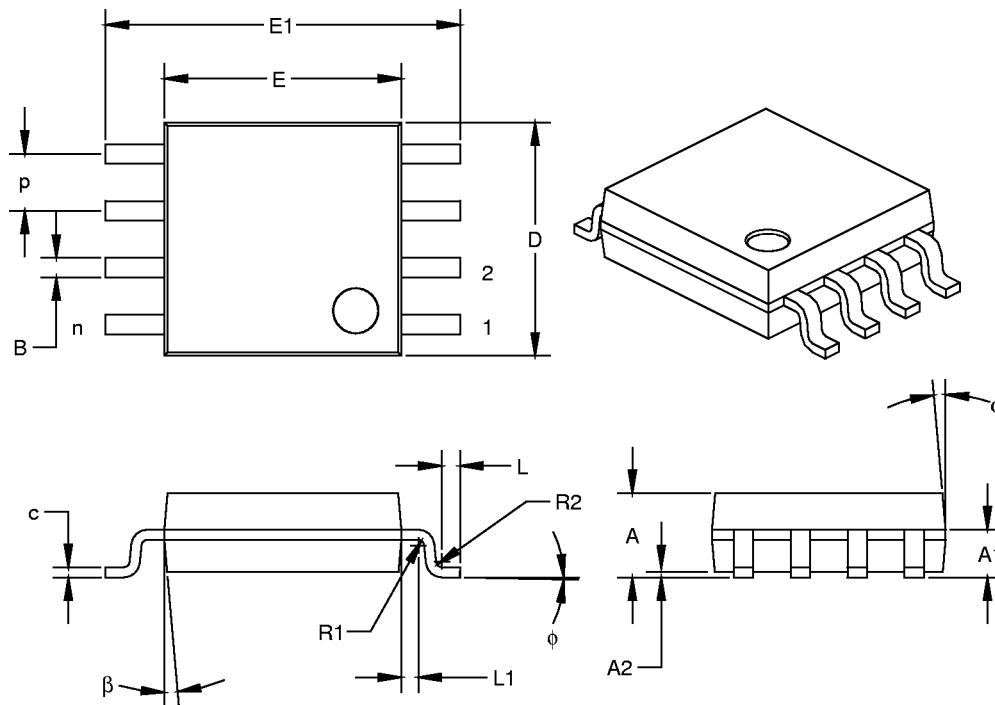
JEDEC equivalent: MS-012 AA



MICROCHIP

Packaging Diagrams and Parameters

Package Type: K04-056 8-Lead Plastic Small Outline (SM) – Medium, 208 mil



Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		8			8	
Overall Pack. Height	A	0.070	0.074	0.079	1.78	1.89	2.00
Shoulder Height	A1	0.037	0.042	0.048	0.94	1.08	1.21
Standoff	A2	0.002	0.005	0.009	0.05	0.14	0.22
Molded Package Length	D [‡]	0.200	0.205	0.210	5.08	5.21	5.33
Molded Package Width	E [‡]	0.203	0.208	0.213	5.16	5.28	5.41
Outside Dimension	E1	0.300	0.313	0.325	7.62	7.94	8.26
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	phi	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.008	0.009	0.010	0.19	0.22	0.25
Lower Lead Width	B [†]	0.014	0.017	0.020	0.36	0.43	0.51
Mold Draft Angle Top	alpha	0	12	15	0	12	15
Mold Draft Angle Bottom	beta	0	12	15	0	12	15

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

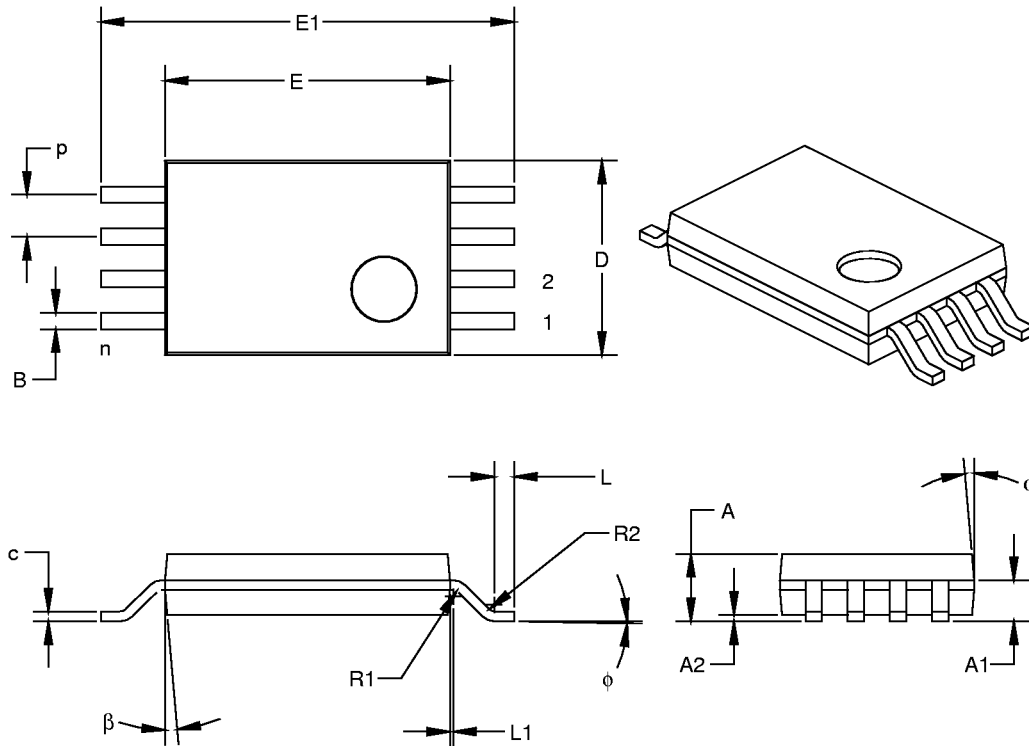
‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."



MICROCHIP

Packaging Diagrams and Parameters

Package Type: K04-086 8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.026			0.65	
Number of Pins	n		8			8	
Overall Package Height	A	0.039	0.041	0.043	1.00	1.05	1.10
Shoulder Height	A1	0.020	0.025	0.030	0.51	0.64	0.76
Standoff	A2	0.002	0.004	0.006	0.05	0.10	0.15
Molded Package Length	D†	0.114	0.118	0.122	2.90	3.00	3.10
Molded Package Width	E‡	0.169	0.173	0.177	4.30	4.40	4.50
Outside Dimension	E1	0.246	0.251	0.256	6.25	6.38	6.50
Shoulder Radius	R1	0.000	0.004	0.010	0.00	0.10	0.25
Gull Wing Radius	R2	0.000	0.004	0.010	0.00	0.10	0.25
Foot Length	L	0.007	0.012	0.017	0.18	0.30	0.43
Foot Angle	phi	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.002	0.005	0.00	0.05	0.13
Lead Thickness	c	0.004	0.006	0.008	0.09	0.15	0.20
Lower Lead Width	B†	0.007	0.010	0.012	0.19	0.25	0.30
Mold Draft Angle Top	alpha	0	5	10	0	5	10
Mold Draft Angle Bottom	beta	0	5	10	0	5	10

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-153 AA