National Semiconductor

Programmable Array Logic (PAL®) 24-Pin Polarity PAL Family—Series B

General Description

The PAL family utilizes National Semiconductor's advanced oxide isolated Schottky TTL process and bipolar PROM fusible-link technology to provide user-programmable logic to replace conventional SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PAL devices is greater than 4:1.

The family lets the systems engineer customize his chip by opening fusible links to configure AND and OR gates to perform his desired logic functions. Complex interconnections that previously required time-consuming layout are thus transferred from PC board to silicon where they can be easily modified during prototype checkout or production.

The PAL transfer function is the familiar sum of products with a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array. (The PROM is a fixed AND array driving a programmable OR array). In addition, the PAL family offers the options of having variable input/output ratios, programmable TRI-STATE® outputs and having registers with feedback.

The programmable output polarity feature allows the user to program individual outputs either active high or active low. This feature eliminates any possible need for inversion of signals outside the device.

Registers consist of D-type flip-flops that are loaded on the low-to-high transition of the clock. The registers power up with a high (V_{OH}) at the output pin, regardless of the polarity fuse.

The entire PAL family is programmed on inexpensive conventional programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Features

- 15 ns maximum propagation delay (combinatorial)
- User-programmable replacement for TTL logic
- Large variety of JEDEC-compatible programming equipment and design development software available
- Fully supported by National PLAN™ development software
- Power-up reset for registered outputs
- Register preload facilitates device testing
- Security fuse prevents direct copying of logic patterns
- Skinny DIP packages

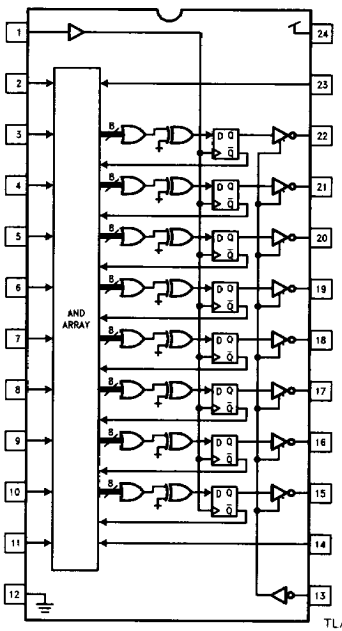
Device Types

Part Number	Dedicated Inputs	Registered Outputs (With Feedback)	Combinatorial	
			I/Os	Outputs
PAL20P8B	14	—	6	2
PAL20RP4B	12	4	4	—
PAL20RP6B	12	6	2	—
PAL20RP8B	12	8	—	—

Speed/Power Versions

Series	Example	Commercial		Military	
		t_{PD}	I_{CC}	t_{PD}	I_{CC}
B	PAL 20P8B	15 ns	210 mA	20 ns	210 mA

Block Diagram—PAL20RP8B



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Series-B (PAL20P8B, PAL20RP4B, PAL20RP6B, PAL20RP8B)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.5V to +5.5V
Off-State Output Voltage (Note 2)	−1.5V to +5.5V
Input Current (Note 2)	−30 mA to +5.0 mA
Output Current (I_{OL})	+100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C
ESD Tolerance	2000V
C_{ZAP} = 100 pF R_{ZAP} = 1500Ω Test Method: Human Body Model Test Specification: NSC SOP-5-028	

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55			0		75	°C
T_C	Operating Case Temperature				125				°C
t_W	Clock Pulse Width	Low	12	5		10	5		ns
		High	12	5		10	5		ns
t_{SU}	Setup Time from Input or Feedback to Clock		20	10		15	10		ns
t_H	Hold Time of Input after Clock		0	−8		0	−8		ns
f_{CLK}	Clock Frequency (Note 3)	With Feedback			28.6			37	MHz
		Without Feedback			41.7			50	MHz

Electrical Characteristics Over Recommended Operating Conditions (Note 4)

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 5)						0.8	V
V_{IH}	High Level Input Voltage (Note 5)				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I = −18 mA				−0.8	−1.5	V
I_{IL}	Low Level Input Current (Note 6)	V_{CC} = Max, V_I = 0.4V				−0.04	−0.25	mA
I_{IH}	High Level Input Current (Note 6)	V_{CC} = Max, V_I = 2.4V					25	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 12 mA	MIL		0.3	0.5	V
			I_{OL} = 24 mA	COM				
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA	MIL	2.4	3.4		V
			I_{OH} = −3.2 mA	COM				
I_{OZL}	Low Level Off-State Output Current (Note 6)	V_{CC} = Max	V_O = 0.4V				−100	μA
I_{OZH}	High Level Off-State Output Current (Note 6)	V_{CC} = Max	V_O = 2.4V				100	μA
I_{OS}	Output Short-Circuit Current (Note 7)	V_{CC} = 5V, V_O = 0V			−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open				140	210	mA

Series-B (PAL20P8B, PAL20RP4B, PAL20RP6B, PAL20RP8B) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: f_{CLK} with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.
f_{CLK} without feedback is derived as $(2t_W)^{-1}$.

Note 4: All typical values are for $V_{CC} = 5.0V$ and $T_A = 25°C$.

Note 5: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

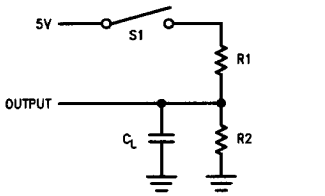
Note 6: Leakage current for bidirectional I/O pins is the worst case between I_{IL} and I_{OZL} or between I_{IH} and I_{OZH}.

Note 7: To avoid invalid readings in other parameter tests it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Military			Commerical			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Combinatorial Output	C_L = 50 pF, S1 Closed		11	20		11	15	ns
t_{CLK}	Clock to Registered Output or Feedback	C_L = 50 pF, S1 Closed		8	15		8	12	ns
t_{PZXG}	$\overline{G}$ Pin to Registered Output Enabled	C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed		10	20		10	15	ns
t_{PXZG}	$\overline{G}$ Pin to Registered Output Disabled	C_L = 5 pF, from V_{OH}: S1 Open, from V_{OL}: S1 Closed		11	20		11	15	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed		10	20		10	15	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	C_L = 5 pF, from V_{OH}: S1 Open, from V_{OL}: S1 Closed		11	20		11	15	ns
t_{RESET}	Power-Up to Registered Output High			600	1000		600	1000	ns

Test Load



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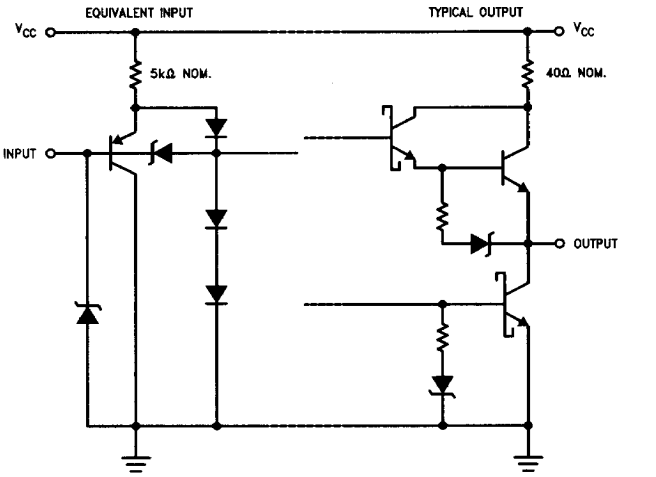
MIL	COM'L
R1 = 390	R1 = 200
R2 = 750	R2 = 390

Schematic of Inputs and Outputs



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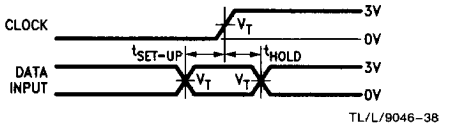
Test Waveforms

Set-Up and Hold



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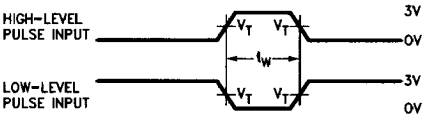
Pulse Width



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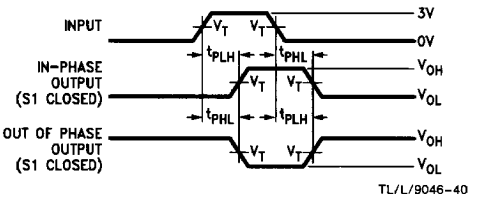
Propagation Delay



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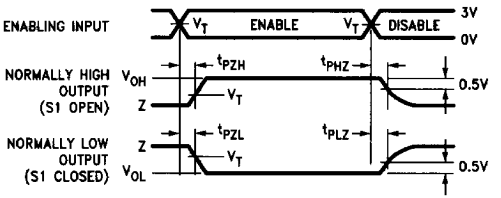
Enable and Disable



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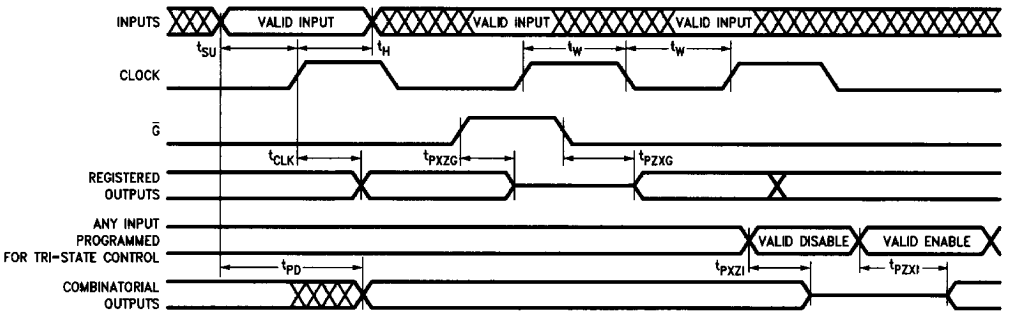
Notes:

V_T = 1.5V

C_L includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms



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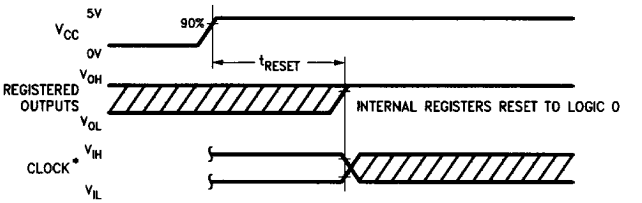
Power-Up Reset Waveform



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*The clock input should not be switched from low to high until after time t_{RESET}.

Functional Description

All of the 24-pin Polarity PAL logic arrays consist of 20 complementary input lines and 64 product-term lines with a programmable fuse link at each intersection (2560 fuses). The product terms are organized into eight groups of eight each. Seven or eight of the product terms in each group connect into an OR-gate to produce the sum-of-products logic function, depending on whether the output is combinatorial or registered.

An unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses) are in the high logic state. Therefore, if both the true and complement of at least one array input is left connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed device). Conversely, if all fuses on a product term were programmed, the product term and the resulting logic function would be held in the high state.

The Polarity PAL family consists of four device types with differing mixtures of combinatorial and registered outputs. The 20P8, 20RP4, 20RP6 and 20RP8 architectures have 0, 4, 6 and 8 registered outputs, respectively, with the balance of the 8 outputs combinatorial. All outputs have TRI-STATE capability.

Each combinatorial output has a seven product-term logic function, with the eighth product term being used for TRI-STATE control. A combinatorial output is enabled while the TRI-STATE product term is satisfied (true). Combinatorial outputs also have feedback paths from the device pins into the logic array (except for two outputs on the 20P8). This allows a pin to perform bidirectional I/O or, if the associated logic function were left unprogrammed, the output driver would remain disabled and the pin could be used as an additional dedicated input.

Registered outputs each have an eight product-term logic function feeding into a D-type flip-flop. All registers are triggered by the high-going edge of the clock input pin. All registered outputs are controlled by a common output enable ($\overline{G}$) pin (enabled while low). The output of each register is also fed back into the logic array via an internal path. This provides for sequential logic circuits (state machines, counters, etc.) which can be sequenced even while the outputs are disabled.

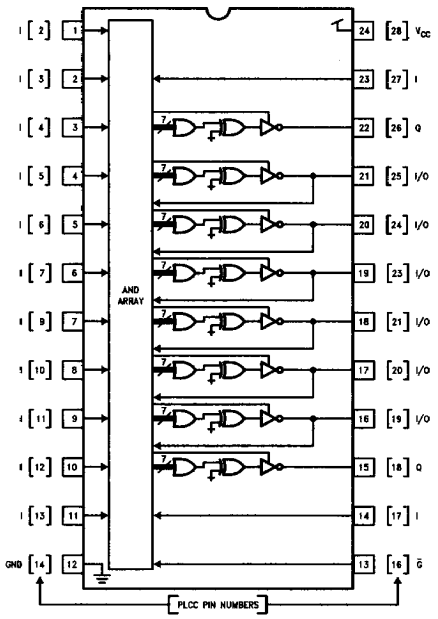
The programmable polarity feature controls active-high and active-low polarity on individual output pins, eliminating the need for external inverters. When the programmable polarity selection fuse is left unprogrammed, the output pin is active-low. When the fuse is programmed, the output pin is active-high. Polarity inversions occur before any output registers.

Series-B Polarity PAL devices reset all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled regardless of the state of the polarity fuses). This may simplify sequential circuit design and test. To ensure successful power-up reset, V_{CC} must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, V_{OL}, V_{OH}, or resistively to V_{CC}. However, switching any input not connected to a product term or logic function has no effect on its output logic state.

24-Pin Polarity PAL Family Block Diagrams—DIP Connections

PAL20P8



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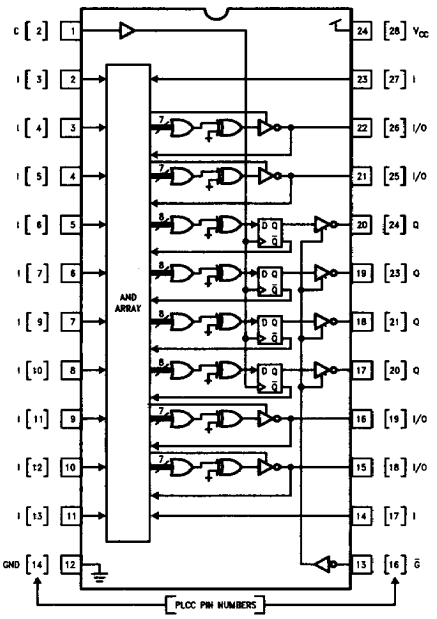
PAL20RP4



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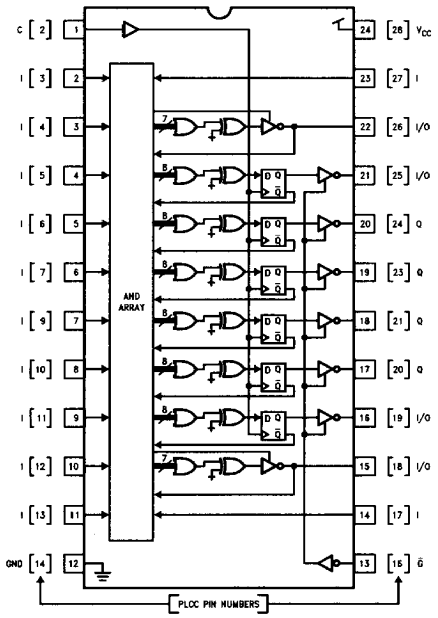
PAL20RP6



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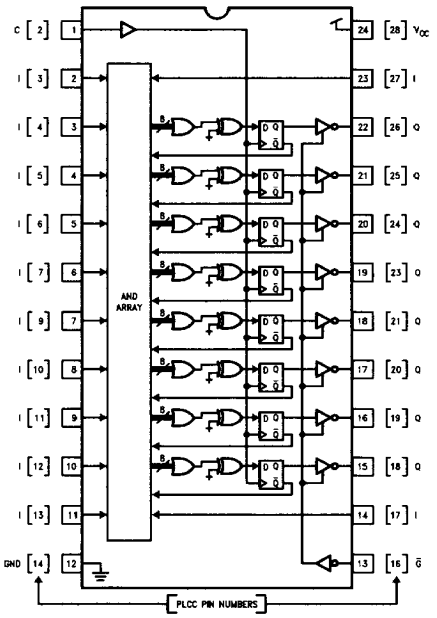
PAL20RP8



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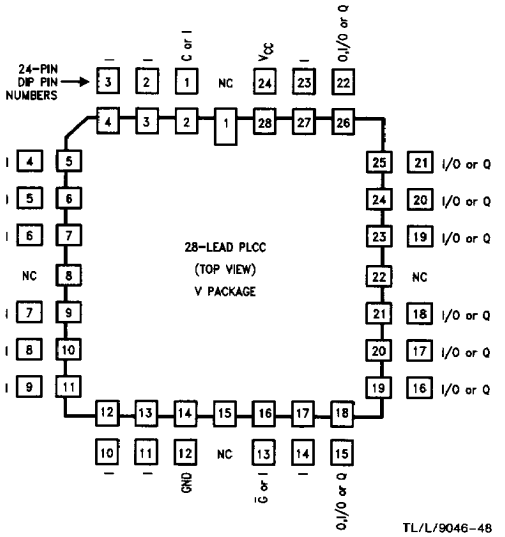
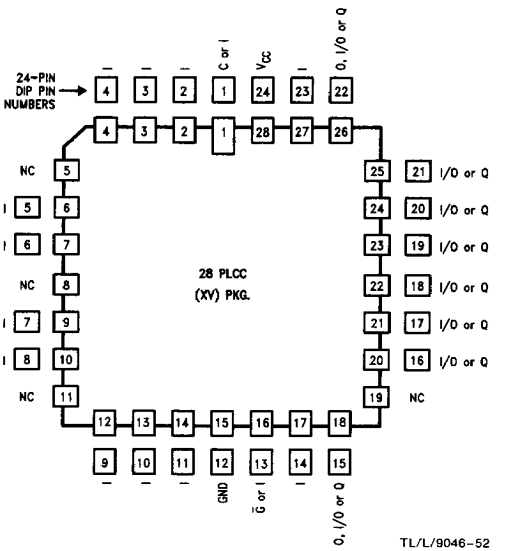
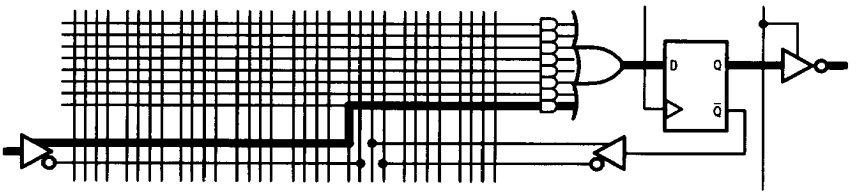
28-Lead PLCC Connection Conversion Diagram



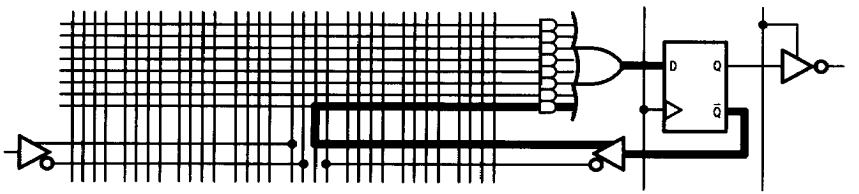
Non-JEDEC PLCC Diagram



Typical Registered Logic Function Without Feedback



Typical Registered Logic Function With Feedback



Functional Description (Continued)

CLOCK FREQUENCY SPECIFICATION

The clock frequency (f_{CLK}) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum clock period (t_W high + t_W low) and the minimum "data window" period (t_{SU} + t_H). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (f_{CLK}^{-1} with feedback) is defined as t_{CLK} + t_{SU}. This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the inputs to the registers before the end of each cycle.

Output Register Preload

The preload function allows the registers to be loaded asynchronously from data placed on the output pins. This feature simplifies device testing since any state may be loaded into the registers at any time during the functional test sequence. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. Register preload is not an operational mode and is not intended for board level testing because elevated voltage levels are required. The programming system normally provides the preload capability as part of its functional test facility.

The register preload procedure is as follows:

1. V_{CC} is raised to 4.5V.
2. Registered outputs are disabled by raising output enable ($\overline{G}$) to V_{IH}.
3. The desired data values are applied to all registered output pins (V_{IL} = set, V_{IH} = reset).
4. DIP pin 23 (PCC pin 27) is pulsed to V_P, then back to V_{IL}. (V_P = 18.0V ±0.5V).
5. Data inputs are removed from registered output pins.
6. $\overline{G}$ is lowered to V_{IL} to enable registered outputs.
7. The desired data values are verified at all registered outputs (V_{OL} = set, V_{OH} = reset).

Note: The minimum recommended time delay (t_D) between successive input transitions (including the V_P pulse width on DIP pin 8) is 100 ns.

Security Fuse

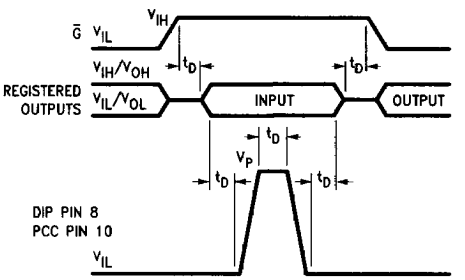
Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.

Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a large variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the 24-pin Polarity PAL family are provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Register Preload Waveform



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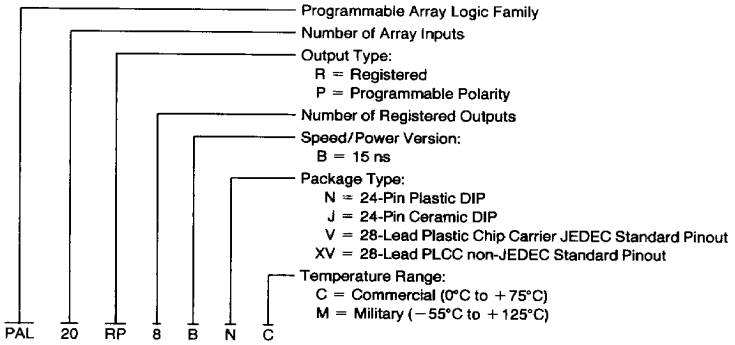
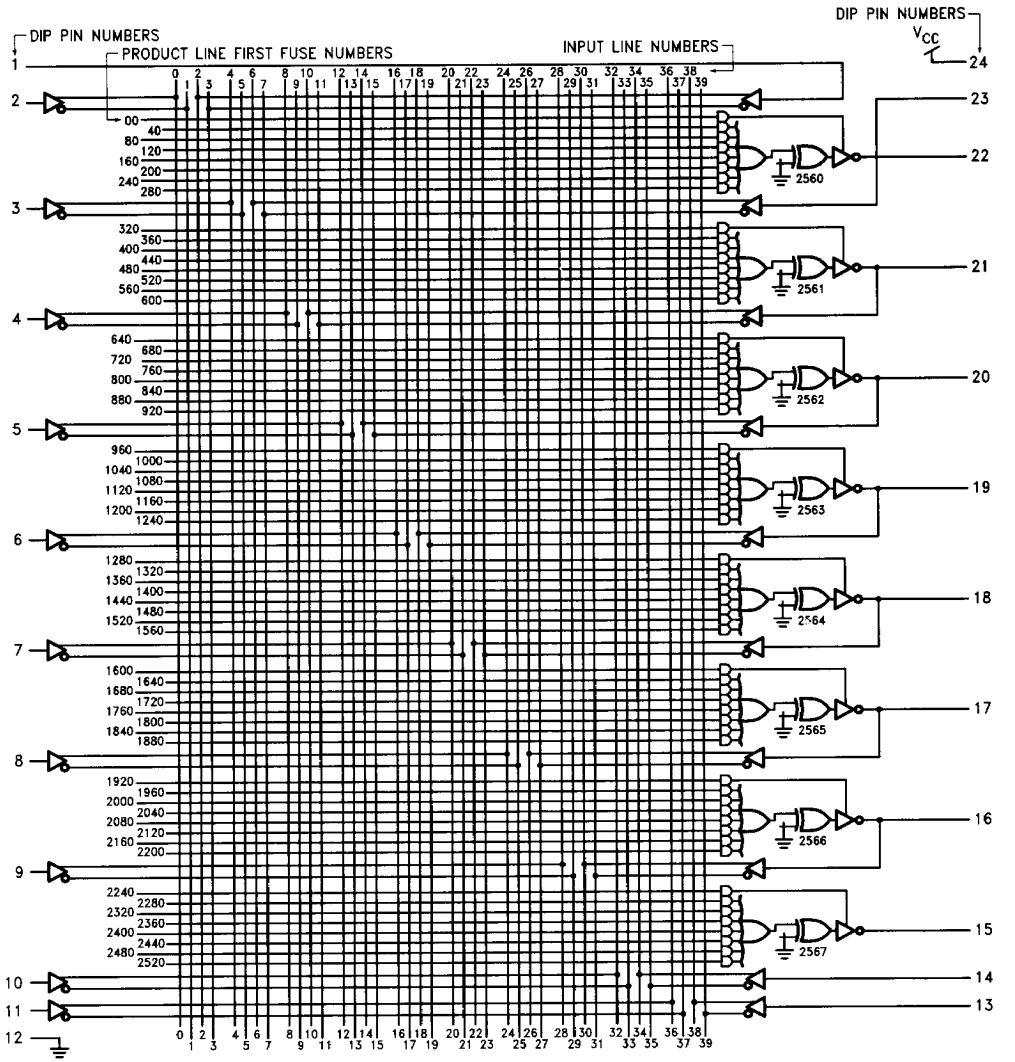
Note: V_P = 18.0V ±0.5V, t_D min. = 100 ns

Ordering Information



Logic Diagram—PAL20P8B



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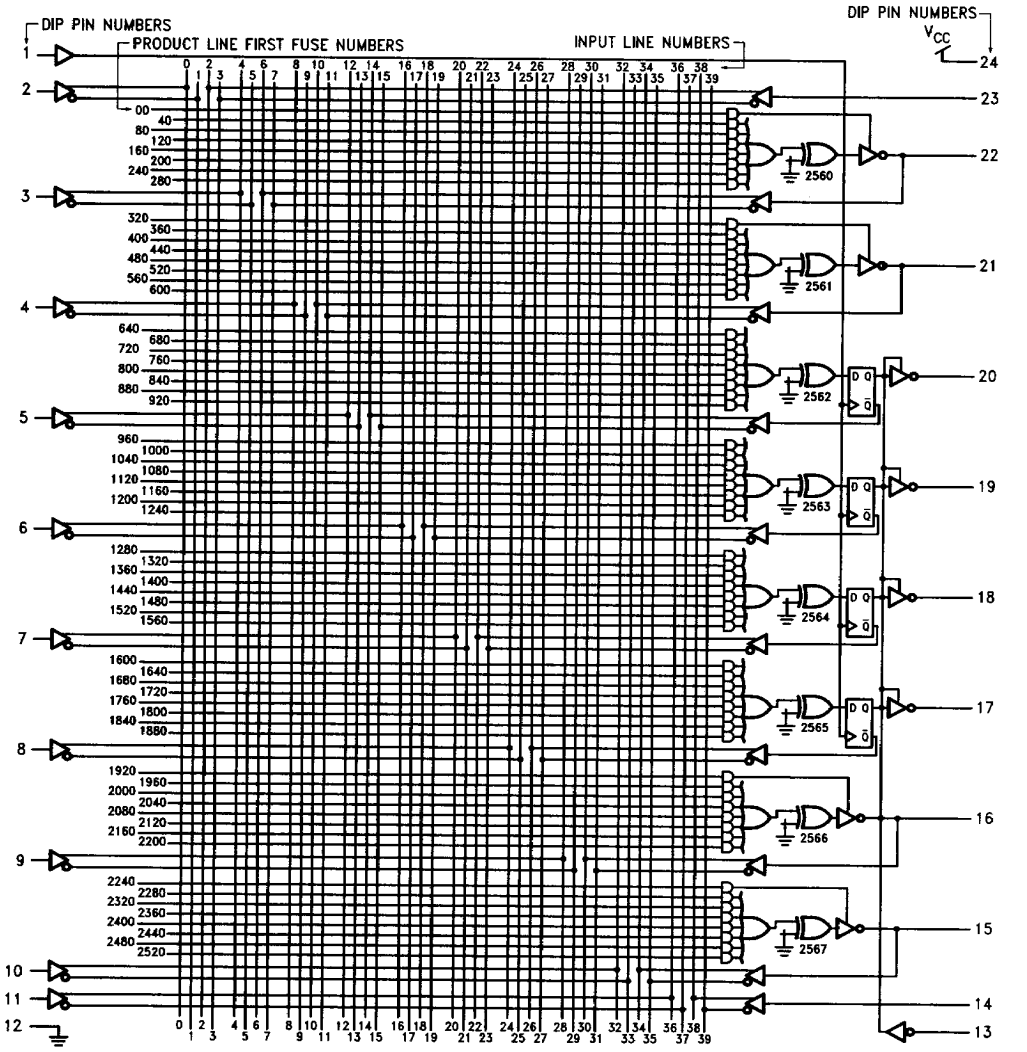
JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

Logic Diagram—PAL20RP4B



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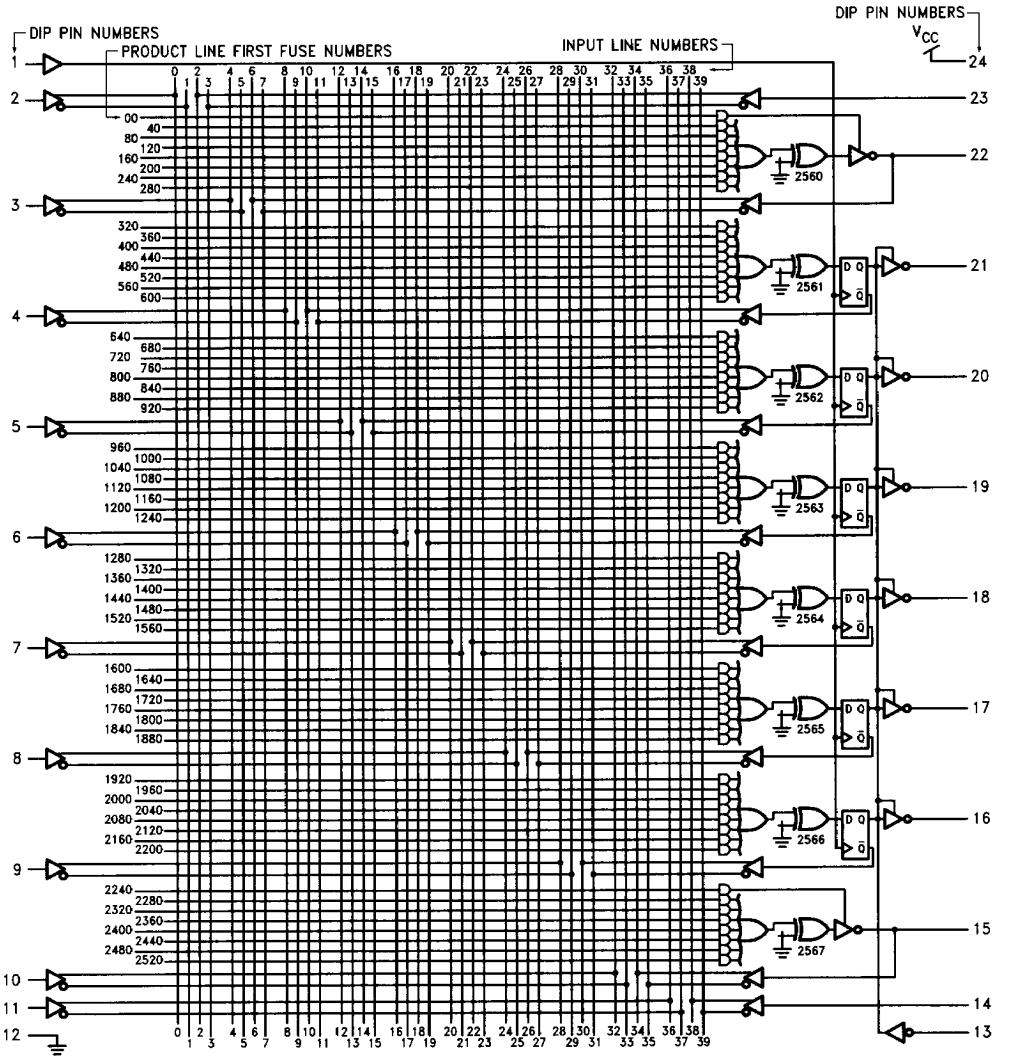
JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

Logic Diagram—PAL20RP6B



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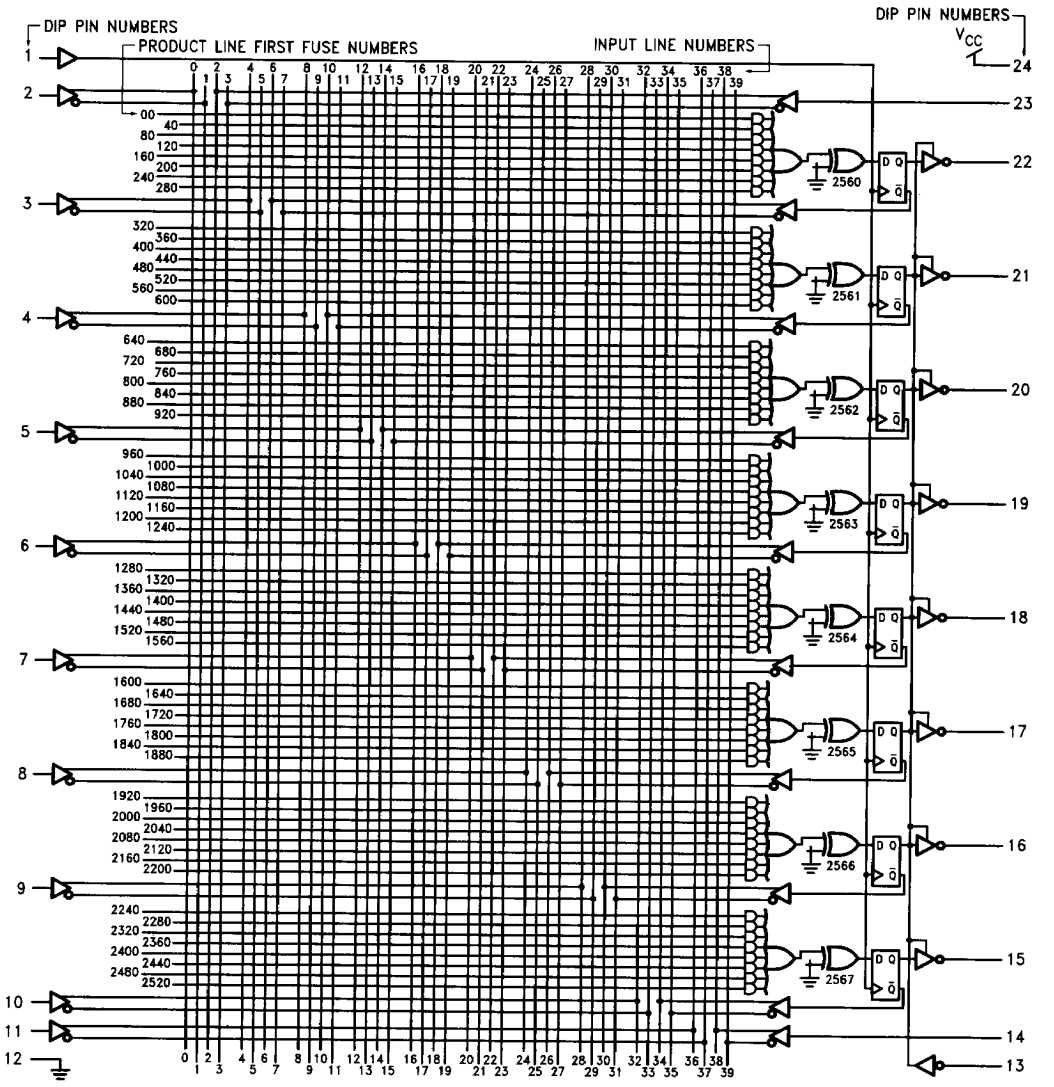
JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

Logic Diagram—PAL20RP8B



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JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.