National Semiconductor

PRELIMINARY
May 1991

Programmable Array Logic (PAL®) 24-Pin Medium PAL Series -7 and -5

General Description

The 24-pin medium PAL family contains four of the most popular PAL architectures with speeds as fast as 5 ns maximum propagation delay. Series -7 and -5 devices are manufactured using National Semiconductor's proprietary ASPECT™ II TTL process with highly reliable "vertical-fuse" programmable cells. Vertical fuses are implemented using avalanche-induced migration (AIM™) technology offering very high programming yields. The 24-pin medium PAL family provides high-speed user-programmable replacements for conventional SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming the programmable cells to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

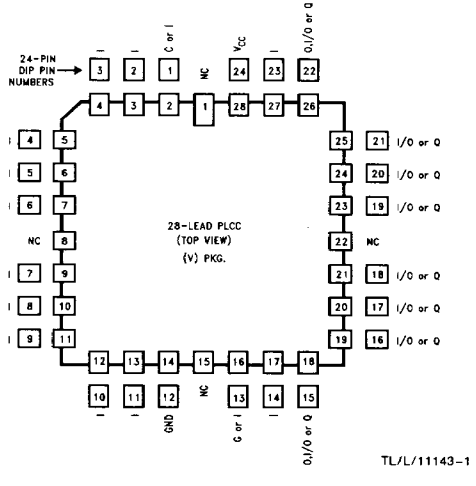
The PAL logic array has a total of 20 complementary input pairs and 8 outputs generated by a single programmable AND gate array with fixed OR-gate connections. Device outputs are either taken directly from the AND-OR functions (combinatorial) or passd through D-type flip-flops (registered). Registers allow the PAL device to implement sequential logic circuits. TRI-STATE® outputs facilitate busing and provide bidirectional I/O capability. The medium PAL family offers a variety of combinatorial and registered output mixtures.

On power-up series -7 and -5 devices reset all registers to simplify sequential circuit design and testing, direct register preload is also provided to facilitate device testing. Security fuses can be programmed to prevent direct copying of proprietary logic patterns.

Features

- 5 ns maximum propagation delay (combinatorial outputs)
- Pin compatible with existing PAL families
- High programming yield and reliability of vertical-fuse AIM technology
- Supported by industry standard programming equipment and design development software
- Fully supported by National's OPAL™ and OPAL jr. software
- Power-up reset for registered outputs
- Register preload facilitates device testing
- User programmable replacement for high speed TTL Logic
- Security fuse prevents direct copying of logic patterns
- High noise immunity DIP package

28-Lead PLCC Connection Conversion Diagram



Block Diagram—PAL20R8

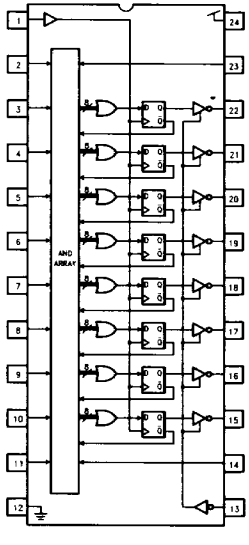


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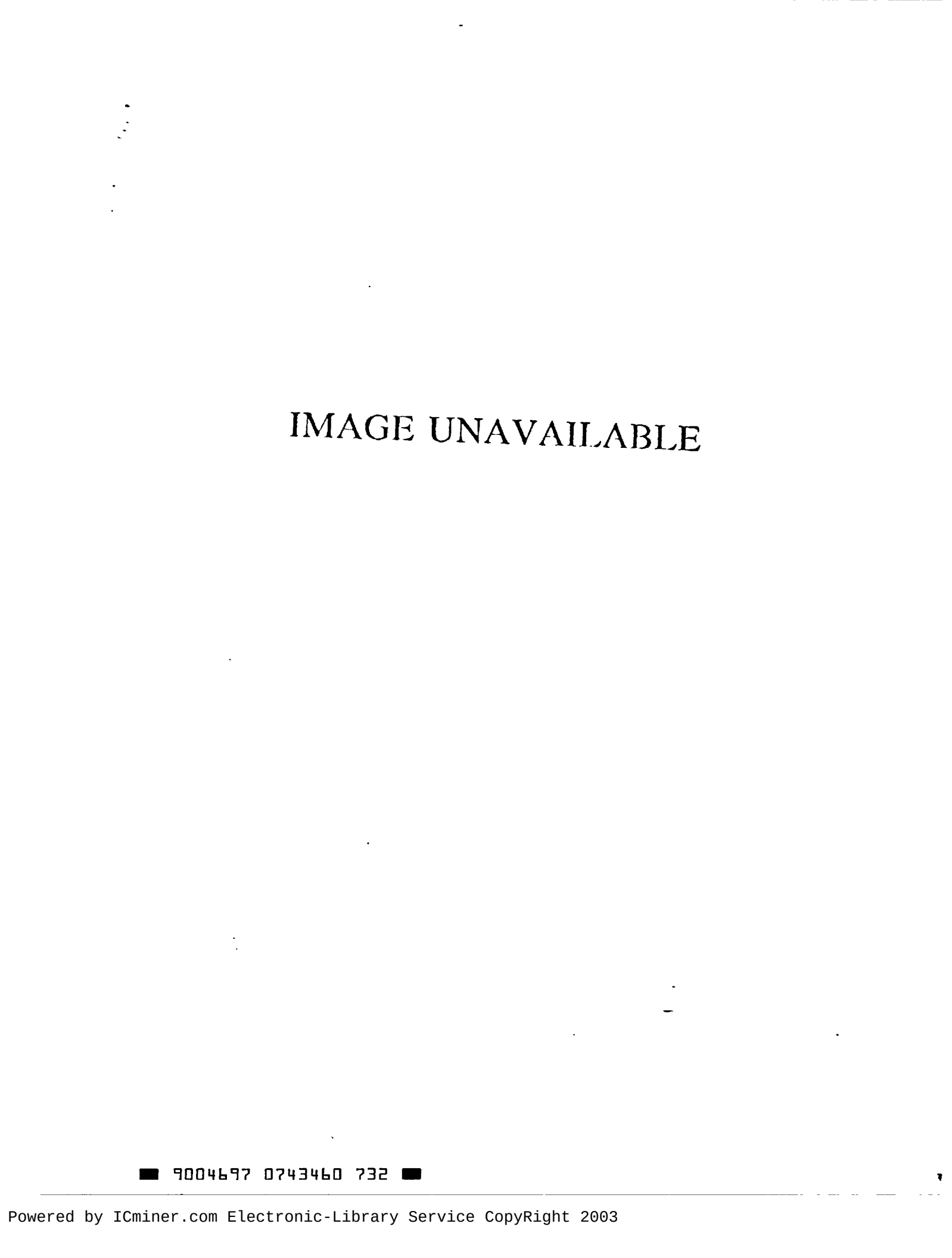
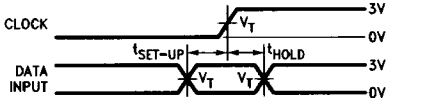
IMAGE UNAVAILABLE



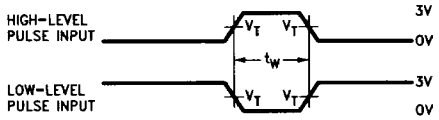
Test Waveforms

Set-Up and Hold



TL/L/11143-7

Pulse Width



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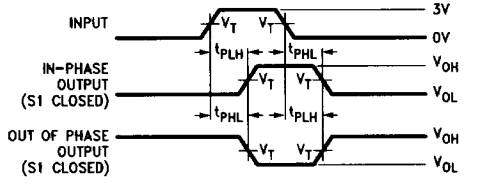
Propagation Delay



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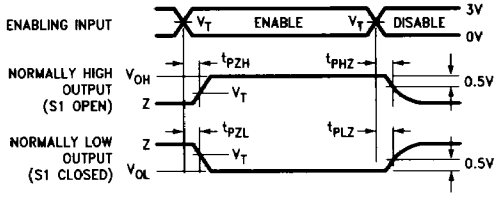
Enable and Disable



TL/L/11143-10

Notes:

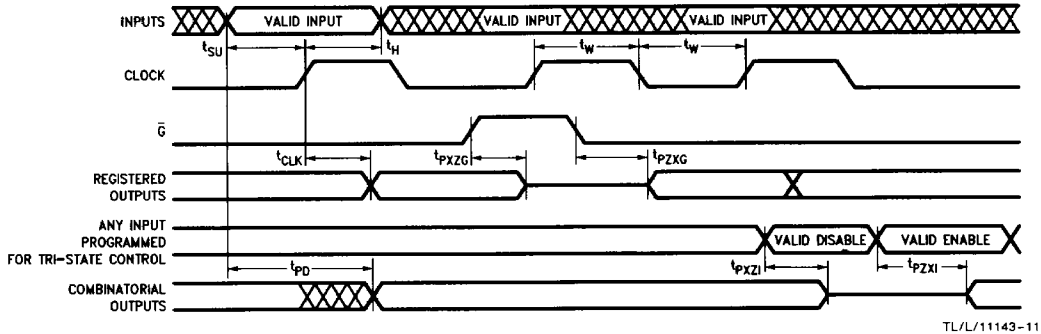
V_T = 1.5V

C_L includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

For all input pulses: $t_r = t_f \leq 2$ ns, duty cycle = 50%.

Switching Waveforms



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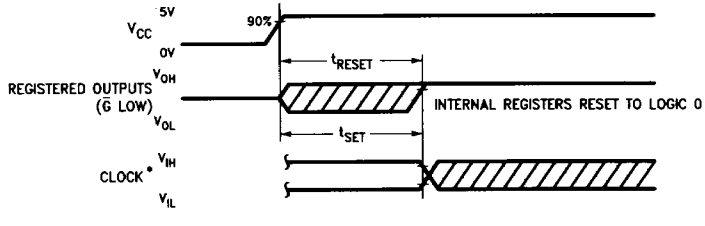
Power-Up Set/Reset Waveform



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*The clock input should not be switched from low to high until after time t_{RESET} or t_{SET}.

Functional Description

All of the 24-pin medium PAL logic arrays consist of 20 complementary input lines and 64 product-term lines with a programmable cell at each intersection (2560 cells). The product terms are organized into eight groups of eight each. Seven or eight of the product terms in each group connect into an OR-gate to produce the sum-of-products logic function, depending on whether the output is combinatorial or registered.

In the National Series -7 and -5 vertical fuse (AIM) PAL devices, a programmed vertical fuse cell establishes a connection between an input line and a product term. A product term is satisified (logically true) while all of the input lines connected to it (via unprogrammed fuses for the fuse-link devices, or by programming the corresponding cells for the vertical fuse devices) are in the high logic state. Therefore, if both the true and complement of at least one array input is connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed fuse-link device). Conversely, if all input lines are disconnected from a product line, the product term and the resulting logic function would be held in the high state (which is the state of all product terms in an unprogrammed National -7 and -5 PAL device). For more information on vertical fuse technology, consult our application note #594.

The medium PAL family consists of four device types with differing mixtures of combinatorial and registered outputs. The 20L8, 20R4, 20R6 and 20R8 architectures have 0, 4, 6 and 8 registered outputs respectively, with the balance of the 8 outputs combinatorial. All outputs are active-low and have TRI-STATE capability.

Each combinatorial output have a seven product-term logic function, with the eighth product term being used for TRI-STATE control. A combinatorial output is enabled while the TRI-STATE product term is satisfied (true). Combinatorial outputs also have feedback paths from the device pins into the logic array (except for two outputs on the 20L8). This allows a pin to perform bidirectional I/O or, if the associated TRI-STATE control product term were programmed to remain unsatisified (always false), the output driver would remain disabled and the pin could be used as an additional dedicated input.

Registered outputs each have an eight product-term logic function feeding into a D-type flip-flop. All registers are triggered by the high-going edge of the clock input pin. All registered outputs are controlled by a common output enable ($\overline{G}$) pin (enabled while low). The output of each register is also fed back into the logic array via an internal path. This provides for sequential logic circuits (state machines, counters, etc.) which can be sequenced even while the outputs are disabled.

Series -7 and -5 medium PAL devices reset all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. To ensure successful power-up reset, V_{CC} must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the set or reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

During power-up, all outputs are held in the high-impedance state until DC power supply conditions are met (V_{CC} approximately 3.0V), after which they may be enabled by the TRI-STATE control product terms (combinatorial outputs) or the $\overline{G}$ pin (registered outputs). Whenever V_{CC} goes below 3V (at 25°C), the outputs are disabled as shown in *Figure 1* below.

In an unprogrammed National Series -7 and -5 PAL devices, no array inputs are connected to any product-term lines. Therefore, all combinatorial outputs would be enabled and driving low logic levels (after power-up is completed). All registers would still initialize to the low state, but would become permanently set (low-level outputs, if enabled) following the first clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, V_{OL}, V_{OH}, or resistively to V_{CC}. However, switching any input not connected to a product term or logic function has no effect on its output logic state.

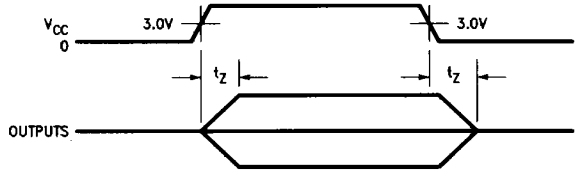

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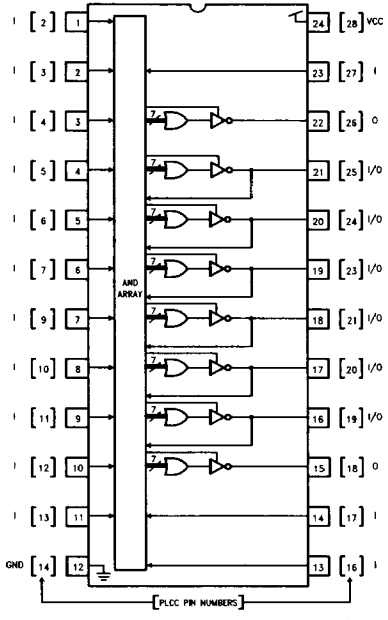
FIGURE 1. Power-Up TRI-STATE Waveform

24-Pin Medium PAL Family Block Diagrams—DIP Connections

PAL20L8



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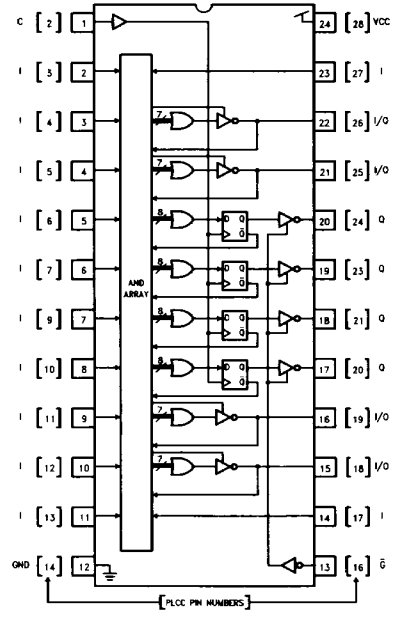
PAL20R4



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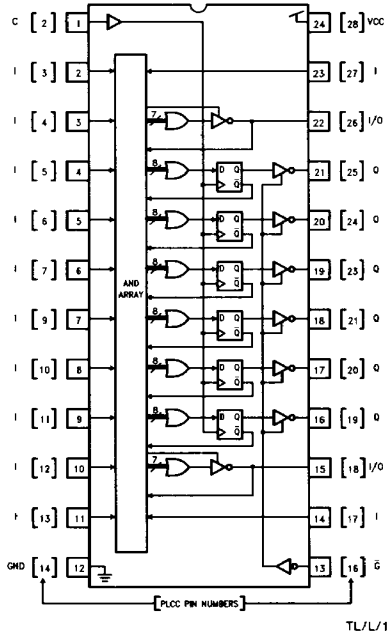
PAL20R6



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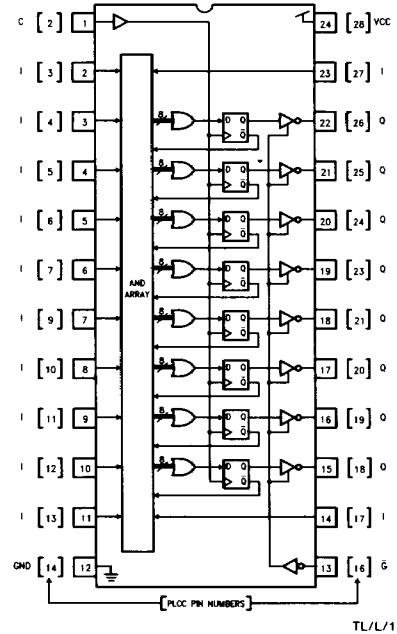
PAL20R8



TL/L/11143–17

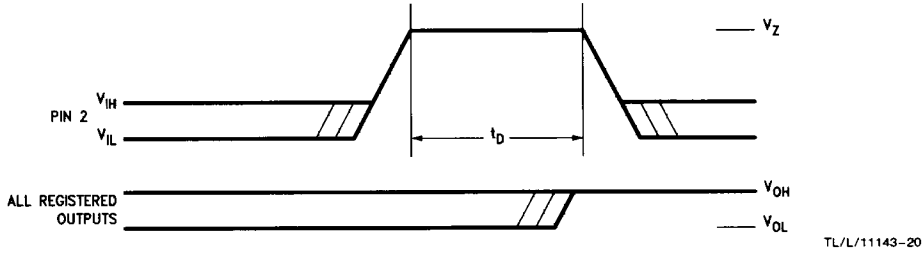
IMAGE UNAVAILABLE

Design Development Support (Continued)

In National Series -7 and -5 devices, logical and physical connections between array input lines and product-term lines are established when vertical fuse cells are programmed. This is opposite to other PAL products based on fusible links in which connections are established when fuses are left unprogrammed (intact). This difference is compensated by the vertical-fuse PAL programming algorithm so that the *user's design development process looks the same.* (The only functional difference due to vertical-fuse technology is the behavior of "unprogrammed" devices.) The JEDEC programming maps produced by PAL development software for all Medium PAL devices denote a "connection" with a "0", and a "non-connection" with a "1". The programming algorithms for most fuse-link PLDs program fuses where ones are located in the map to remove corresponding connections, whereas the algorithm for National Series PAL -7 and -5 products automatically compensates by programming vertical-fuse cells where zeroes are located in the map to establish connections. Therefore, the *same JEDEC map* representing the user's desired logic equations produces the *same functional results* when using either PAL technology. The user need only provide the appropriate device code and/or adapter for the programming equipment to invoke the proper programming algorithm. Only programmers with the certified National vertical-fuse PAL programming algorithm should be used to program these vertical-fuse devices.

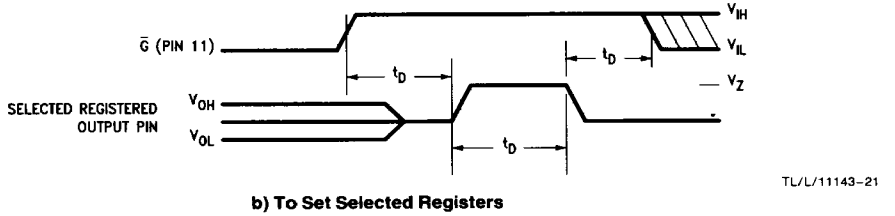
Detailed logic diagrams showing all JEDEC fuse-map addresses for the 24-pin medium PAL family are provided for direct map editing and diagnostic purposes. The DIP and PLCC package for -7 and -5 series are pin for pin replacements for all slower 24-pin medium PAL devices (A, B and D Series). For a list of current software and programming support tools available for theses devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Functional Description (Continued)



TL/L/11143–20

a) To Reset All Registers



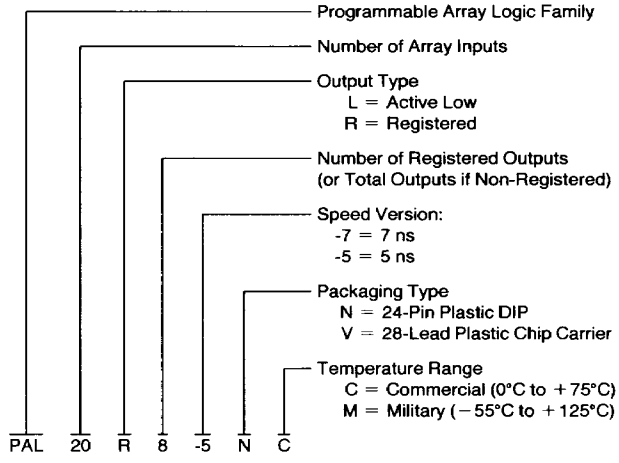
TL/L/11143–21

b) To Set Selected Registers

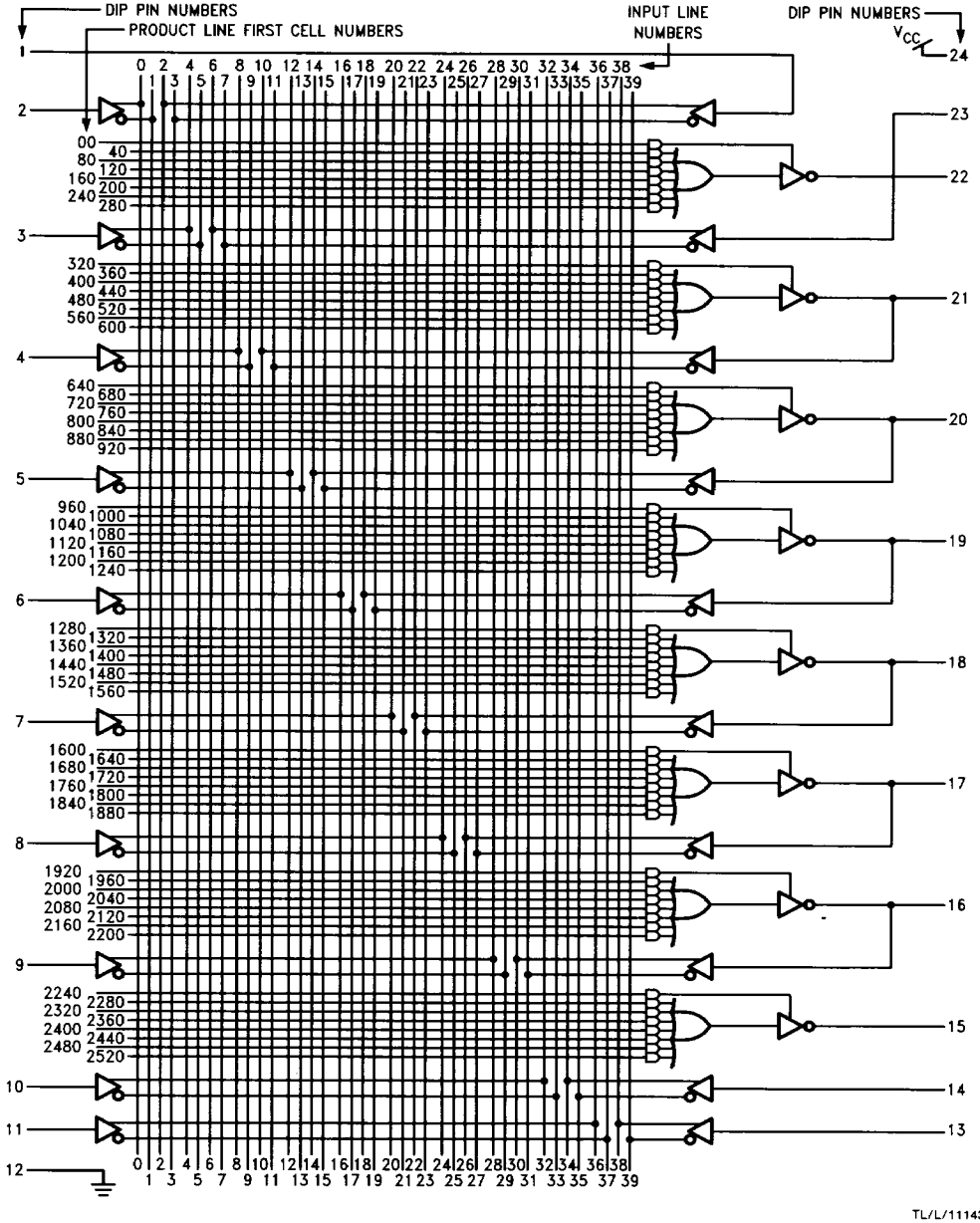
Note: V_Z = 9.5V to 10.0V, t_D min. = 500 ns

FIGURE 2. Register Preload Waveforms

Ordering Information



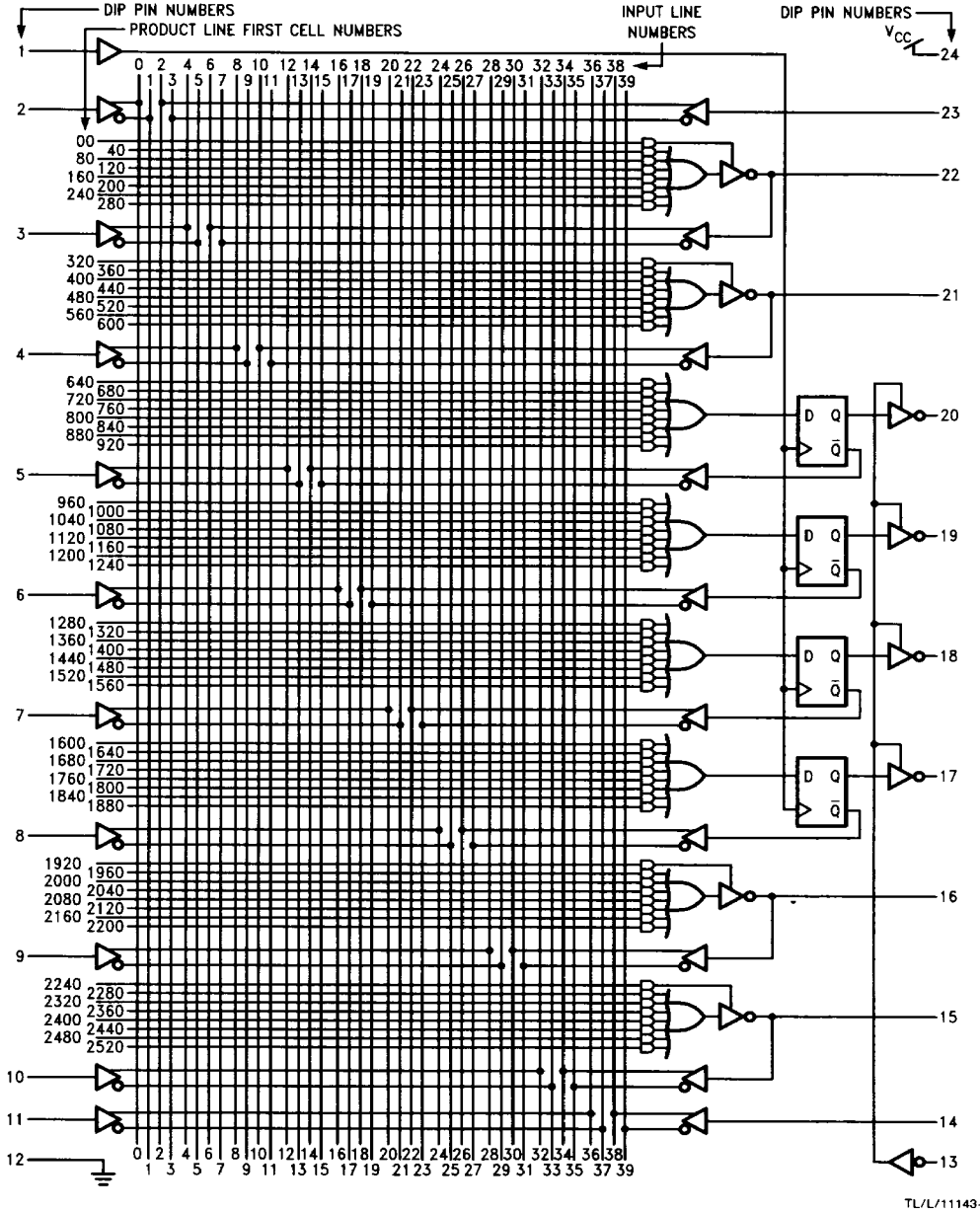
Logic Diagram—PAL20L8



TL/L/11143–22

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

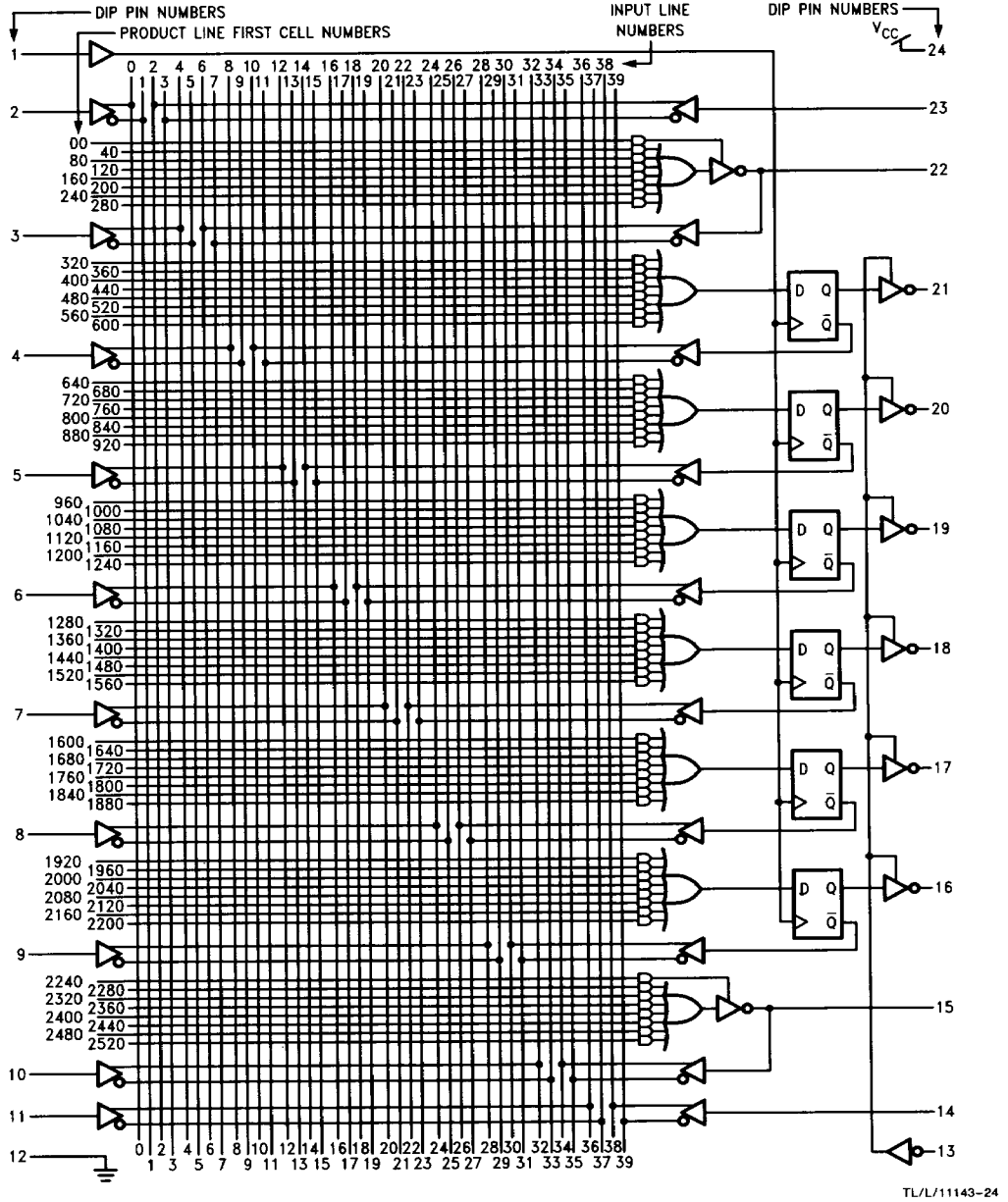
Logic Diagram—PAL20R4



TL/L/11143–23

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

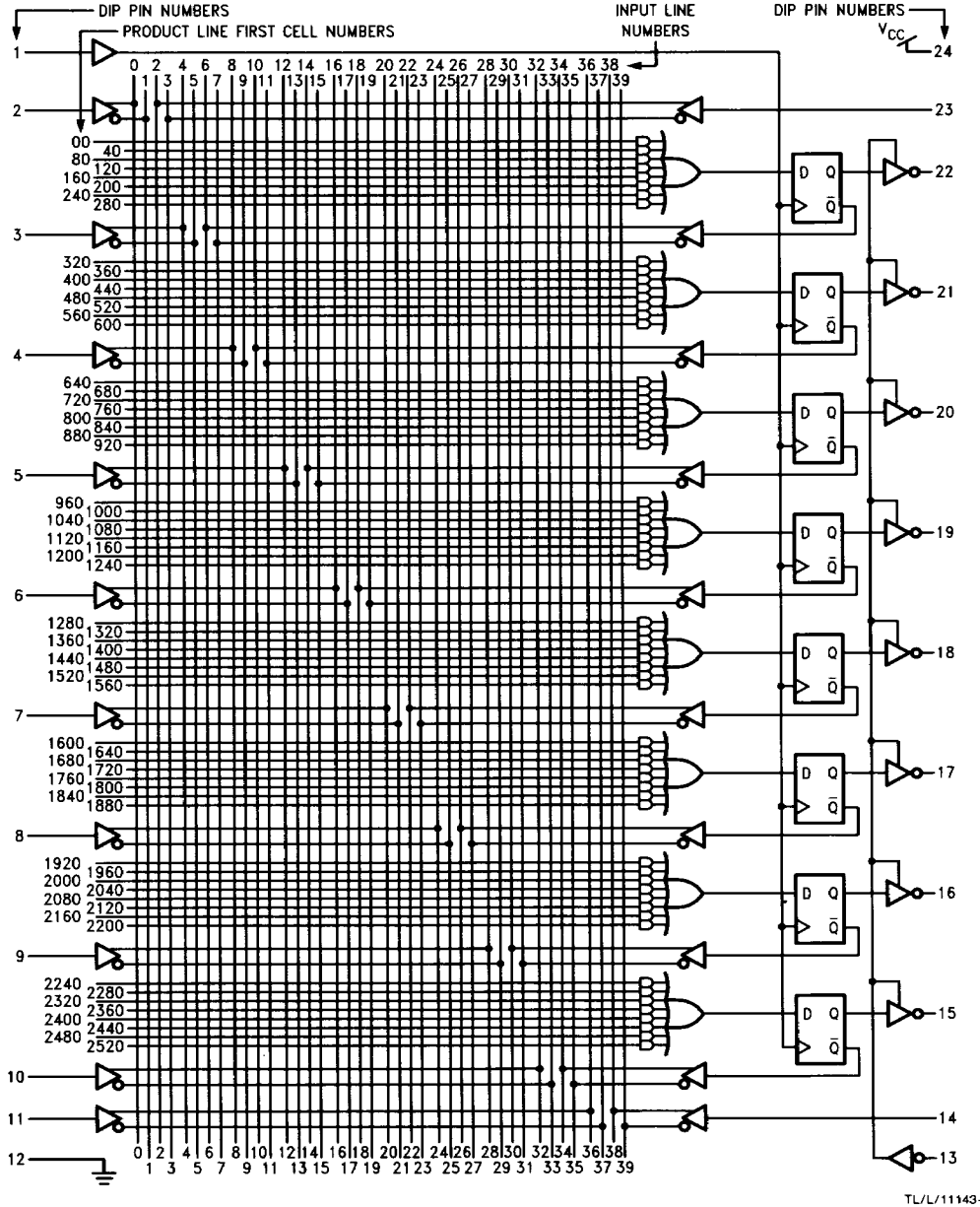
Logic Diagram—PAL20R6



TL/L/11143–24

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

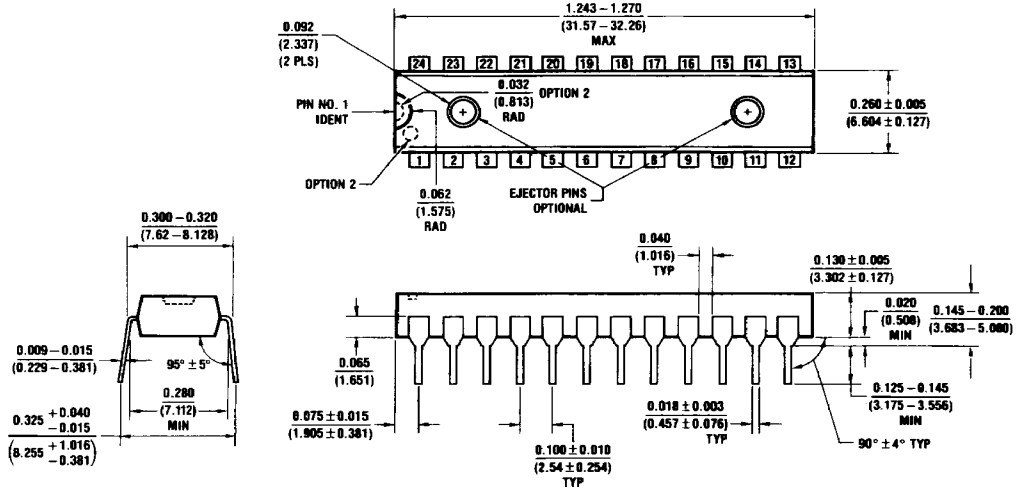
Logic Diagram—PAL20R8



TL/L/11143–25

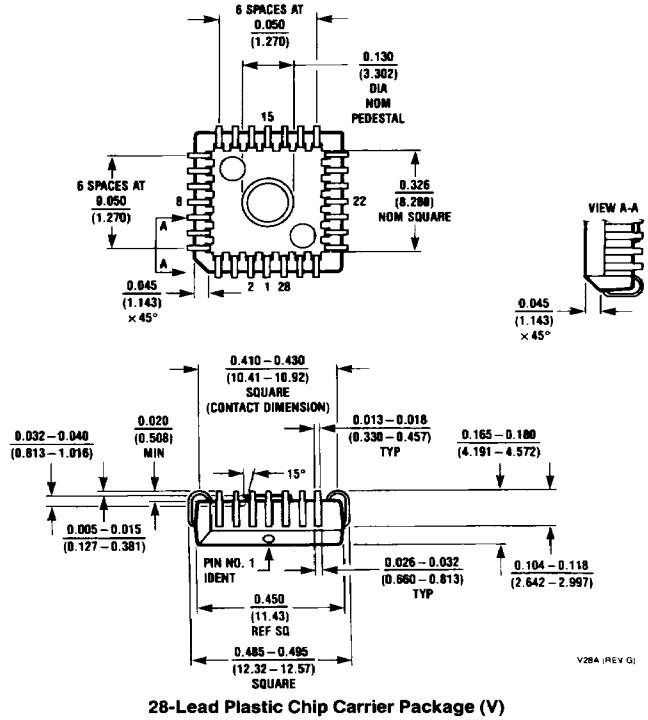
JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

Physical Dimensions inches (millimeters)



24-Pin Narrow Plastic Dual-In-Line Package (N)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



28-Lead Plastic Chip Carrier Package (V)
NS Package Number V28A

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