Final | COM'L : -20/std | MIL: std

PAL20RA10/-20

24-pin Asynchronous TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 20 ns maximum propagation delay and 30 MHz f_{MAX}
- Individually programmable asynchronous clock, preset, reset, and enable
- Registered or combinatorial outputs
- Programmable polarity
- Programmable replacement for high-speed TTL logic
- TTL-level register preload for testability
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The PAL20RA10 offers asynchronous clocking for each of the ten flip-flops in the device. The ten macrocells feature programmable clock, preset, reset, and enable, and all can operate asynchronously to other macrocells in the same device. The PAL20RA10 also has flip-flop bypass, allowing any combination of registered and combinatorial outputs.

The PAL20RA10 utilizes Advanced Micro Devices' advanced oxide- and junction-isolated bipolar processes and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL20RA10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

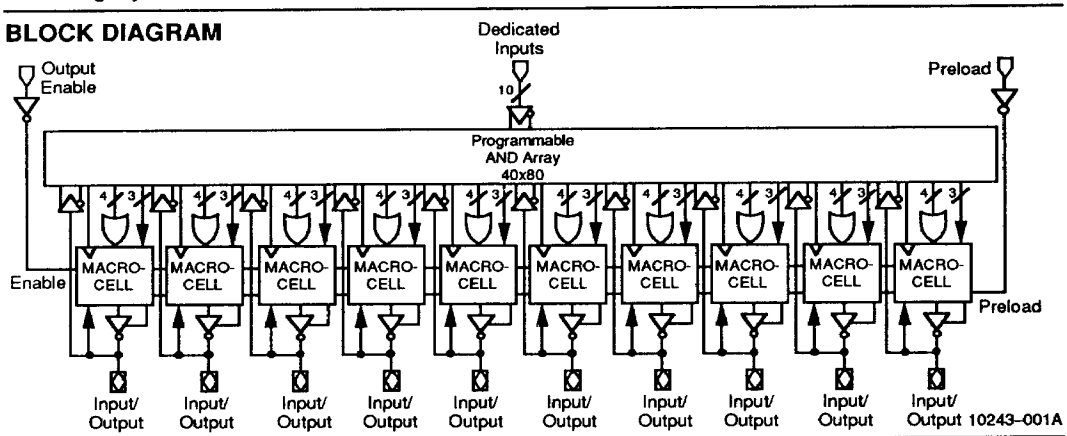
The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers.

2

BLOCK DIAGRAM



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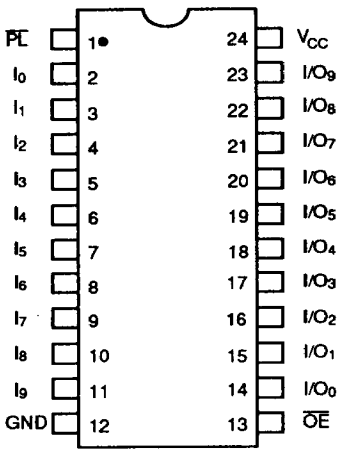
CONNECTION DIAGRAMS
Top Views

SKINNYDIP/FLATPACK



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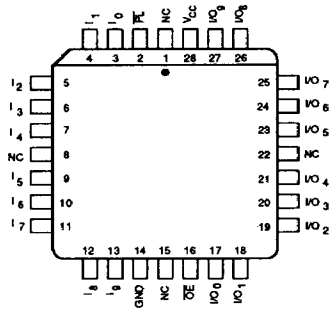
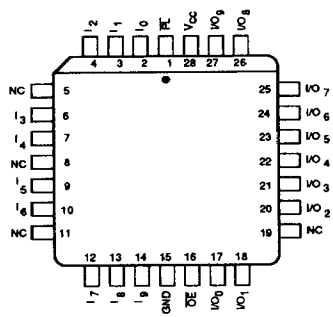
PLCC (-20 only)



10243–003A

PLCC (std only)



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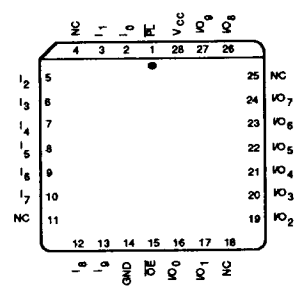
LCC



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Note:
Pin 1 is marked for orientation

PIN DESIGNATIONS

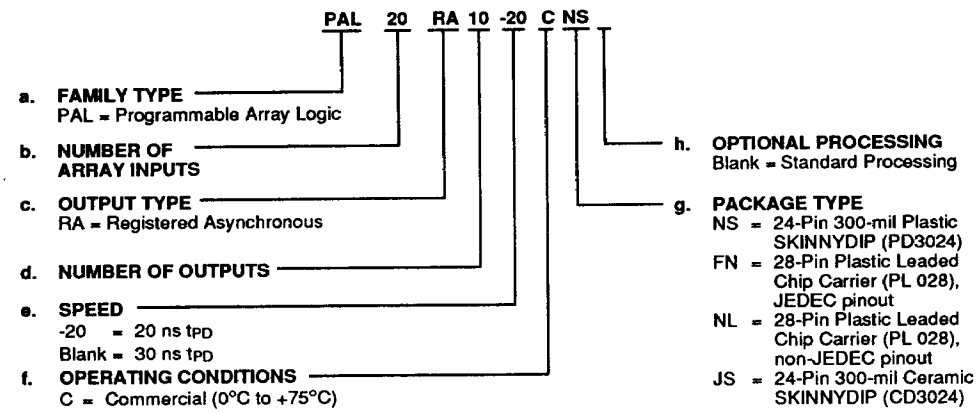
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
$\overline{OE}$	Output Enable
$\overline{PL}$	Preload
V_{CC}	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Speed**
f. **Operating Conditions**
g. **Package Type**
h. **Optional Processing**



Valid Combinations	
PAL20RA10-20	CNS, CFN, CJS
PAL20RA10	CNS, CNL, CJS

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

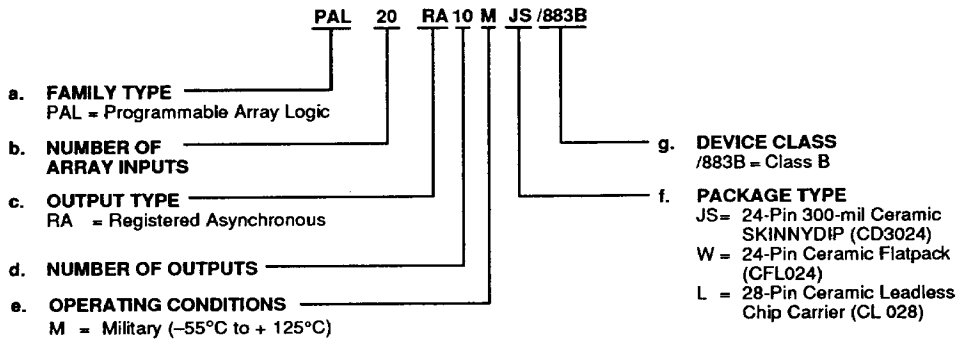
Note: Marked with MMI logo.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Operating Conditions**
f. **Package Type**
g. **Device Class**



Valid Combinations	
PAL20RA10	MJS/883B, MW/883B, ML/883B

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

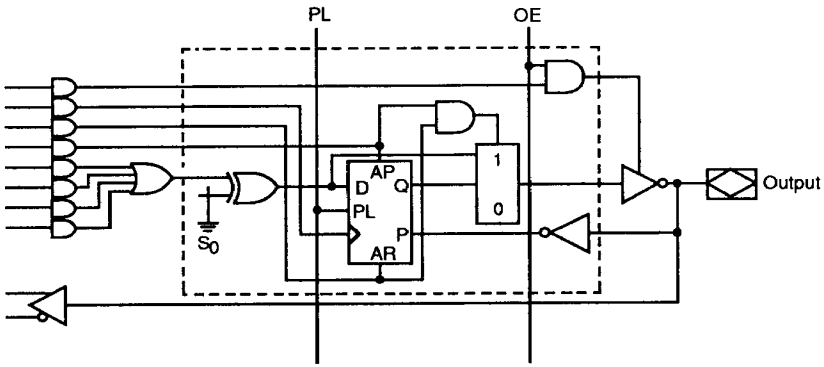
Note: Marked with MMI logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.



10232-004A

Figure 1. PAL20RA10 Macrocell

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FUNCTIONAL DESCRIPTION

The PAL20RA10 has ten dedicated input lines and ten programmable I/O macrocells. The Registered Asynchronous (RA) macrocell is shown in Figure 1. Pin 1 serves as global register preload and pin 13 serves as global output enable. Programmable output polarity is available to provide user-programmable output polarity for each individual macrocell.

The programmable functions in the PAL20RA10 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

Programmable Preset and Reset

In each macrocell, two product lines are dedicated to asynchronous preset and asynchronous reset. If the preset product line is HIGH, the Q output of the register becomes a logic 1. If the reset product line is HIGH, the Q output of the register becomes a logic 0. The operation of the programmable preset and reset overrides the clock.

Combinatorial/Registered Outputs

If both the preset and reset product lines are HIGH, the flip-flop is bypassed and the output becomes combinatorial. Otherwise, the output is from the register. Each output can be configured to be combinatorial or registered.

Programmable Clock

The clock input to each flop-flop comes from the programmable array, allowing any flip-flop to be clocked independently if desired.

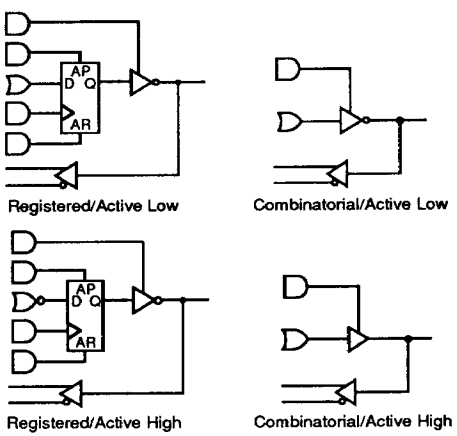

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Figure 2. Macrocell Configurations

Three-State Outputs

The devices provide a product term dedicated to local output control. There is also a global output control pin. The output is enabled if both the global output control pin is LOW and the local output control product term is HIGH. If the global output control pin is HIGH, all outputs will be disabled. If the local output control product term is LOW, then that output will be disabled.

Security Fuse

A security fuse is also provided to prevent unauthorized copying of PAL device patterns. Once the fuse is programmed, the circuitry enabling verification is permanently disabled, and the array will read as if every fuse is programmed. With verification not operating, it is impossible to simply copy the PAL device pattern on a PAL device programmer.

Programmable Polarity

The outputs can be programmed either active-LOW or active-HIGH. This is represented by the Exclusive-OR gate shown in the PAL20RA10 logic diagram. When the output polarity fuse is programmed, the lower input to the Exclusive-OR gate is HIGH, so the output is active-HIGH. Similarly when the output polarity fuse is intact, the output is active-LOW. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.

Programming

The PAL20RA10 can be programmed on standard logic programmers. Programmers approved by Advanced Micro Devices are listed in the Programmer Reference Guide.

Register Preload

The register on the PAL20RA10/20 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transistions from illegal states can be verified by loading illegal states and observing proper recovery. Register preload is controlled by a TTL-level signal, making it a convenient board-level initialization function.

Pinouts

All PAL20RA10 devices have the same SKINNYDIP pinouts independent of performance and operating conditions. Because the 24-pin SKINNYDIP requires four no-connects when mapped into the 28-pin PLCC/LCC packages, the PLCC/LCC pinouts can vary.

Two different PLCC pinouts are offered. The PAL20RA10-20 and all future devices will follow the JEDEC electronics committee's standard pinout ("JEDEC pinout") with no-connects on pins 1, 8, 15, and 22. The older, standard PAL20RA10 devices retain their original pinouts with no-connects on pins 5, 8, 11, and 19.

PAL20RA10 devices with the MMI marking indicate the PLCC pinout by the package designator: FN indicates JEDEC, and NL indicates non-JEDEC.

A different LCC pinout is offered for the military PAL20RA10. Older devices retain their original pinouts, with no-connects on pins 4, 11, 18, and 25.

Series	Com'l PLCC No-connects	Mil LCC No-connects
-20	1, 8, 15, 22 (JEDEC)	N/A
std.	5, 8, 11, 19	4, 11, 18, 25

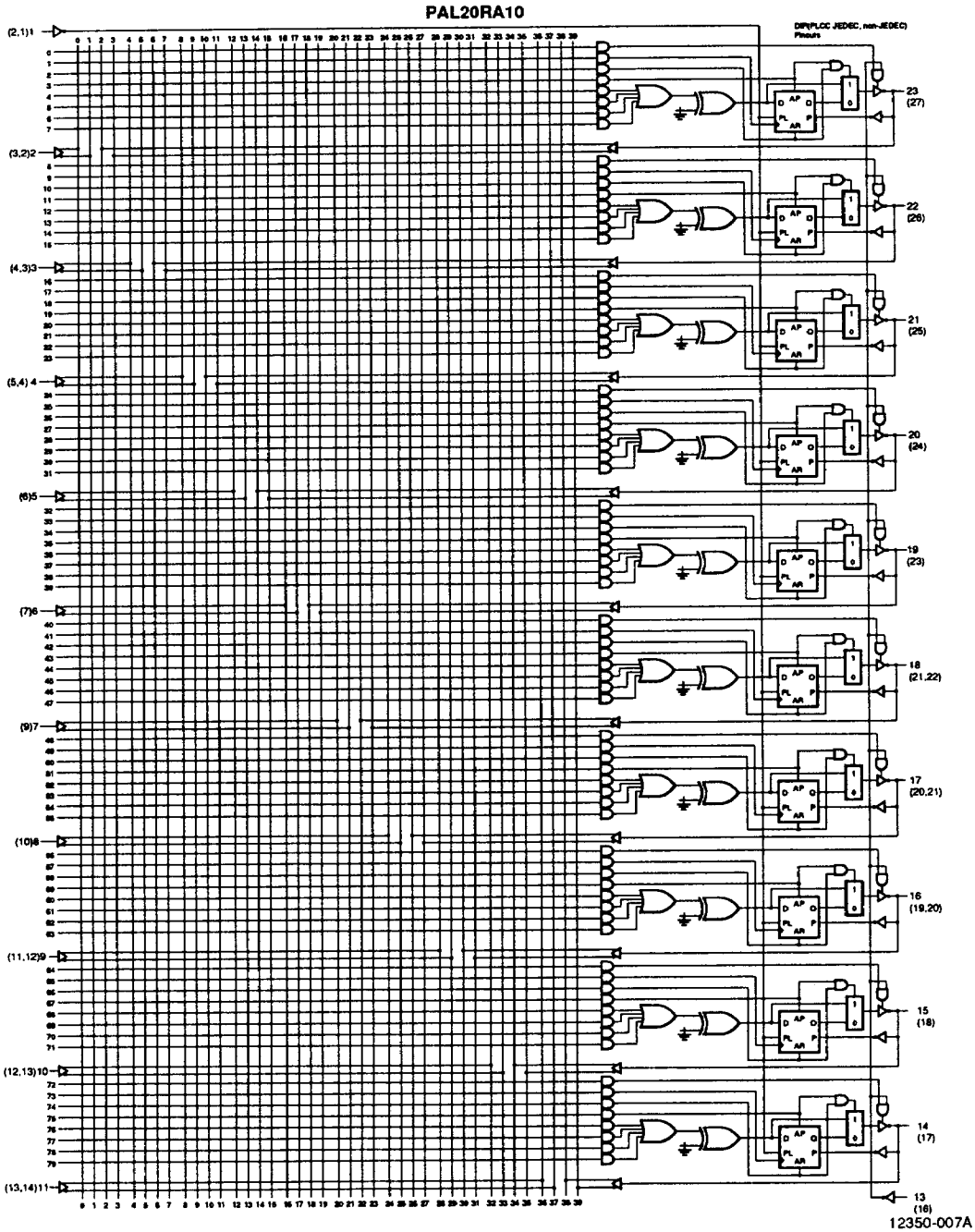
Quality and Testability

The PAL20RA10-20 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PAL20RA10-20 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven TiW fuses. The standard PAL20RA10 is fabricated with AMD's junction-isolated process, utilizing TiW fuses.

LOGIC DIAGRAM
DIP (PLCC JEDEC, non-JEDEC) Pinouts, see Connection Diagrams for LCC Pinout



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
DC Current into Outputs (-20 only)	16 mA
Static Discharge Voltage (-20 only)	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		200	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1) (-20 only)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Inputs	V_{IN} = 2.0 V	V_{CC} = 5.0 V	5	pF
		CLK, $\overline{OE}$		T_A = +25°C	9	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	5	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20		Std		Unit
				Min. (Note 3)	Max.	Min. (Note 3)	Max.	
t_{PD}	Input or Feedback to Combinatorial Output	Active Low			20		30	ns
		Active High			20		35	ns
t_S	Setup Time from Input or Feedback to Clock			13		20		ns
t_H	Hold Time	Active Low		5		10		ns
		Active High		5		0		ns
t_{CO}	Clock to Output or Feedback			5	20	10	30	ns
t_{AP}	Asynchronous Preset to Registered Output				20		35	ns
t_{APW}	Asynchronous Preset Width			20		20		ns
t_{AR}	Asynchronous Reset to Registered Output				25		40	ns
t_{ARW}	Asynchronous Reset Width			20		20		ns
t_{WL}	Clock Width	LOW		14		20		ns
t_{WH}		HIGH		14		20		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	30		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	36		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				20		30	ns
t_{ER}	Input to Output Disable Using Product Term Control				20		30	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		200	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

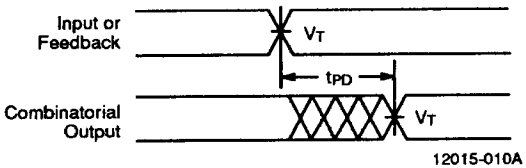
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description			Standard Min.	Standard Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output	Active Low			35	ns
		Active High			40	ns
t_S	Setup Time from Input or Feedback to Clock			25		ns
t_H	Hold Time	Active Low		10		ns
		Active High		0		ns
t_{CO}	Clock to Output or Feedback				35	ns
t_{AP}	Asynchronous Preset to Registered Output				40	ns
t_{APW}	Asynchronous Preset Width			25		ns
t_{AR}	Asynchronous Reset to Registered Output				55	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{WL}	Clock Width	LOW		25		ns
t_{WH}		HIGH		25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$	16.7		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)				25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)				25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				35	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				35	ns

Notes:

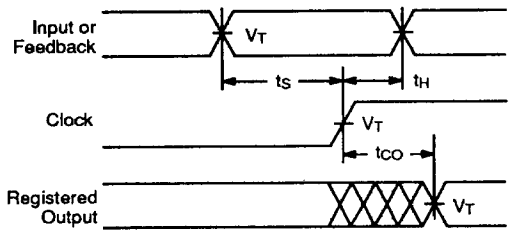
1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

SWITCHING WAVEFORMS



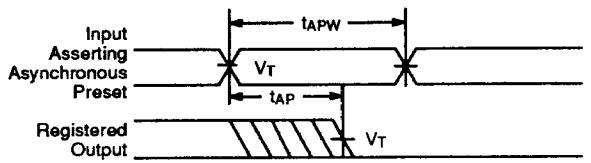
12015-010A

Combinatorial Output



12015-012A

Registered Output



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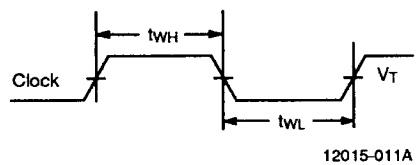
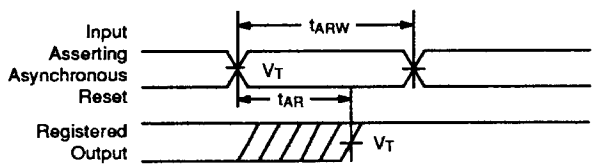
Asynchronous Preset



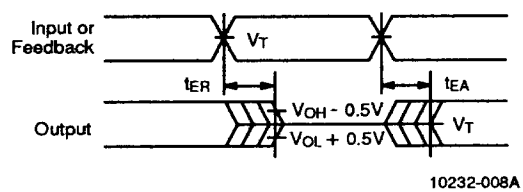
12015-011A

Clock Width



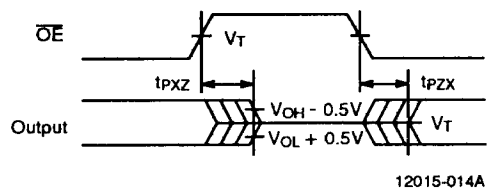
10232-009A

Asynchronous Reset



10232-008A

Input to Output Disable/Enable



12015-014A

$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

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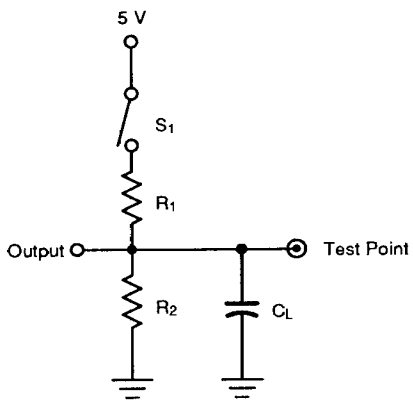
SWITCHING TEST CIRCUIT

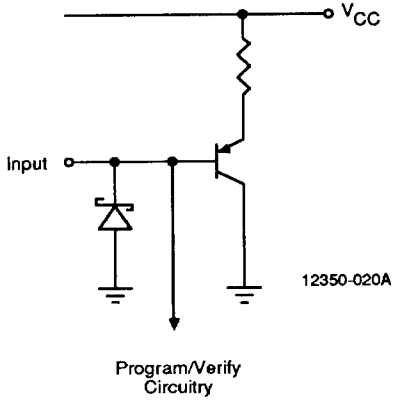


12350-019A

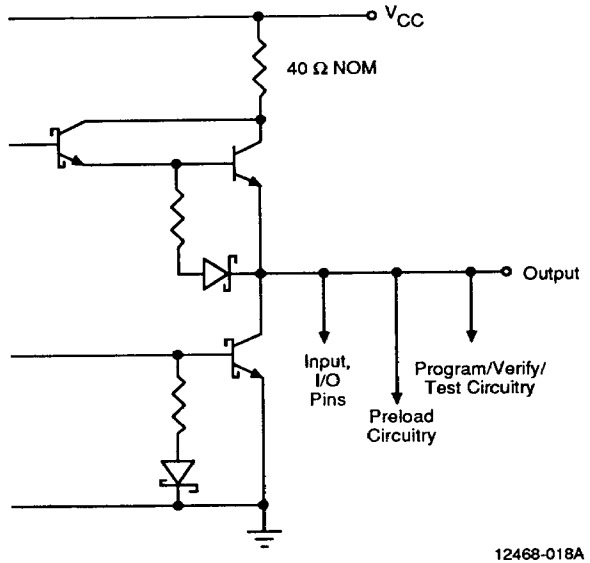
Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	560 Ω	1.1K Ω	560 Ω	1.1K Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



Typical Output

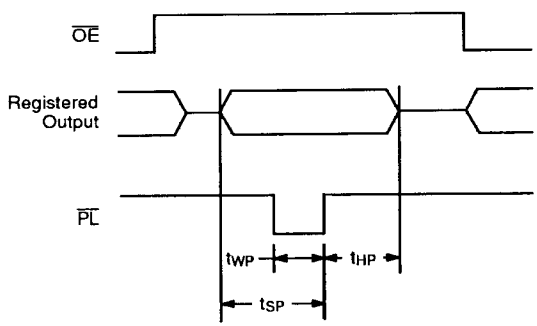


OUTPUT REGISTER PRELOAD

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Set $\overline{OE}$ to V_{IHP} to disable output registers.
2. Apply either V_{IHP} or V_{ILP} to all registered outputs. Leave combinatorial outputs floating.
3. Pulse $\overline{PL}$ from V_{IHP} to V_{ILP} to V_{IHP}.
4. Remove V_{ILP}/V_{IHP} from all registered output pins.
5. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
6. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description		Min.	Rec.	Max.	Unit
V_{ILP}	Low-level input voltage		0	0	0.5	V
V_{IHP}	High-level input voltage		2.4	5.0	5.5	V
t_{SP}	Preload setup time	-20 COM'L	15			ns
		std COM'L	25			
		std MIL	30			
t_{WP}	Preload pulse width	-20 COM'L	20			ns
		std COM'L	35			
		std MIL	45			
t_{HP}	Preload hold time	-20 COM'L	15			ns
		std COM'L	25			
		std MIL	30			



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Output Register Preload Waveform