High Speed Programmable Array Logic

PAL22RX8A

T-46-13-47

Features/Benefits

- Programmable flip-flops allow J-K, S-R, T or D-types for the most efficient use of product terms
- 8 input/output macrocells for flexibility
- Programmable registered or combinatorial outputs
- Programmable output polarity
- Global register asynchronous preset/asynchronous reset
- Automatic register reset on power up
- Preloadable output registers for testability
- High speed at 25 ns t_{PD}, 28.5 MHz f_{MAX}
- Space-saving 24-pin 300-mil SKINNYDIP® package or 28-pin chip carrier

General Description

The PAL22RX8A is a high-density Programmable Array Logic (PAL®) device which implements a sum-of-products transfer function via a user-programmable AND logic array and a fixed OR logic array. Featured are eight highly flexible input/output macrocells which are user-configurable for combinatorial or registered operation. Each flip-flop can be programmed to be either a J-K, S-R, T, or D-type for optimal design of state machines and other synchronous logic. The PAL22RX8A is a functional superset of, and pin-compatible with, the PAL24A Series, but can implement many new functions due to its added features. Supplied in space-saving 300-mil-wide dual in-line packages or 28-pin chip carriers, the PAL22RX8A offers a powerful, space-saving alternative to SSI/MSI logic devices, while providing the advantage of instant prototyping. Security fuses defeat readout after programming and make proprietary designs difficult to copy.

The PAL22RX8A is fabricated using Monolithic Memories' advanced bipolar process for high speed and low power. TiW fuse links provide high reliability and programming yields. Special on-chip test circuits allow full AC, DC, and functional testing before programming. Preloadable output registers facilitate functional testing.

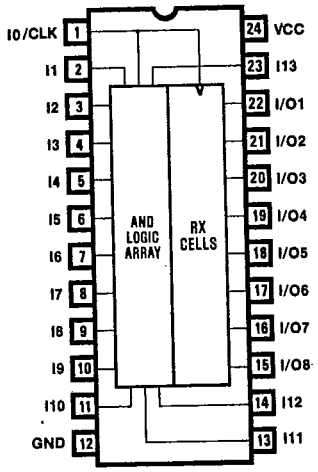
The PAL22RX8A can be programmed on standard PAL device programmers, fitted with appropriate programming modules and configuration software. Design development is supported by Monolithic Memories' PALASM® 2 software as well as by other programmable logic CAD tools available from third party vendors.

Ordering Information

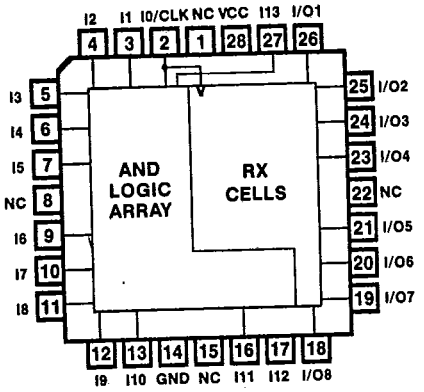
PAL22RX8A C NS STD

- PROGRAMMABLE ARRAY LOGIC
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE: RX = Registered XOR
- NUMBER OF OUTPUTS
- SPEED: A = High Speed
- PROCESSING: STD = Standard, XXXX = Other
- PACKAGE: NS = Plastic SKINNYDIP, JS = Ceramic SKINNYDIP, FN = Plastic Leaded Chip Carrier
- TEMPERATURE RANGE: C = 0°C to 75°C

Pin Configurations



SKINNYDIP Package



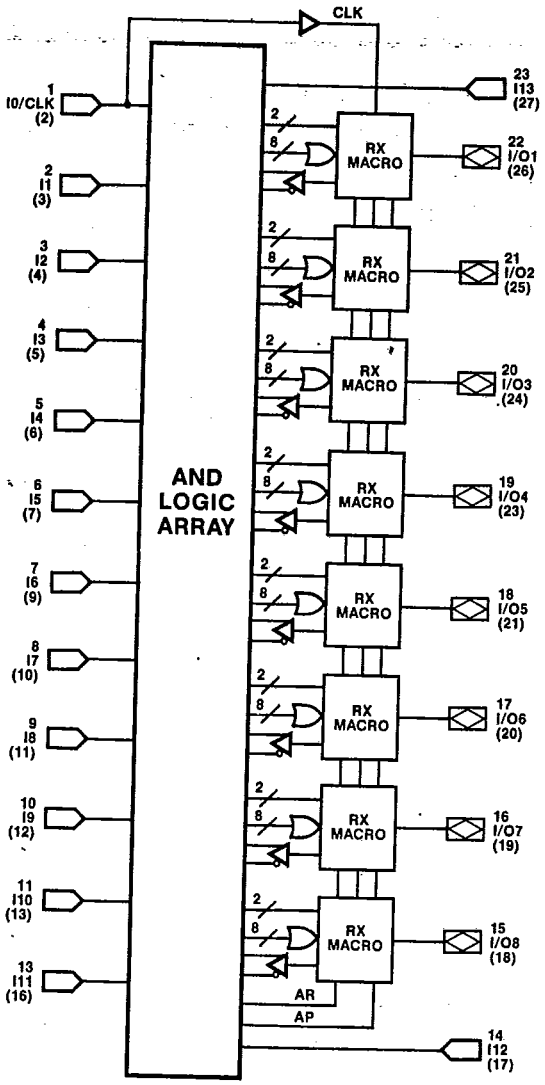
Plastic Leaded Chip Carrier

Package Drawings

(refer to PAL Device Package Outlines, page 3-179)

10295A
JANUARY 1988

Block Diagram



Note:
PLCC pin numbers are indicated in parentheses.
PLCC pins 1, 8, 15 and 22 are not connected.

Description of Architecture

The PAL22RX8A has fourteen dedicated inputs and eight programmable I/O macrocells. Pin 1 serves either as an array input or as a clock for all flip-flops. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. The fuse matrix implements a programmable AND logic array, which drives a fixed OR logic array.

The high level of flexibility built into each macrocell, shown in Figure 1, allows the PAL22RX8A to implement several different architecture options. Each macrocell can be individually programmed to implement a variety of combinatorial or registered logic functions.

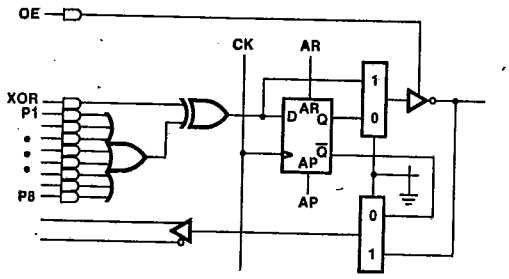


Figure 1. PAL22RX8A Macrocell

Programmable Flip-Flops

Each output macrocell contains a unique programmable flip-flop consisting of a basic D-type flip-flop driven by an XOR gate. This allows the user to choose the optimal flip-flop for the design, since either J-K, S-R, or T-type flip-flops can be synthesized from such a structure without wasting product terms.

As indicated in the macrocell logic diagram, one input of the XOR gate is connected to a single product term, while the second input is connected to the output of the OR logic array. The XOR gate output feeds the input of the D flip-flop. The way in which the XOR gate is used to synthesize the different flip-flop types is described in detail below.

D Flip-Flop. The D flip-flop option is implemented directly. In this configuration, the XOR gate on the input of the flip-flop can be used to program the logic polarity of the transfer function.

J-K Flip-Flop. The J-K flip-flop option can be easily synthesized with a more sophisticated manipulation of the XOR gate inputs and the D flip-flop output.

The transfer function of a J-K flip-flop can be mapped in the Karnaugh Map of Figure 2, where Q+ represents the next state of the flip-flop:

J K \ Q	0	1	Q+
0 0	0	[1]	(HOLD)
0 1	0	0	(RESET)
1 1	[1]	0	(TOGGLE)
1 0	[1]	[1]	(SET)

Figure 2. J-K Flip-Flop Transfer Function

Dropping the (+) for simplicity, the equivalent Boolean expression for Q+ is:

$$Q := \overline{K}*Q + J*\overline{Q}$$

In general, J and K can be sum-of-product expressions which are provided in the PAL architecture only in active-high form. Thus, a direct implementation of $\overline{K}$ expressions must invoke a DeMorgan transformation, which can use excessive product terms. This can be avoided by rewriting the equation for Q without inversions on the J or K inputs.

The XOR gate can be used to construct a logically equivalent expression without any inversions on the J or K inputs. The rewritten Boolean expression is:

$$Q := Q :+: (J*\overline{Q} + K*Q)$$

To check that these expressions are logically equivalent, change the XOR to its equivalent sum of products form (remember $A :+: B = A*\overline{B} + \overline{A}*B$) and reduce (using DeMorgan's theorem):

$$\begin{aligned} Q &:= Q*\overline{(J*\overline{Q} + K*Q)} + \overline{Q}*(J*\overline{Q} + \overline{K}*Q) \\ Q &:= Q*\overline{(J + Q)}*\overline{(\overline{K} + \overline{Q})} + \overline{Q}*J*\overline{Q} + \overline{Q}*K*Q \\ Q &:= Q*(\overline{J}*\overline{K} + J*\overline{Q} + Q*\overline{K} + Q*\overline{Q}) + J*\overline{Q} \\ Q &:= \overline{J}*\overline{K}*Q + \overline{K}*Q + J*\overline{Q} \end{aligned}$$

which simplifies to $Q := \overline{K}*Q + J*\overline{Q}$.

Since J and K are, in general, sums of products, J and K in either expression can be substituted with (J1 + J2 + ... + Jm) and (K1 + K2 + ... + K8-m), where 8 is the total number of product terms associated with a given output macrocell. Thus, the total 8 product term resource is shared between the J and K control inputs (Figure 3). Note that all J terms will contain $\overline{Q}$ and all K terms will contain Q.

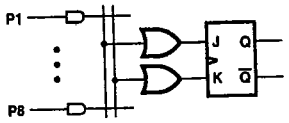


Figure 3. J-K Flip-Flop Logic Equivalent; J and K Can Also be Active-Low

The above discussions have assumed that it was most convenient to "group ones" in the Karnaugh Map. Sometimes it takes fewer product terms to "group zeros", i.e., implement the inversion of the desired function. The equations shown in Table 1 are equivalent and can be interchanged to optimize product term utilization. This can be readily proved through logic reductions similar to that above.

J and K active high	$Q := Q :+: (J*\overline{Q} + K*Q)$
J active high, K active low	$Q := J*\overline{Q} + \overline{K}*Q$
J active low, K active high	$\overline{Q} := \overline{J}*\overline{Q} + K*Q$
J and K active low	$Q := \overline{Q} :+: (\overline{J}*\overline{Q} + \overline{K}*Q)$

Note: J = sum of products J1 + J2 + ... + Jm
K = sum of products K1 + K2 + ... + K8-m
8 = total number of available product terms for a given macrocell

Table 1. J-K Flip-Flop Transfer Functions

S-R Flip-Flop. The S-R flip-flop has a truth table identical to that of the J-K flip-flop, with the exception that the J=K=1 (toggle) condition is not allowed. The S-R flip-flop implementation is identical to that of the J-K flip-flop, with J-K replaced by S-R, and the S=R=1 condition avoided.

T Flip-Flop. A T (toggle) flip-flop either holds its state or toggles, depending on the logic state of the T input. The T flip-flop is a subset of the J-K flip-flop and can be considered equivalent to a J-K type with J=K. The general transfer function and its active-low T equivalent are both given in Table 2.

$Q := Q :+: T$
$Q := \overline{Q} :+: \overline{T}$

Note: T = sum of products T1 + T2 + T3 + ... + T8.

Table 2. T Flip-Flop Transfer Functions

Summary

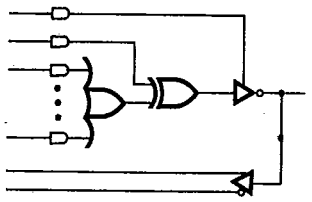
The PAL22RX8A can synthesize J-K, S-R, T, and D flip-flops, whichever is most convenient for the application, without sacrificing product terms. Additionally, the synthesized equations can use the active-high or active-low forms of the inputs, allowing the designer to minimize product term requirements.

5

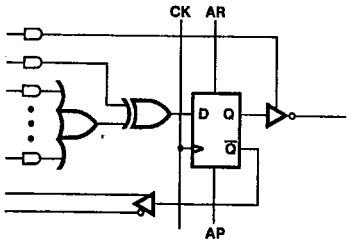
Flip-Flop Bypass

Any output in the PAL22RX8A can be configured as combinatorial by bypassing the output flip-flop. This is done by setting the output multiplexer to the appropriate state. The multiplexer is controlled by a single architecture fuse which, when intact, selects a registered output with register feedback and, when opened, selects a combinatorial output with feedback from the output pin.

Combinatorial I/O



Registered Output



Programmable I/O

Each macrocell has a three-state output buffer with programmable three-state control. Control is implemented by a single product term, allowing specification of enable/disable functions controlled by any device input or output. Each macrocell can be configured as a dedicated input by selecting the combinatorial output configuration and disabling the buffer drive capability.

Programmable Polarity

The polarity of each macrocell output can be set active high or active low.

Combinatorial Outputs. The XOR gate provides polarity control for combinatorial outputs, with the single product term to the XOR gate controlling the invert/not invert function. With all fuses intact, there is no inversion through the XOR gate, creating an active high output.

Registered Outputs. For D-type registered outputs, polarity can be set by the XOR gate, as is the case with combinatorial outputs. Using this method to set polarity, preset and reset will not be affected.

Polarity options for J-K, S-R, and T flip-flops have been discussed in the section on programmable flip-flops.

Programmable Preset and Reset

The eight macrocell flip-flops share common programmable preset and reset control for easy system initialization. The Q outputs of the register will go to the logic low state independent of the clock when the asynchronous reset (AR) product term is asserted. The register will be forced to the logic high state independent of the clock when the asynchronous preset (AP) product term is asserted.

Power-Up Reset

All flip-flops power up to a logic low for predictable system initialization. The power-up state of the flip-flop is not affected by the output polarity option chosen. Due to the output inverter, the outputs will power up to a logic high. See waveform at end of TTL/CMOS PAL Devices section.

Register Preload

The register on the PAL22RX8A can be preloaded by use of supervoltages to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by preloading illegal states and observing proper recovery.

Security Fuses

After programming and verification, a PAL22RX8A design can be secured by programming the security fuses. Once programmed, these fuses defeat readback of the internal fuse pattern by a device programmer, making proprietary designs very difficult to copy.

Quality and Testability

The PAL22RX8A offers a very high level of built-in quality. Special on-chip test circuitry provides a means of verifying performance of all AC and DC parameters prior to programming. In addition, these built-in test paths verify complete functionality of each device to provide the highest post-programming functional yields in the industry.

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7 V	−0.5 V to 12 V
Input voltage	−1.5 V to 5.5 V	−1.0 V to 12 V
Off-state output voltage	5.5 V	12 V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1] MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	10	7		ns
		High	10	7		
t_{su}	Setup time from input or feedback to clock		20	16		ns
t_h	Hold time		0	−10		ns
t_{aw}	Asynchronous preset/reset width		15	10		ns
t_{ar}	Asynchronous preset/reset recovery time		30	25		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.1	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.35	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2 mA	2.4	3.4		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}[3]			V_O = 2.4 V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			180	210	mA
C_{IN}	Input capacitance	V_{IN} = 2.0 V at f = 1 MHz	DIP pins 1, 13		15		pF
			All other inputs		12		
C_{OUT}	Output capacitance	V_{OUT} = 2.0 V at f = 1 MHz			12		

Notes. 1. The PAL22RX8A is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

5

Switching Characteristics Over Operating Conditions

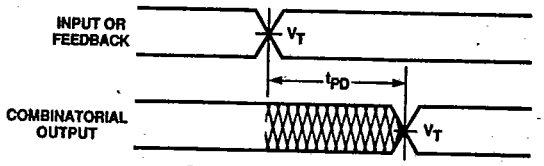
SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output		$R_1 = 200\ \Omega$ $R_2 = 390\ \Omega$		20	25	ns
t_{CLK}	Clock to output or feedback				12	15	ns
t_{EA}	Input to output enable				20	25	ns
t_{ER}	Input to output disable				18	25	ns
t_{AP}	Asynchronous preset/reset to output				25	35	ns
f_{MAX}	Maximum frequency	External feedback		28.5	40		MHz
		No feedback		50	55		

Switching Test Load
(refer to page 5-164)

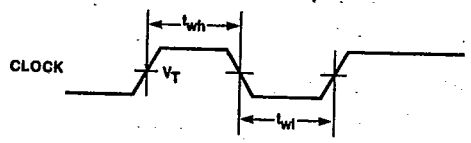
Power-Up Reset Waveform
(refer to page 5-164)

Schematic of Inputs and Outputs
(refer to page 5-164)

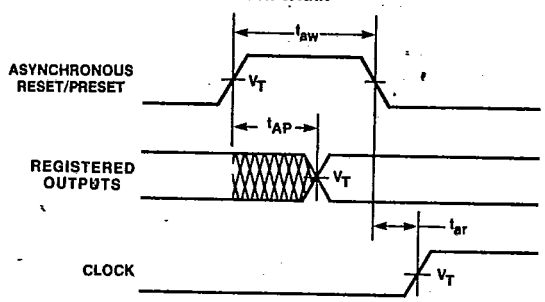
Switching Waveforms



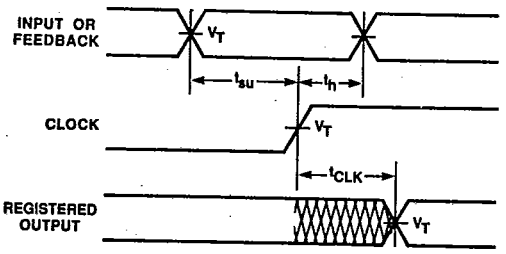
Combinatorial Output



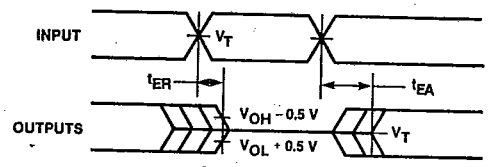
Clock Width



Asynchronous Reset/Preset



Registered Output



Input to Output Disable/Enable

Notes:
1. VT = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2-5 ns typical

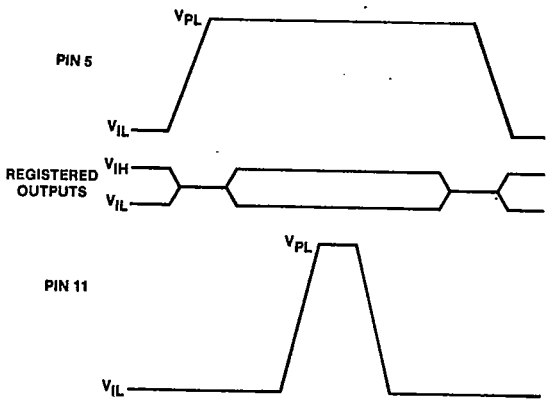
Output Register Preload

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure is:

1. Raise V_{CC} to 5.0 V.
2. Set pin 1 (CLK) to V_{IL}.
3. Disable output registers by setting pin 5 to V_{PL} (18.0 V ± 0.5 V).
4. Apply the desired level (V_{IL}/V_{IH}) to all registered output pins. Leave combinatorial outputs floating.
5. Pulse pin 11 to V_{PL}, then back to 0 V.
6. Remove V_{IL}/V_{IH} from all output registers.
7. Lower pin 5 to V_{IL}.
8. Enable output registers per programmed pattern.
9. Verify for V_{OL}/V_{OH} at all registered output pins.

Programmers/Development Systems

(refer to Programmer Reference Guide, page 3-81)



5

Key to Timing Diagrams

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Logic Diagram

DIP (PLCC) Pinouts

PAL22RX8A