CYPRESS SEMICONDUCTOR

PAL22V10CF
PAL22VP10CF

Universal PAL® Device

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 7.5 ns**
  - **— t_{SU} = 3 ns**
  - **— f_{MAX} = 100 MHz**
  - **— Drives 50-pF load (C_L)**
- **"No Connect" PLCC pinout**
- **Up to 22 inputs and 10 outputs for more logic power**
- **Variable product terms**
  - **— 8 to 16 per output**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— 2 new feedback paths (PAL22VP10CF)**
- **Synchronous PRESET, asynchronous RESET, and PRELOAD capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
- **Security Fuse**

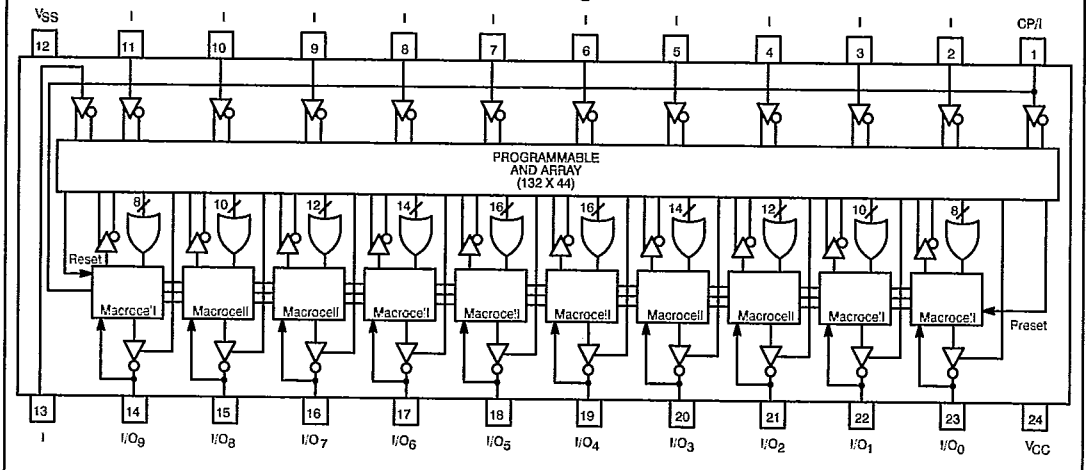
Functional Description

The Cypress PAL22V10CF and PAL22VP10CF are second-generation programmable array logic devices. Using BiCMOS process and Ti-W fuses, the PAL22V10CF and PAL22VP10CF use the familiar sum-of-products (AND-OR) logic structure and a new concept, the programmable macrocell.

Both the PAL22V10CF and PAL22VP10CF provide 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O allows this selection.

The PAL22V10CF and PAL22VP10CF feature variable product-term architecture, where 8 to 16 product terms are allocated to each output. This structure permits more applications to be implemented with these devices than with other PAL devices that have fixed number of product terms for each output.

Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration



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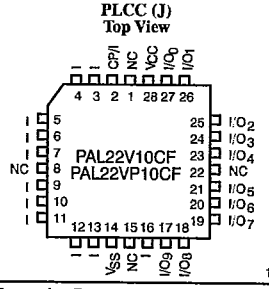
Pin Configuration

PLCC (J)
Top View



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QuickProII is a trademark of Cypress Semiconductor Corporation.

Functional Description (continued)

Additional features include common synchronous preset and asynchronous reset product terms. They eliminate the need to use standard product terms for initialization functions

Both the PAL22V10CF and PAL22VP10CF automatically reset on power-up. In addition, the preload capability allows the output registers to be set to any desired state during testing.

A security fuse is provided on each of these two devices to prevent copying of the device fuse pattern.

With the programmable macrocells and variable product term architecture, the PAL22V10CF and PAL22VP10CF can implement logic functions in the 700 to 800 gate array complexity, with the inherent advantages of programmable logic.

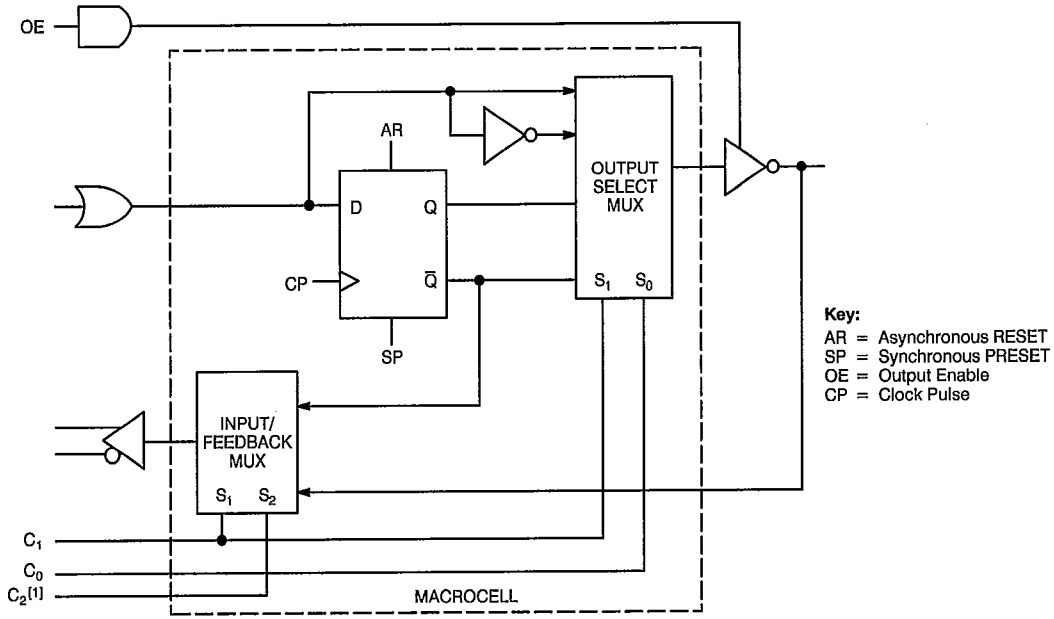
Programmable Macrocell

The PAL22V10CF and PAL22VP10CF each has 10 programmable output macrocells (see Macrocell figure). On the PAL22V10CF two fuses (C_1 and C_0) can be programmed to configure output in one of four ways. Accordingly, each output can be registered or combinatorial with an active HIGH or active LOW polarity. The feedback to the array is also from this output (see *Figure 1*). An additional fuse (C_2) in the PAL22VP10CF provides for two feedback paths (see *Figure 2*).

Programming

The PAL22V10CF and PAL22VP10CF can be programmed using the QuickPro II™ programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG and other programmers. Please contact your local Cypress representative for further information.

Macrocell



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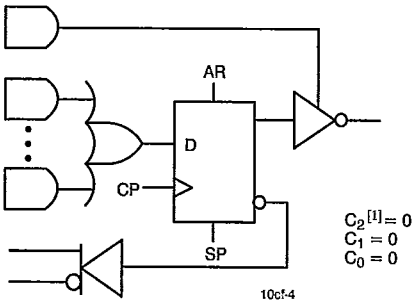
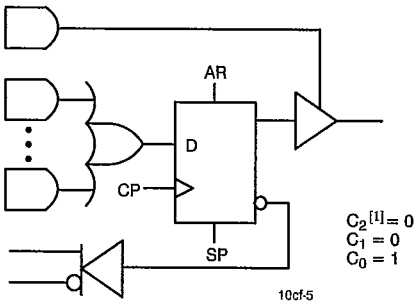
Output Macrocell Configuration

C_2[1]	C_1	C_0	Output Type	Polarity	Feedback
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
X	1	0	Combinatorial	Active LOW	I/O
X	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O[1]
1	0	1	Registered	Active HIGH	I/O[1]

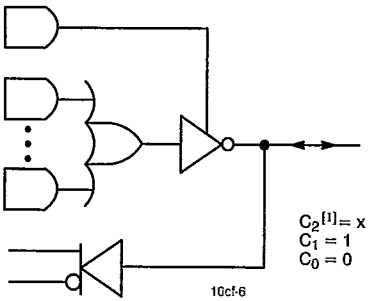
Notes:
1. PAL22VP10CF only.



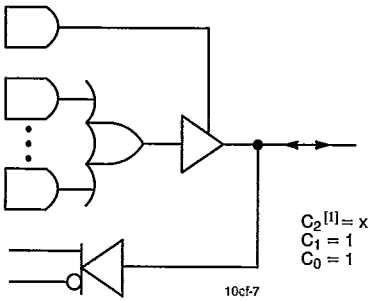
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

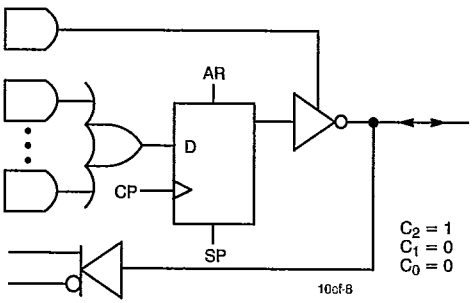


I/O FEEDBACK, COMBINATORIAL, ACTIVE-LOW OUTPUT

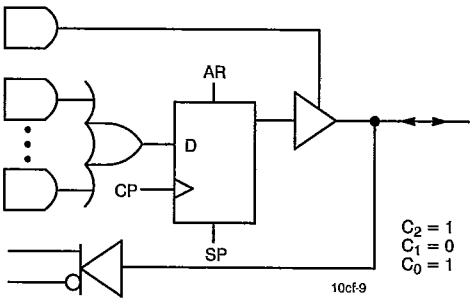


I/O FEEDBACK, COMBINATORIAL, ACTIVE-HIGH OUTPUT

Figure 1. PAL22V10CF and PAL22VP10CF Macrocell Configurations



I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

Figure 2. Additional Macrocell Configurations for the PAL22VP10CF

Selection Guide

	22V10CF–7 22VP10CF–7	22V10CF–10 22VP10CF–10
I_{CC} (mA)	190	190
t_{PD} (ns)	7.5	10
t_S (ns)	3.0	3.6
t_{CO} (ns)	7.0	7.5
f_{MAX} (MHz)	100	90

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to V_{CC}

DC Input Voltage ..... – 0.5V to V_{CC}

DC Input Current ..... – 30 mA to +5 mA (except during programming)

DC Program Voltage 10V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = – 3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[2]		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[2]			0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le 2.7V$, V_{CC} = Max.		– 250	50	µA
I_I	Maximum Input Current	V_{IN} = V_{CC}, V_{CC} = Max.			100	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$		– 100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]		– 30	– 120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open			190	mA

Notes:

2. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Switching Characteristics[4]

Parameters	Description	22V10CF–7 22VP10CF–7		22V10CF–10 22VP10CF–10		Units
		Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[5]	2	7.5	2	10	ns
t_{EA}	Input to Output Enable Delay	2	7.5	2	10	ns
t_{ER}	Input to Output Disable Delay[6]	2	7.5	2	10	ns
t_{CO}	Clock to Output Delay[5]	1	7.0	1	7.5	ns
t_S	Input or Feedback Set-Up Time	3		3.6		ns
t_H	Input Hold Time	0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	10		11.1		ns
t_{WH}	Clock Width HIGH[7]	3		3		ns
t_{WL}	Clock Width LOW[7]	3		3		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[8]	100		90		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[7, 9]	166		166		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[10]	133		100		MHz
t_{CF}	Register Clock to Feedback Input[11]		4.5		6.4	ns
t_{AW}	Asynchronous Reset Width	8.5		10		ns
t_{AR}	Asynchronous Reset Recovery Time	5		6		ns
t_{AP}	Asynchronous Reset to Registered Output Delay	2	12	2	12	ns
t_{SPR}	Synchronous Preset Recovery Time	5		6		ns
t_{PR}	Power-Up Reset Time[12]	1		1		µs

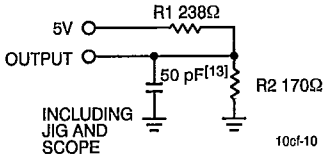
Capacitance[7]

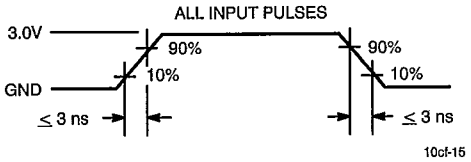
Parameters	Description	Max.	Units
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	10	pF

Notes:

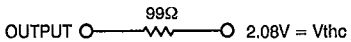
4. AC test load used for all parameters except where noted.
5. This specification is guaranteed for all device outputs changing state in a given access cycle.
6. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
7. Tested initially and after any design or process changes that may affect these parameters.
8. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
9. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
11. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 10) minus t_S.
12. The registers in the PAL22V10CF/PAL22VP10CF have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

AC Test Loads and Waveforms

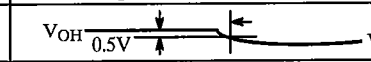
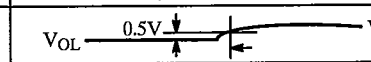
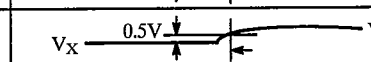
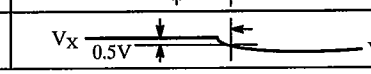




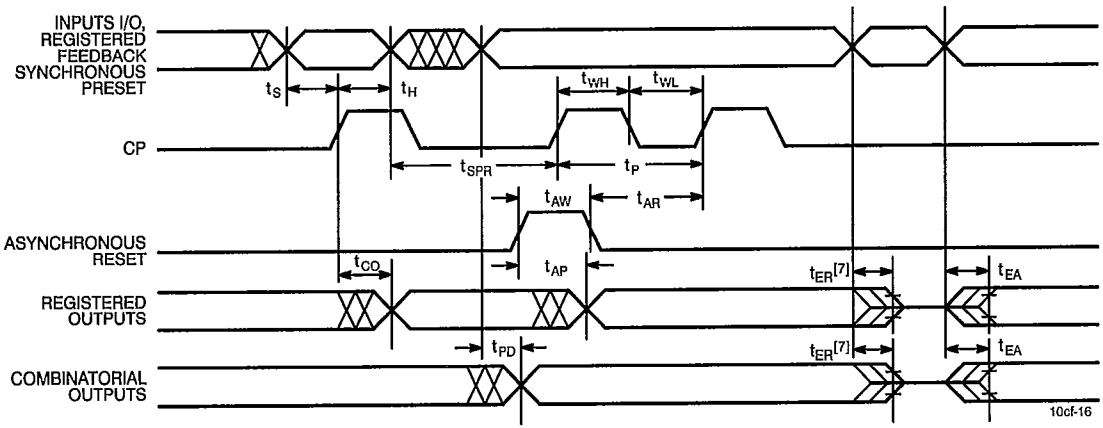
Equivalent to: THÉVENIN EQUIVALENT



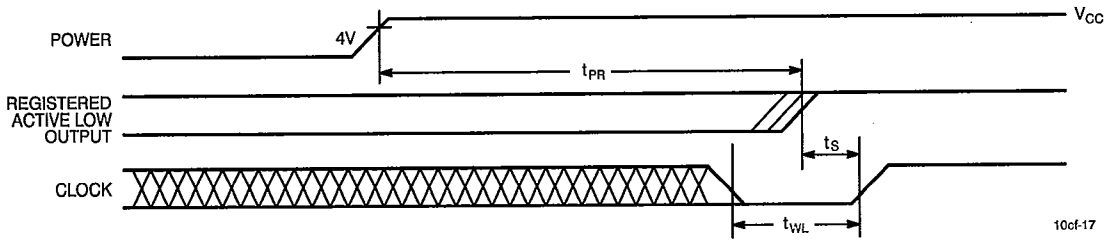
Commercial

Parameter	V_X	Output Waveform—Measurement Level
t_{ER} (–)	1.5V	 10cf-11
t_{ER} (+)	2.6V	 10cf-12
t_{EA} (+)	1.5V	 10cf-13
t_{EA} (–)	1.5V	 10cf-14

Switching Waveform

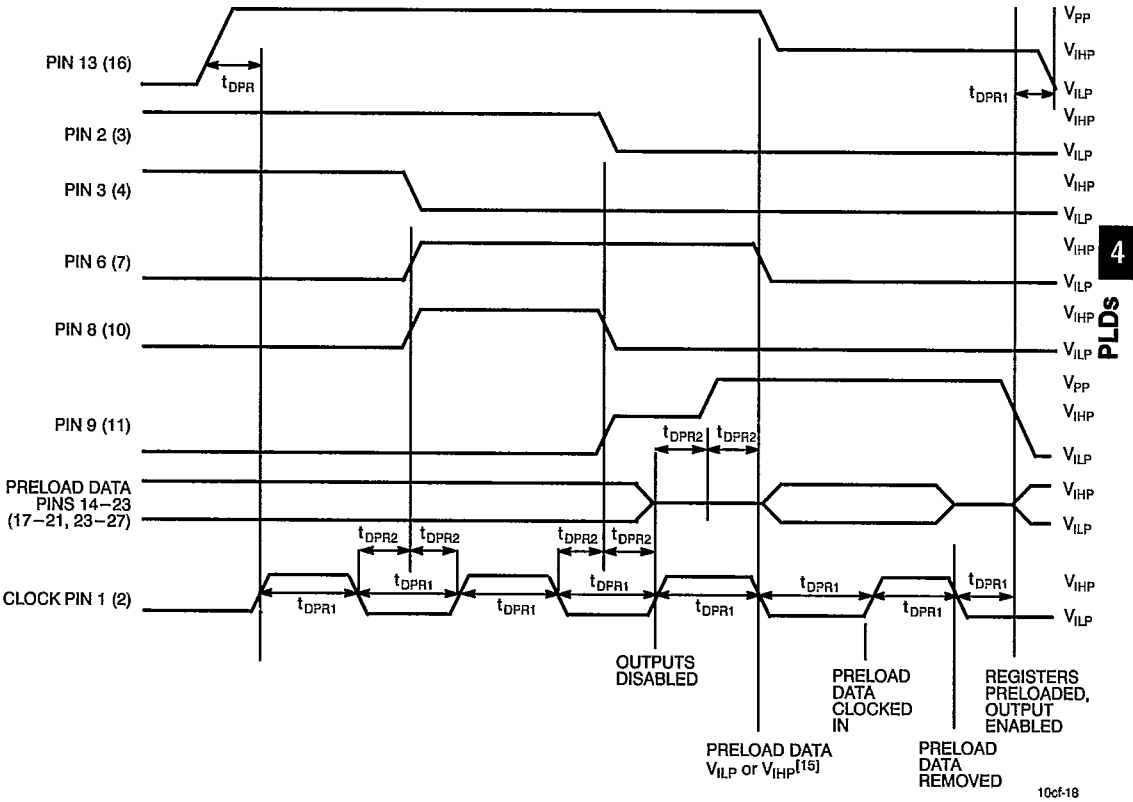


Power-Up Reset Waveform[13]



Notes:
13. C_L = 5 pF for t_{ER} measurement for all packages.

Preload Waveform[14]



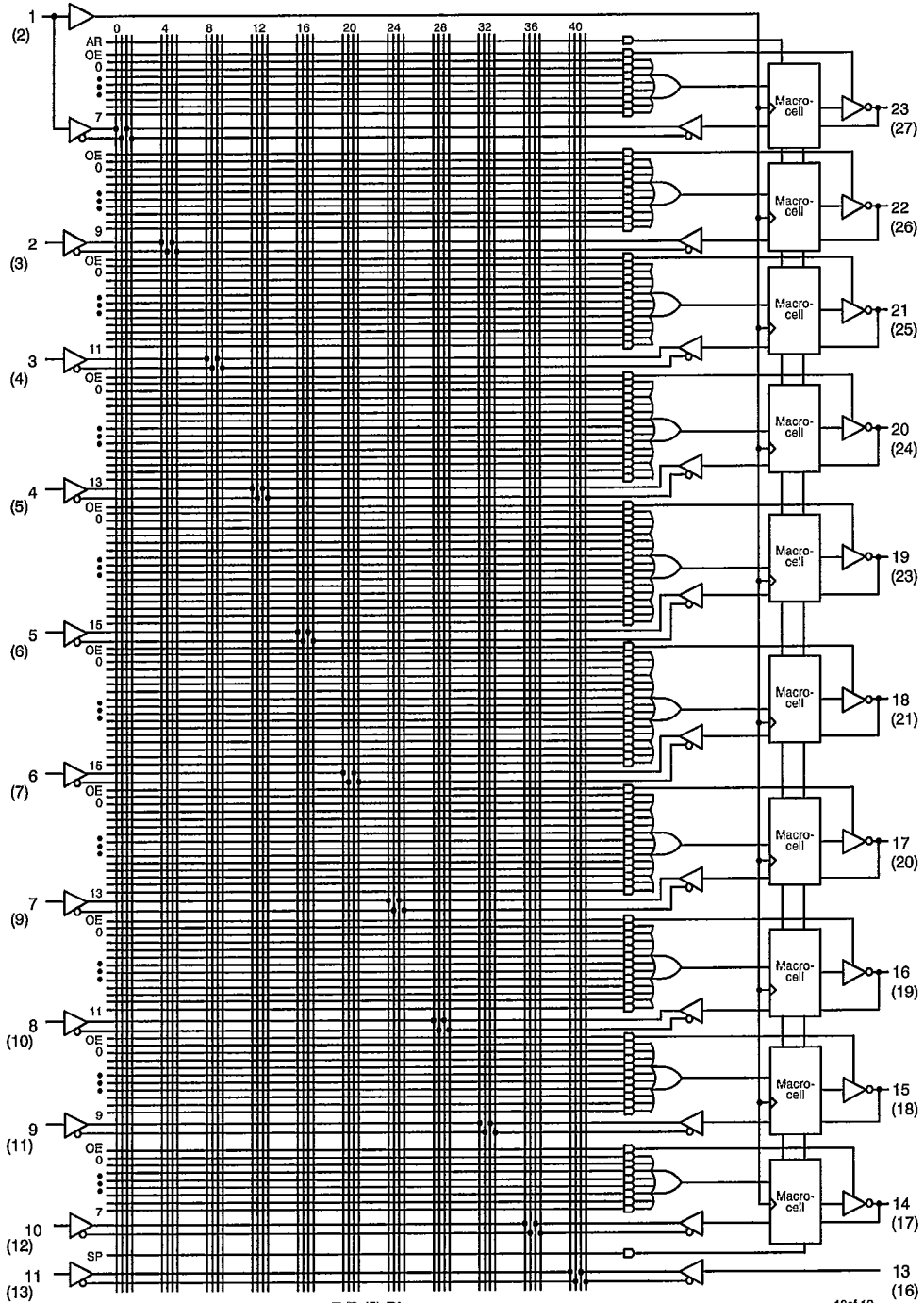
Notes:
14. Pins 4 (5), 5 (6), 7 (9) at V_{ILP}; Pins 10 (12) and 11 (13) at V_{IHP}; V_{CC} (Pin 24 (1 and 28)) at V_{CCP}
15. Pins 2–8 (3–7, 9, 10), 10 (12), 11 (13) can be set at V_{IHP} or V_{ILP} to insure asynchronous reset is not active.

D/P (J) Pinouts

Forced Level on Register Pin During Preload	Register Q Output State After Preload
V_{IHP}	HIGH
V_{ILP}	LOW

Name	Description	Min.	Max.	Unit
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR1}	Delay for Preload	1		µs
t_{DPR2}	Delay for Preload	0.5		µs
V_{ILP}	Input LOW Voltage	0	0.4	V
V_{IHP}	Input HIGH Voltage	3	4.75	V
V_{CCP}	V_{CC} for Preload	4.75	5.25	V

Functional Logic Diagram for PAL22V10CF/PAL22VP10CF



D/P (J) Pinouts

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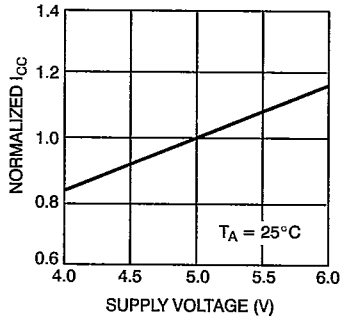
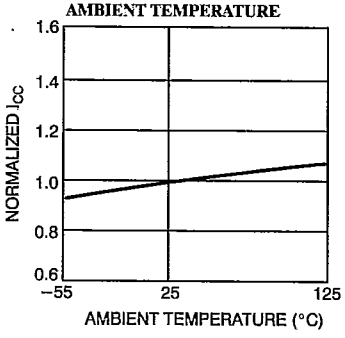
Typical DC and AC Characteristics

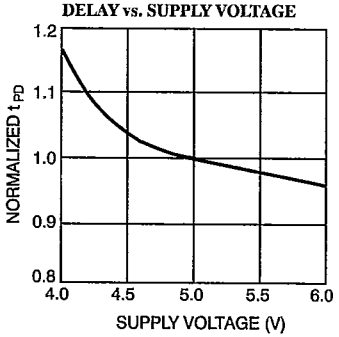
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



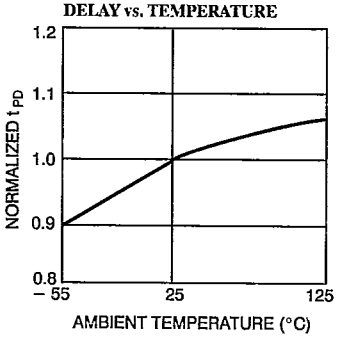
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



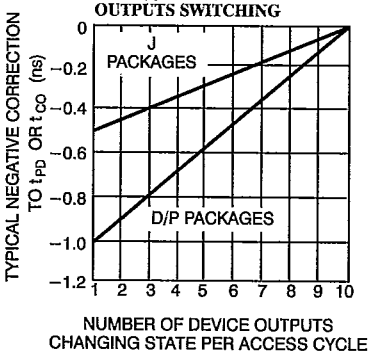
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



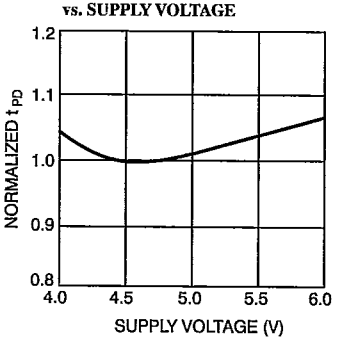
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



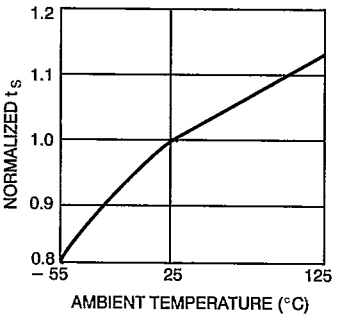
TYPICAL CORRECTION TO t_{PD} AND t_{CO} vs. NUMBER OF OUTPUTS SWITCHING



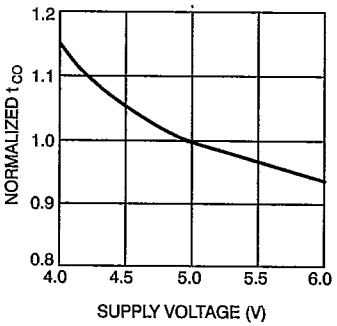
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



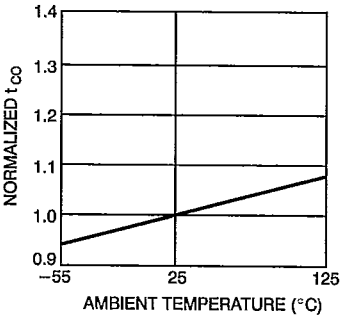
NORMALIZED SET-UP TIME vs. TEMPERATURE



NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



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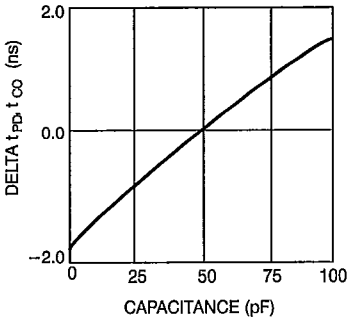
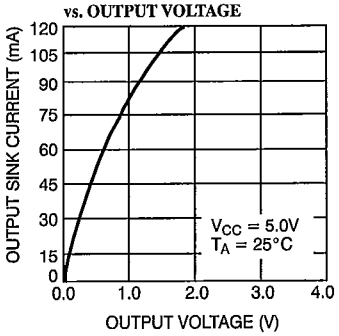
Typical DC and AC Characteristics (continued)

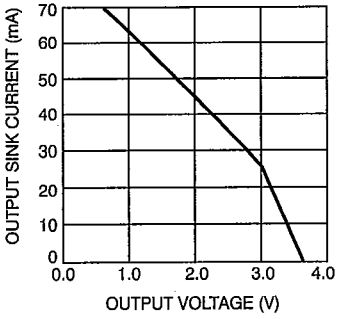
DELTA t_{PD}, t_{CO} vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



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Ordering Information

I_{CC} (mA)	t_{AA} (ns)	f_{MAX} (MHz)	Ordering Code	Package Type	Package Type	Operating Range
190	7.5	100	PAL22V10CF–7DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10CF–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10CF–7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10CF–7DC	D14	24-Lead (300-Mil) CerDIP	
			PAL22VP10CF–7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10CF–7PC	P13	24-Lead (300-Mil) Molded DIP	
	10	90	PAL22V10CF–10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PAL22V10CF–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10CF–10PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10CF–10DC	D14	24-Lead (300-Mil) CerDIP	
			PAL22VP10CF–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10CF–10PC	P13	24-Lead (300-Mil) Molded DIP	

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CYPRESS SEMICONDUCTOR

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PLCC and CLCC Packaging for High-Speed Parts

The semiconductor industry is constantly searching for package options that enhance the capabilities of high-performance devices. For fast device performance with minimal ground bounce, electrical characteristics must include low inductance and capacitance from external pin to die bond-wire pad. A package should also furnish good thermal characteristics for reliability over extended temperature ranges.

Other major properties sought after are low cost, as well as standardized outline/pin configurations for compatibility, ease of manufacturing, and handling throughput. The package must also work with surface mount technology and have a small footprint to save board space.

The package that best meets all these requirements is the PLCC (plastic leaded chip carrier). In the past, utilization of PLCCs was not practical for high-power, bipolar devices. However, the advent of low-power bipolar and BiCMOS ECL-compatible SRAMs and PLDs now provides the opportunity for high-volume usage. As manufacturers switch from bipolar to BiCMOS, the lower power dissipation of high-density ECL SRAMs and complex PLDs promise to give PLCC packages a bright future. For military applications and extended temperature environments or for devices with higher power dissipation, you can substitute the CLCC (ceramic leaded chip carrier).

The PLCC has many desirable qualities:

- Suitable for surface mounting with J-type leads
- Small footprint to save board space
- Low inductance and capacitance for high speed with little ground-bounce
- Good thermal characteristics for reliability over temperature range
- Ease of manufacturing and handling for production throughput
- Low cost compared to CERDIP, flatpack, LCC
- Standard package outline and pin-configuration compatibility

The PLCC's J-type surface-mount leads have the advantage over gull-wing leads, which are susceptible to fatigue. J leads also enhance handling ease in test and burn-in fixtures. The PLCC's 1-pF capacitance compares favorably with the 3 and 6 pF for plastic DIPs and CERDIPs, and inductance is equally impressive: 2 nH versus 6 and 11 nH for plastic DIP and CERDIP. Unlike flatpacks, PLCCs are available in standard tooling. PLCCs come in a variety of pin configurations, from 18 to over 200 pins, versus a maximum of 40 pins for plastic DIPs.

The Ceramic Leaded Chip Carrier

For high-temperature environments and high-power devices, you can make use of the ceramic leaded chip carrier (CLCC, Y package), which can also be surface mounted. The Y package has the same footprint and J leads as the PLCC (*Figure 1*) and works well for the faster PLDs and SRAMs.

If you do not know system temperature in the early stages of a design, you can substitute the Y package for the PLCC and vice versa, so long as the device's die junction temperature does not exceed 150°C. The Y package is slightly more expensive than the PLCC, but with a thermal resistance from junction to ambient (Θ_{JA}) of 35°C/W at 500 LFPM, the Y package can dissipate heat more efficiently.

Reliability

Cypress's bipolar and BiCMOS products in PLCC and CLCC packages go through extensive burn-in and testing at elevated temperature to guarantee package integrity. Cypress strongly recommends 500-LFPM system forced air flow but guarantees reliability in systems with or without the flow if the ambient air does not cause the junction temperature (T_J) to exceed 150°C.

The PLCC's Θ_{JA} is approximately 45°C/W. The SRAMs have power dissipation that ranges from 780 mW max for the CY100E422L-5 up to 1097 mW max for the CY10E474L-5. This dissipation results in junction temperature rises from 35 to 49°C. The 16P4-type PLD (CY100E302L-6) has a temperature rise of 39°C, and the

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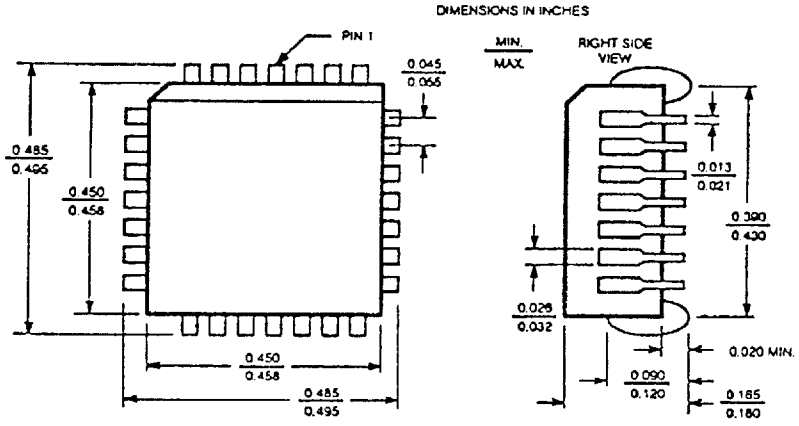
28-Lead Plastic Leaded Chip Carrier J64



28-Pin Ceramic Leaded Chip Carrier Y64

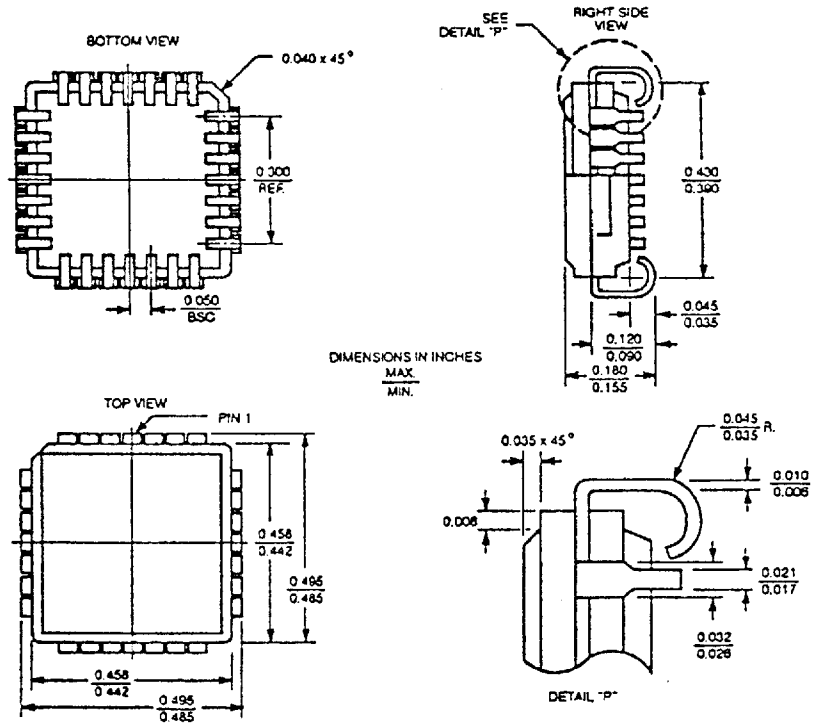


Figure 1. Diagrams of 28-Lead Chip Carriers

16P8-type PLD (CY10E301L-6) has a temperature rise of 47°C. The CLCC package's Θ_{JA} equals 35°C/W for temperature rises of up to 55°C (CY10E474-3).

Finding Chip-Level Junction Temperature

The following relationship determines chip-level junction temperature for the PLCC package:

$T_J = \Delta T + T_A$

where

$\Delta T = P_D \times \Theta_{JA}$

and

$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$

To calculate worst case junction temperature (T_J) use maximum supply V_{EE} and I_{EE} for power dissipation and maximum T_A for the temperature range of interest. For the 10K/10KH CY10E301L in a PLCC, for example, device I_{EE} = 170 mA max and V_{EE} = 5.46V max for P_D = 928 mW. Add 15 mW per output for a total output P_D = 120 mW. Therefore, the total P_D = 1048 mW.

For a PLCC, Θ_{JA} = 45°C/W at 500 LFPM, and Θ_{JA} = 64°C/W for still air.

For a CLCC, Θ_{JA} = 35°C/W at 500 LFPM, and Θ_{JA} = 54°C/W for still air.

Because

T_J = total $P_D \times \Theta_{JA} + T_A$

and

T_A = 75°C worst-case commercial temperature range, for the PLCC:

$T_J = (1.048\ W)(45°C/W) + 75°C = 122°C$ at 500 LFPM

$T_J = (1.048\ W)(64°C/W) + 75°C = 142°C$ in still air

This calculation is for absolute worst-case data sheet conditions. The burn-in temperature used by Cypress (T_J) is much higher than the device will ever see in a system. Note that *most systems will not run at worst case due to guard-banding*. For this reason, use V_{EENOM} = 5.2V or 4.5V and $I_{EENOM} = (I_{EEMAX})(85\%)$ for nominal-condition calculations.

Real-World Values

Obviously, most systems do not operate at the worst-case conditions. Therefore, *Figures 2* through *5* show graphs over different operating conditions to determine failures in time (FITs) and mean time between failure (MTBF) for a typical system or in a worst-case scenario.

The graphs are based on a linear method of interpreting the failures observed at burn-in and indicate the long-term reliability of Cypress devices. You can use the graphs to determine MTBF and FITs for any Cypress device in any package after calculating the appropriate ΔT.

The X-axis on the graphs indicates junction temperature. These values are determined by adding the ΔT to ambient temperature, as described earlier. As an example, *Figures 2* and *3* note the following critical points for a CY10E301L ECL PLD under three different operating conditions:

- Point A — 10K/10KH typical data sheet conditions: 25°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 64°C, FITs = 7, MTBF = 18,000 yrs.
- Point B — 10K/10KH typical operating conditions: 55°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 94°C, FITs = 45, MTBF = 2800 yrs.
- Point C — 10K/KH absolute worst-case conditions: 75°C ambient, 5.46 V max and 170 mA max, 50Ω loads, 500 LFPM air flow, T_J = 122°C, FITs = 225, MTBF = 525 yrs.

The activation energy used for the MTBF and FITs information is 0.7 eV. This is an average number for die-surface-related defects, such as metal and oxide pinholes, etc., but is very conservative for silicon defects or mechanical interfaces to packages. The number is usually 1.0 eV. A small change here results in a significant change in MTBF or FITs. A change to 0.8 eV equates to a 33% reduction in FITs rate or a 50% increase in MTBF.

The Packages of Choice

The PLCC and CLCC are accepted as the packages of choice by many manufacturers of high-speed devices. Motorola Semiconductor uses the PLCC as the only package for the company's very high speed ECL$_{INPS}$ ECL logic family, which stands for "ECL in picoseconds" and is pronounced "eclipse." This family has set-up times and propagation delays in the sub-nanosecond range, with power dissipation of over 1W. Fully compatible with Cypress SRAMs and PLDs, the ECL$_{INPS}$ family includes many 10K, 10KH, and 100K standard logic gates, building blocks, and transceivers.

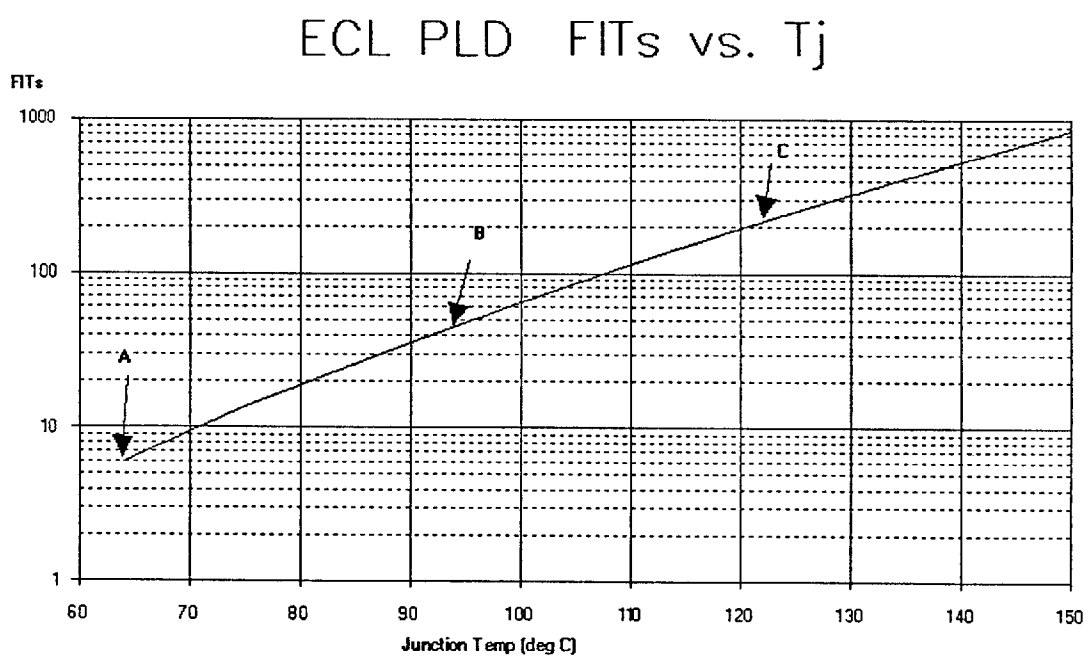


Figure 2. Failures in Time vs Junction Temperature

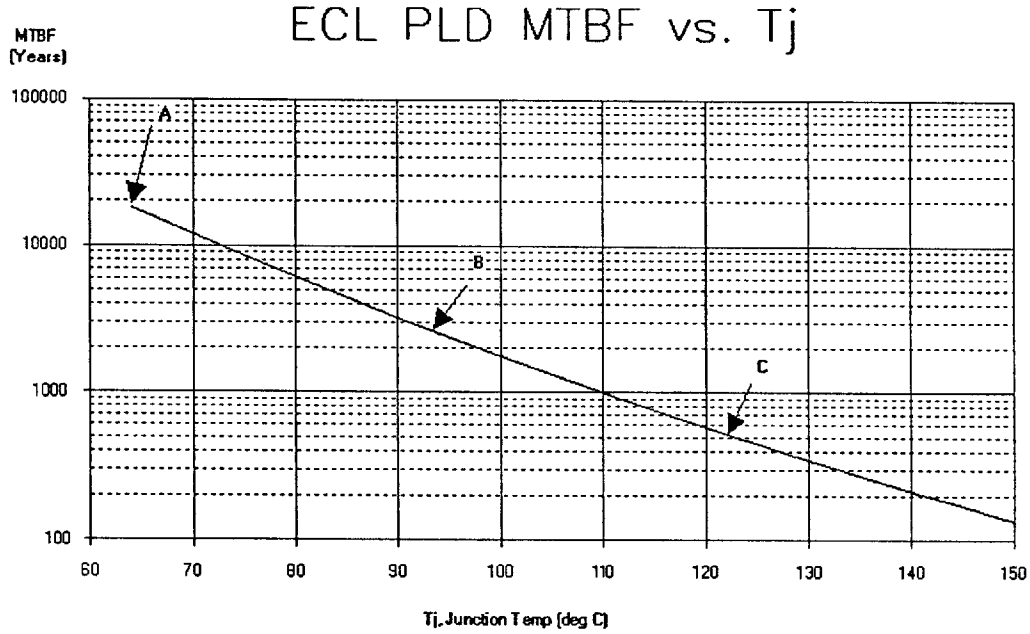


Figure 3. Mean Time Between Failures vs Junction Temp.

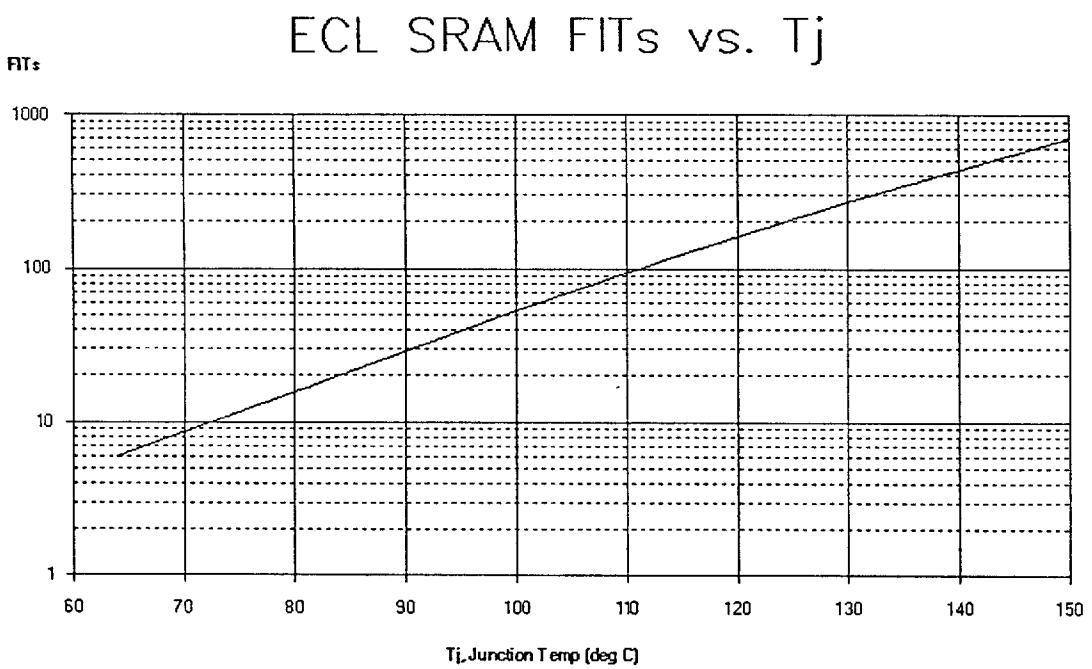


Figure 4. Failures in Time vs Junction Temperature

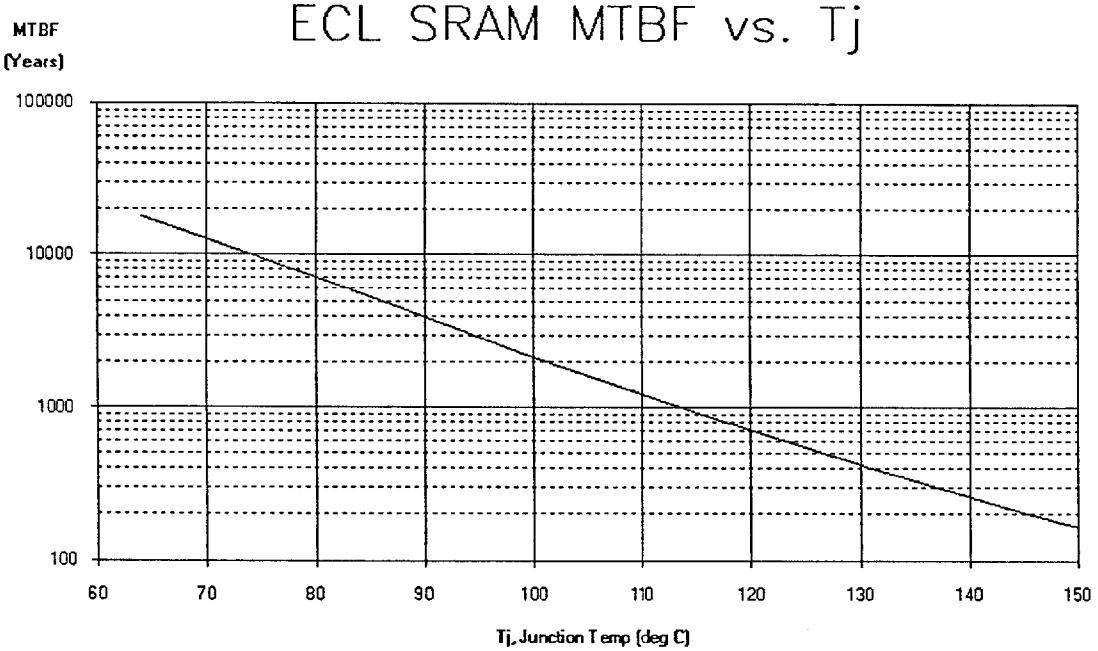


Figure 5. Mean Time Between Failure vs Junction Temp.