T-79-07-10

9740

DATA AND SPECIFICATIONS
DESCRIPTION AND INSTRUCTIONS

Optical Electronics Incorporated

FET INPUT HIGH SLEWING RATE OPERATIONAL AMPLIFIER

FEATURES

- SLEW RATE: ±3000V/μsec
- SETTLING TIME: 100ns to 0.1%
- OUTPUT: ±10V, ±50mA
- DIFFERENTIAL INPUT
- DRIFT: 20 μV/° C

APPLICATION

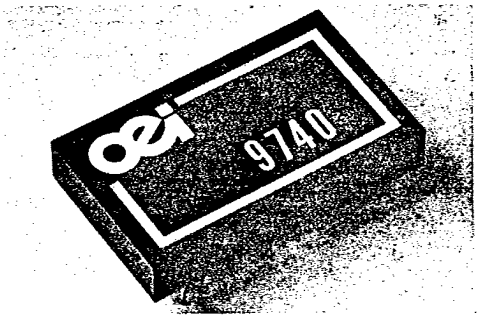
- PULSE AMPLIFIER
- TEST EQUIPMENT
- WAVE FORM GENERATOR
- FAST D/A CONVERTERS

DESCRIPTION

The 9740 is constructed of discrete devices in a modular fashion. The FET input provides a very high impedance of at least 100G ohm (10^{11}). The 3000 V/μs slew rate makes the 9740 an excellent candidate for applications in data conversion and other high speed designs. The front end contains a monolithic device to control offset and temperature drift. This makes the device applicable where these parameters must be held at a minimum.

The open loop gain is a very high 110dB minimum (120dB typically). This high gain is achieved with a unique feed forward design. The discontinuity to zero which this type of design usually shows is later compensated, so that only a small knee effect can be seen in the gain vs. frequency curve between 100KHz and 1 MHz. The two poles and one zero design provides a 6dB/octave gain vs. frequency roll off.

The 9740 will provide ±10 Volts at ±50mA drive current at the output. Internal short circuit protection is included, which will protect the device from direct short circuits across the output for extended periods of time. It operates from a standard ±15V power supply, and in the quiescent state draws approximately ±33mA. Internal compensation is provided, therefore no external power supply bypass capacitors are needed.



Due to the non-standard construction of the module housing the 9740, it is advisable to use the OEI 11028 socket for insertion in the overall design.

This very high-speed, high-output current device finds applications in very fast D/A and A/D conversion circuits. Also, of course, video communications and photo multiplier designs can benefit from the speed and bandwidth features the 9740 offers. It can be used as coaxial cable driver and in instrumentation applications, where it can serve as output amplifier. Even CRT deflection circuits or pulse amplification can be accomplished with this device.

SPECIFICATIONS

T-79-07-10

ELECTRICAL

Specifications at T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

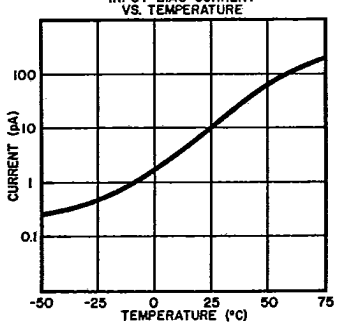
MODEL		9740			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNITS**
OPEN LOOP GAIN, DC					
No Load		110	120		dB
RATED OUTPUT					
Voltage	Io = ±50mA	±10	±12		V
Current	Vo = ±10V	±50			mA
Output Resistance				10	Ω
Max. Load Resistance		200			Ω
Capacitive Load				15	pF
DYNAMIC RESPONSE					
Gain-Bandwidth Product					
A_{CL} = 100		300			MHz
A_{CL} = −1	C_F = 5pF, Rx = 22Ω, Cx = 470pF	100			MHz
Slew Rate					
A_{CL} = −1	C_F = 5pF, Vo = ±10V	3000	4000		V/μsec
Full Power Bandwidth					
Settling Time, A_{CL} = −1					
ε = 1%	C_F = 5pF, Rx = 22Ω, Cx = 470pF			60	ns
ε = 0.1%				100	ns
Small Signal Overshoot				3	dB
INPUT OFFSET VOLTAGE					
Initial Offset			±5	±10	mV
vs Temperature	−55°C to +85°C			±20	μV/°C
INPUT BIAS CURRENT					
Initial Bias			20	30	pA
vs Temperature	−55°C to +85°C		Note 1		
VOLTAGE NOISE DENSITY Rs ≤ 100Ω					
Noise Voltage	10KHz		40	50	nV/√Hz
Noise Current	10KHz		10	20	pA/√Hz
INPUT IMPEDANCE					
Differential					
Resistance		100			GΩ
Capacitance				5	pF
Common-Mode					
Resistance		100			GΩ
Capacitance				5	pF
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range	Linear Operation			±1	V
Common-Mode Rejection	at 1KHz	90			dB
POWER SUPPLY					
Rated Voltage		±7	±15	±20	V
Quiescent Current	Vcc = ±15V			±33	mA
TEMPERATURE RANGE					
Specification		-55		+85	°C
Operating		-55		+100	°C
Storage		-65		+100	°C

NOTE:
9740 1) Doubles approximately every 10°C.

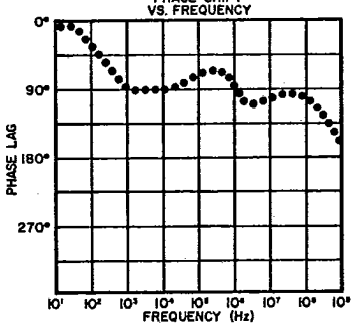
9740
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted)

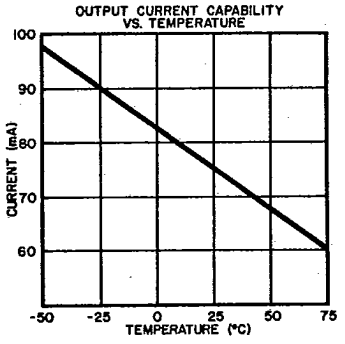
INPUT BIAS CURRENT VS. TEMPERATURE



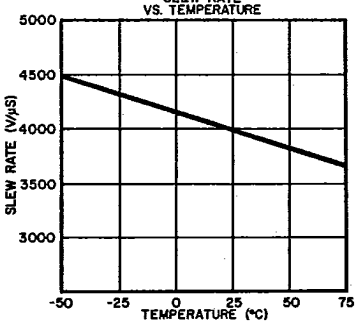
PHASE SHIFT VS. FREQUENCY



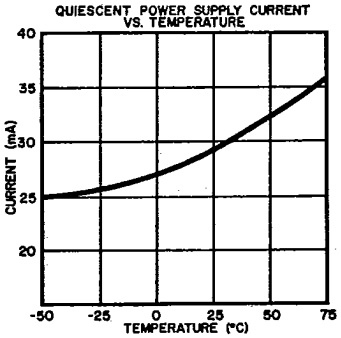
OUTPUT CURRENT CAPABILITY VS. TEMPERATURE



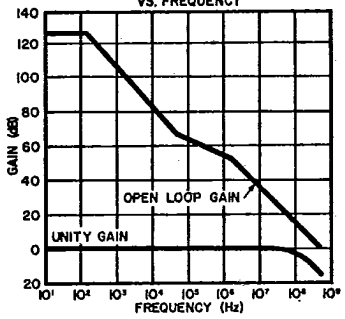
SLEW RATE VS. TEMPERATURE



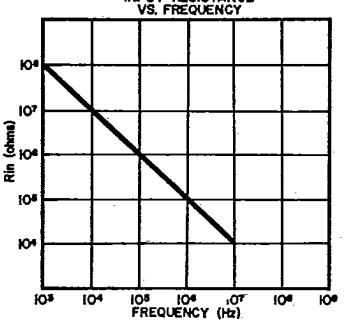
QUIESCENT POWER SUPPLY CURRENT VS. TEMPERATURE



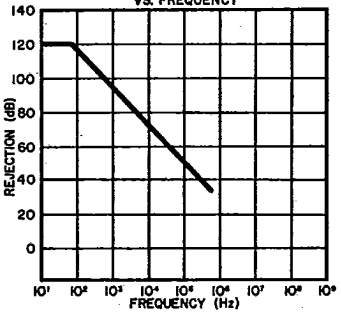
OPEN LOOP GAIN AND UNITY GAIN VS. FREQUENCY



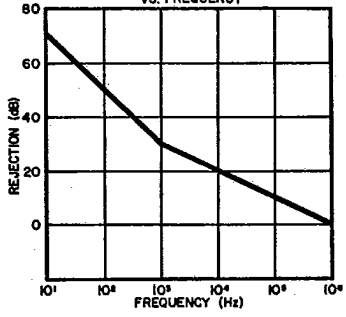
INPUT RESISTANCE VS. FREQUENCY



COMMON MODE REJECTION VS. FREQUENCY

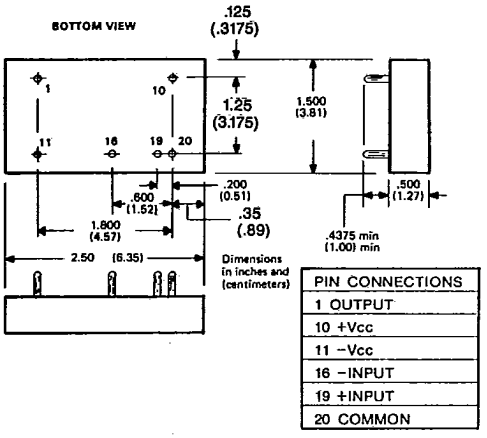


POWER SUPPLY REJECTION VS. FREQUENCY



T-79-07-10

MECHANICAL DESCRIPTION: The circuit is enclosed in a glass-fiber-filled, diallyl-phthalate case and epoxy encapsulant. Its six pins are gold-plated and are 0.040 in (0.102 cm) in diameter.



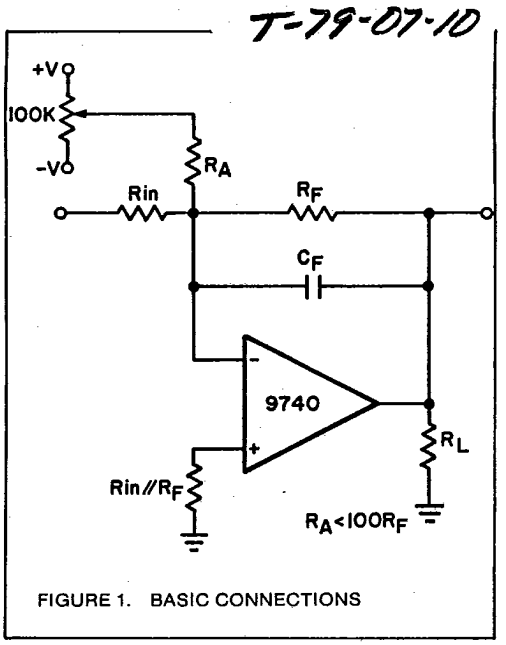


FIGURE 1. BASIC CONNECTIONS

APPLICATIONS

The design of the 9740 FET input op amp is geared to very high slew rate, fast settling time applications and for designs which combine these high performance parameters with high voltage and current drive requirements. The 3000V/μs slewing rate can be coupled with the $\pm$50mA at $\pm$10V drive capability and this combination gives the 9740 an edge over many similar devices. Because of the FET input, very high impedance and therefore very low bias currents can be realized. The only thing the designer should be aware of is the requirement to maintain the lowest possible capacitive loads for input and output. Internal power supply decoupling is provided and therefore need not be considered. Also, the output is short circuit protected and no additional requirements need be met.

BASIC CONNECTIONS

The basic connections to the device are depicted in figure 1. Although the inverting mode is shown, the device can be used in the noninverting mode with the same results.

In this case, the signal is applied via the input resistor, which in part determines the gain to the summing node. The other part of the gain is of course determined by the feedback R_F. This resistor is bypassed by the feedback capacitor for compensation at high frequencies. The resistor from the noninverting node to ground should not be larger than the value of R_{in} and R_F in parallel. This resistor is used to balance bias currents from the 9740.

The offset current can be adjusted by the linear pot connected to the rails of the power supply and the resistor R_A from the wiper to the summing node of the amplfier. As shown in the note on the figure, this fixed value resistor should be kept to less than one hundred times the feedback resistance. A typical value is 10M ohm.

The load resistor R_L can be chosen to match the input impedance of the following stage or to determine the drive current from the device.

D/A CONVERTER

High-speed D/A conversion systems are an application area where the high slew rate, wide bandwidth, and fast settling time are important parameters. In figure 2 (following page) a circuit is depicted which employs the 9740 in a 12 bit system. Here the DAC-8528 from the Data Device Corporation is assumed to provide the input to the OEI Device. The 8528 has an internal op amp, but better performance can be achieved by use of its current output, which exhibits a 60ns settling time. The voltage output is with a 1μs settling time, 17 times slower. The 9740 has a 100ns settling time (to 0.1%) and is therefore much better matched to the current output of the DAC. In addition, the 9740 exhibits a max 30pA bias current and thus contributes very little error to the system. This is an important consideration, particularly in a 12 bit system, where residual currents can cause appreciable system errors.

The design shown exemplifies operation in the 4mA drive current range. The 2.5K ohm feedback resistor allows the full ±10V output swing.

The compensation capacitor will yield the 3000V/μs slew rate the device is capable of and compensates any input capacitance that might appear. The small resistor in the output leg is inserted to somewhat dampen the output, should there be an over- or under-shoot tendency in the signal. The output resistor R_L can be chosen to match the following stage and to allow selection of drive current.

T-79-07-10

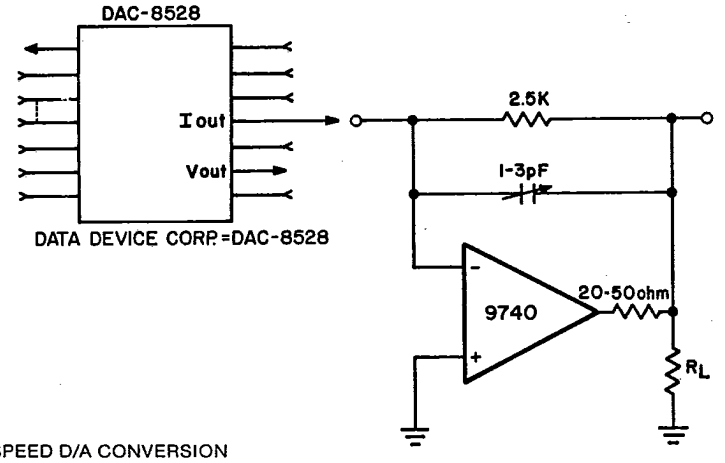


FIGURE 2. HIGH SPEED D/A CONVERSION

TEST EQUIPMENT

The circuit of figure 3 exemplifies use of the 9740 as an inverting amplifier with a gain of 10, as it might be used in high speed applications in test equipment. The input signal is applied via the input resistor of 1K ohm to the summing node. The 51 ohm resistor is inserted to terminate the input line and neutralize input capacitance. Since the gain of this stage is set to 10, no lead/lag network across the input is needed. Of course, this decision also depends on how carefully the layout is designed, because the load capacitance influences the use of this network. The layout given at the end of this section shows a typical example of a good design. The feedback resistor, together with the input resistor, determines the gain of the stage.

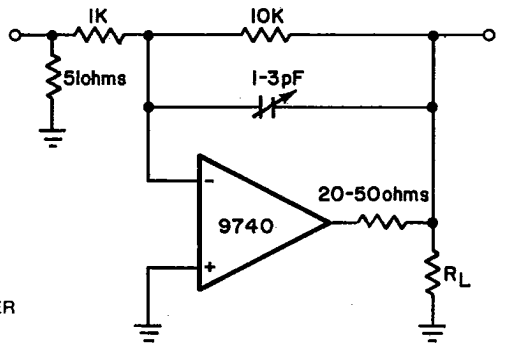


FIGURE 3. INVERTING AMPLIFIER FOR TEST EQUIPMENT

The capacitor parallel to the feedback resistor helps to compensate for input stray capacitance. The small resistor in the output dampens the circuit somewhat to help eliminate overshoot that might be present in the input signal. The load resistor R_L determines the impedance for the following stage and can be chosen by the designer to best fit his needs. The circuit is capable of a ±50mA drive current at a full ±10V output voltage swing. The low drift and good DC characteristics together with the outstanding AC performance make this a very versatile circuit.

PULSE AMPLIFIER

If the requirement exists for a high-speed, fast-settling pulse amplifier, the diagram in figure 4 fits very nicely. Here the amplifier is set for unity gain, since both the input and the feedback resistor are each 1K ohm. The input signal is terminated into 51 ohms and this resistor, together with the capacitor appearing in parallel to the feedback resistor, compensates for stray capacitance that might appear at the input to the 9740.

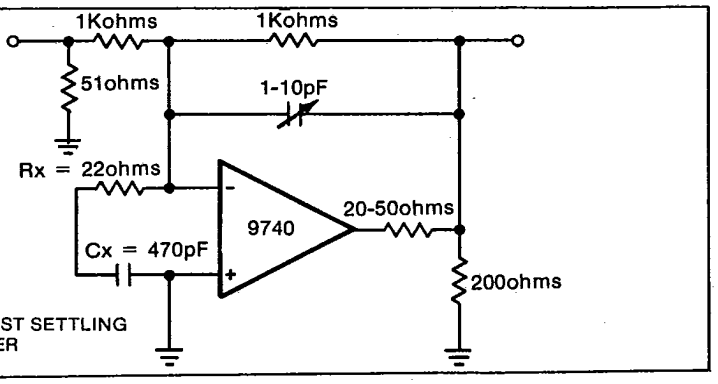


FIGURE 4. HIGH SPEED FAST SETTLING PULSE AMPLIFIER

Since the gain figure is less than 10, a lead/lag network is connected across the inverting and noninverting inputs of the amplifier. This then will eliminate possible oscillations, which the operation near the 180° phase shift point can set up. The values shown are typical for this network. For other gain figures below 10, the two elements can be obtained from the two equations:

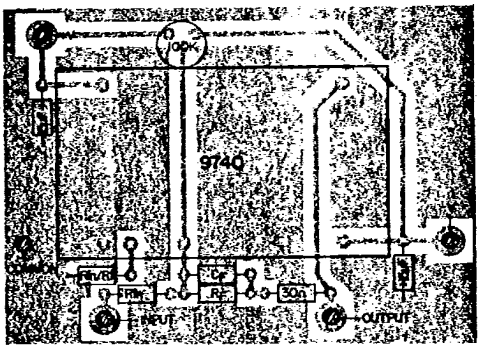
$$C_X = 0.1/R_F(\mu F)$$
$$R_X = 0.01\ R_F(ohm)$$

When the lead/lag circuit is designed, it should be remembered that its use is directed mainly at the suppression of oscillations at the upper frequency range. If the values are chosen too large, the effect will be a slowdown of the overall circuit and thus performance degradation. Some experimentation may be needed to arrive at the best compromise.

As mentioned before, the resistor in the output is used to dampen potential overshoot conditions in the input signal and R_L is, at 200 ohms, set to deliver a full ±10 Volt swing at ±50mA drive current. This will, in many cases, allow elimination of a separate driver stage.

A typical PC board layout that minimizes design problems and maximizes the performance of the 9740 is shown in figure 5.

FIGURE 5. PC BOARD LAYOUT (TYPICAL)



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