PALCE29M16H-25/35

24-Pin E²-Based CMOS Programmable Array Logic

T-46-13-47

DISTINCTIVE CHARACTERISTICS

- High-performance semicustom logic replacement; Electrically Erasable (E²) technology allows reprogrammability
- 16 bidirectional user-programmable I/O logic macrocells for Combinatorial/Registered/Latched operation
- Output Enable controlled by a pin or product terms
- Varied product term distribution for increased design flexibility
- Programmable clock selection with two clocks/latch enables ($\overline{LE}$s) and LOW/HIGH clock/$\overline{LE}$ polarity
- Register/Latch PRELOAD permits full logic verification
- High speed (t_{PD} = 25 ns, f_{MAX} = 33 MHz and f_{MAX} internal = 50 MHz)
- Full-function AC and DC testing at the factory for high programming and functional yields and high reliability
- 24-pin 300-mil SKINNYDIP® and 28-pin chip carrier packages

GENERAL DESCRIPTION

The PALCE29M16H is a high-speed, E²-based CMOS Programmable Array Logic device designed for general logic replacement in TTL or CMOS digital systems. It offers high speed, low power consumption, high programming yield, fast programming and excellent reliability. Programmable Array Logic (PAL®) devices combine the flexibility of custom logic with the off-the-shelf availability of standard products, providing major advantages over other semicustom solutions such as gate arrays and standard cells, including reduced development time and low up-front development cost.

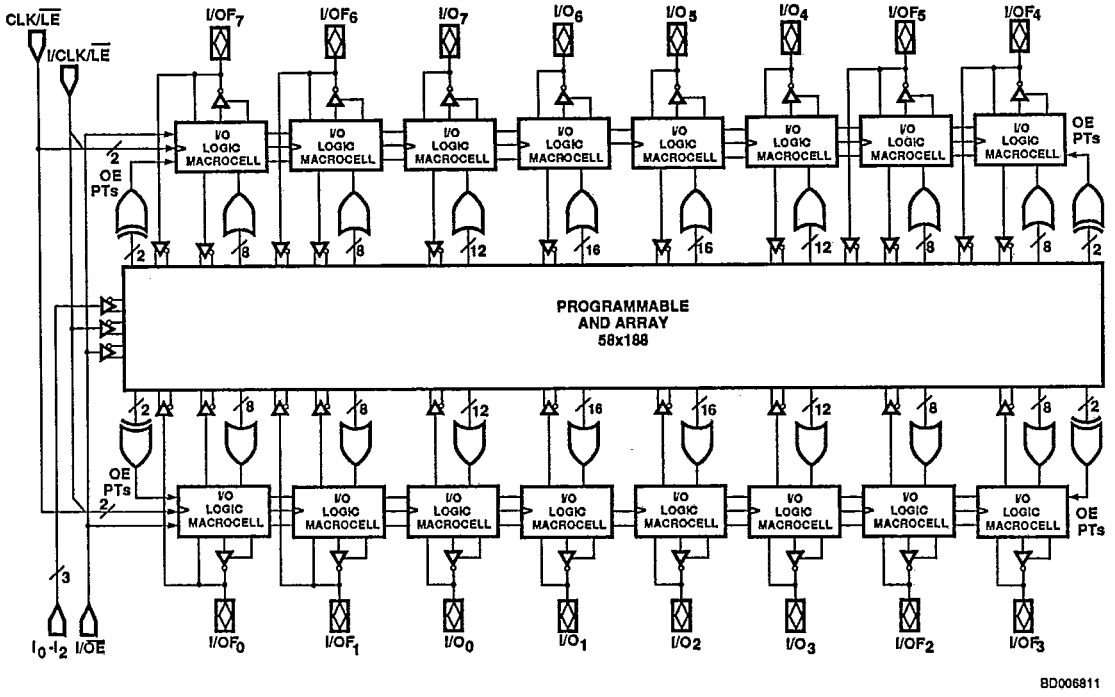


Figure 1. Block Diagram

Monolithic Memories AMD

PAL, PALASM and SKINNYDIP are registered trademarks of Advanced Micro Devices.

Publication # 08740 Rev. C Amendment /0
Issue Date: December 1988

GENERAL DESCRIPTION (continued)

The PALCE29M16H uses the familiar sum-of-products (AND-OR) structure, allowing users to customize logic functions by programming the device for specific applications. It provides up to twenty-nine array inputs and sixteen outputs. It incorporates AMD's unique input/output logic macrocell which provides flexible input/output structure and polarity, flexible feedback selection, multiple Output Enable choices, and a programmable clocking scheme. The macrocells can be individually programmed as "Combinatorial", "Registered", or "Latched" with active-HIGH or active-LOW polarity. The flexibility of the logic macrocells permits the system designer to tailor the device to particular application requirements.

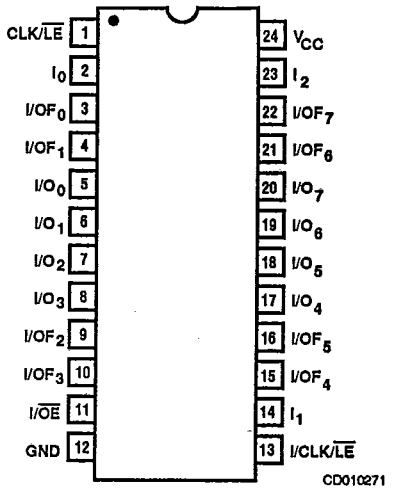
Increased logic power has been built into the PALCE29M16H by providing a varied number of logic product terms per output. Eight outputs have eight product terms each, four outputs have twelve product terms each, and the other four outputs have sixteen product terms each. This varied product-term distribution allows complex functions to be implemented in a single PAL device. Each output can be dynamically controlled by a common Output Enable pin or Output Enable product terms per bank of four outputs. Each output can also be permanently enabled or disabled.

System operation has been enhanced by the addition of common asynchronous-PRESET and RESET product terms and a power-up RESET feature. The PALCE29M16H also incorporates PRELOAD and Observability functions which permit full logic verification of the design.

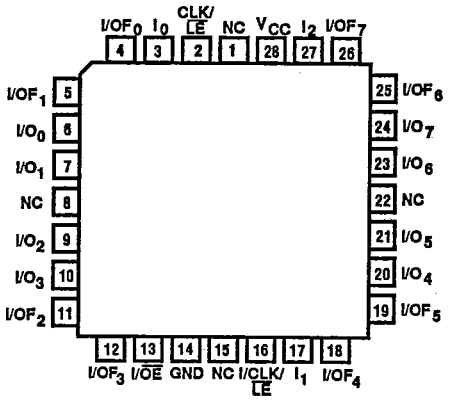
The PALCE29M16H is offered in the space-saving 300-mil SKINNYDIP package as well as the plastic leaded chip carrier package.

CONNECTION DIAGRAMS
(Top View)

SKINNYDIP



PLCC



Note: Pin 1 is marked for orientation

Pin Designations:

I	= Input	GND	= Ground
I/O	= Input/Output	CLK/$\overline{LE}$	= Clock/Latch Enable
I/OF	= Input/Output with Dual Feedback	NC	= No Connection
V_{CC}	= Supply Voltage		

PIN DESCRIPTION

The following describes the functionality of all the pins on the 24-pin DIP. The 28-pin chip carrier has the same functionality with NO CONNECTS on pins 1, 8, 15, 22.

CLK/$\overline{LE}$ (PIN 1): Used as a dedicated clock/latch enable pin for all registers/latches on the device if so selected. (See I/O Logic Macrocell Configurations.) This pin is a clock pin for macrocells configured as registers and a latch enable pin for macrocells configured as latches.

I/CLK/$\overline{LE}$ PIN (PIN 13): Used as dedicated input or as an alternate clock/latch enable pin for all the registers/latches if so selected. (see I/O Logic Macrocell Configurations.) This pin is a clock pin for macrocells configured as registers and a latch enable pin for macrocells configured as latches.

I/$\overline{OE}$ PIN (PIN 11): Used as a dedicated input pin to the AND array or as the Output Enable control pin (Active LOW) for all macrocells with pin-controlled Output Enable selected.

I_0-I_2 (PINS 2, 14, 23): Dedicated input pins.

I/OF_0-I/OF_7 (PINS 3, 4, 9, 10, 15, 16, 21, 22): Eight bidirectional I/O pins with two independent feedback paths to the AND array. The first feedback path is a dedicated I/O pin feedback to the AND array for combinatorial input. The second feedback path consists of direct register/latch feedback to the array (see Figure 2b).

I/O_0-I/O_7 (PINS 5, 6, 7, 8, 17, 18, 19, 20): Eight bidirectional I/O pins with user-programmable register/latch or I/O pin feedback to the AND array (see Figure 2a).

V_{CC} (PIN 24): Supply Voltage

GND (PIN 12): Circuit Ground.

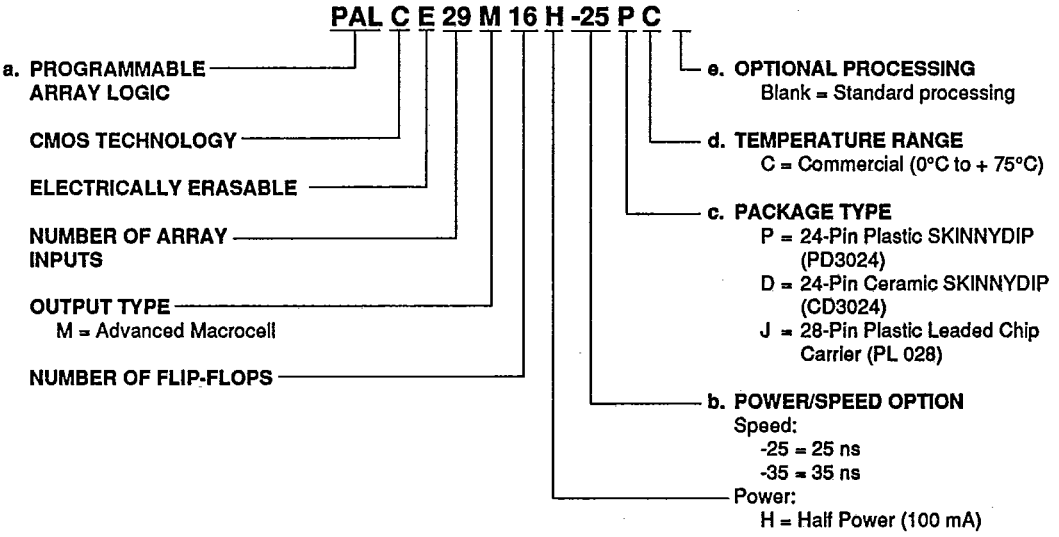
ORDERING INFORMATION

T-46-13-47

Standard Products

AMD/MMI standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Power/Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
PALCE29M16H-25/-35	PC, DC, JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

T-46-13-47

Inputs

The PALCE29M16H has twenty-nine inputs to drive each product term (up to fifty-eight inputs with both TRUE and complement versions available to the AND array) as shown in the block diagram in Figure 1. Of these twenty-nine inputs, three are dedicated inputs, sixteen are from eight I/O logic macrocells with two feedbacks, eight are from other I/O logic macrocells with single feedback, one is the I/$\overline{OE}$ input and one the I/CLK/$\overline{LE}$ input.

Initially the AND-array gates are disconnected from all the inputs. This condition represents a logical TRUE for the AND array. By selectively programming the E^2 cells, the AND array may be connected to either the TRUE input or the complement input. When both the TRUE and complement inputs are connected, a logical FALSE results at the output of the AND gate.

Product Terms

The degree of programmability and complexity of a PAL device is determined by the number of connections that form the programmable-AND and OR gates. Each programmable-AND gate is called a product term. The PALCE29M16H has 188 product terms; 176 of these product terms provide logic capability and twelve are architectural or control product terms. Among the twelve control product terms, two are for common Asynchronous-PRESET and RESET, one is for Observability, and one is for PRELOAD. The other eight are common Output Enable product terms. The Output Enable of each bank of four macrocells can be programmed to be controlled by a common Output Enable pin or two AND/XOR product terms. It may be also permanently enabled or permanently disabled.

Each product term on the PALCE29M16H consists of a 58-input AND gate. The outputs of these AND gates are connected to a fixed-OR plane. Product terms are allocated to OR gates in a varied distribution across the device ranging from eight to sixteen wide, with an average of eleven logic product terms per output. An increased number of product terms per output allows more complex functions to be implemented in a single PAL device. This flexibility aids in implementing functions such as counters, exclusive-OR functions, or complex state machines, where different states require different numbers of product terms.

Common asynchronous-PRESET and RESET product terms are connected to all Registered/Latched inputs/outputs.

When the asynchronous-PRESET product term is asserted (HIGH) all the registers/latches will immediately be loaded with a HIGH, independent of the clock. When the asynchronous-RESET product term is asserted (HIGH) all the registers/latches will be immediately loaded with a LOW, independent of the clock. The actual output state will depend on the macrocell polarity selection. The latches must be in latched mode (not transparent mode) for the RESET/PRESET, PRELOAD, and power-up RESET modes to be meaningful.

Input/Output Logic Macrocells

The I/O logic macrocell allows the user the flexibility of defining the architecture of each input or output on an individual basis. It also provides the capability of using the associated pin either as an input or an output.

The PALCE29M16H has sixteen macrocells, one for each I/O pin. Each I/O macrocell can be programmed for combinatorial, registered or latched operation (see Figure 2). Combinatorial output is desired when the PAL device is used to replace combinatorial glue logic. Registers are used in synchronous logic applications while latches are used in asynchronous applications.

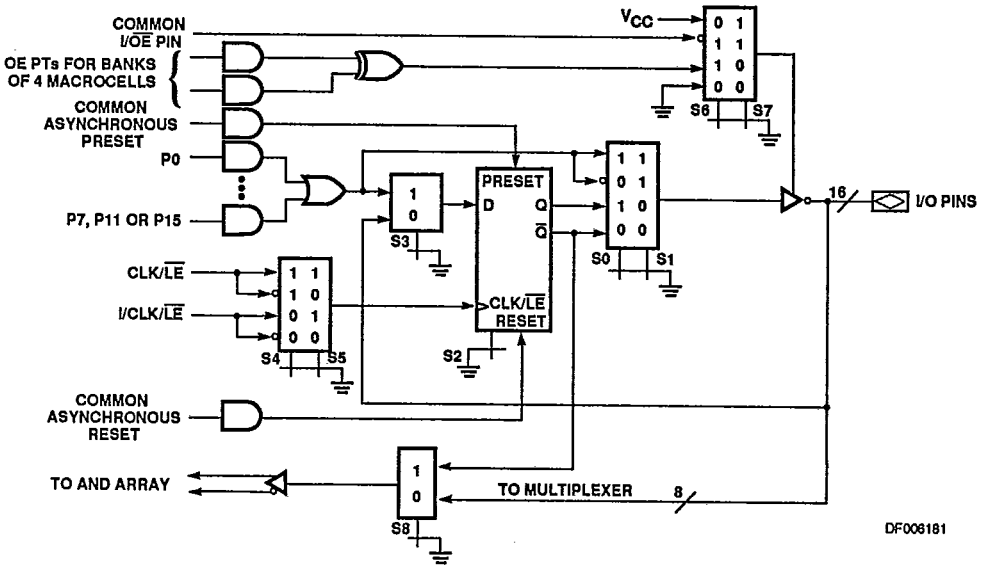


Figure 2a. PALCE29M16H Macrocell (Single Feedback)

The output polarity for each macrocell in each of the three modes of operation is user-selectable, allowing complete flexibility of the macrocell configuration.

Eight of the macrocells (I/OF_0-I/OF_7) have two independent feedback paths to the AND array (see Figure 2b). The first is a dedicated I/O pin feedback to the AND array for combinatorial input. The second path consists of a direct register/latch feedback to the array. If the pin is used as a dedicated input using the first feedback path, the register/latch feedback path is still available to the AND array. This path provides the capability of using the register/latch as a buried state register/latch. The other eight macrocells have a single feedback path to the AND array. This feedback is user-selectable as either an I/O pin or a register/latch feedback (see Figure 2a).

Each macrocell can provide true input/output capability. The user can select each macrocell register/latch to be driven by either the output generated by the AND-OR array or the I/O pin. When the I/O pin is selected as the input, the feedback path provides the register/latch input to the array. When used as an input, each macrocell is also user-programmable for registered, latched, or combinatorial input.

The PALCE29M16H has one dedicated CLK/$\overline{LE}$ pin and an I/CLK/$\overline{LE}$ pin. All macrocells have a programmable select to choose between these two pins as the clock or the latch enable signal. These signals are clock signals for macrocells configured as registers and latch enable signals for macrocells configured as latches. The polarity of these CLK/$\overline{LE}$ signals is also individually programmable. Thus different registers can be driven by different clocks and clock phases.

The Output-Enable mode of each of the macrocells can be selected by the user. The I/O pin can be configured as an output pin (permanently enabled) or as an input pin (permanently disabled). It can also be configured as a dynamic I/O controlled by the Output Enable pin or by two AND-XOR product terms which are available for each bank of four I/O Logic Macrocells.

I/O Logic Macrocell Configuration T-46-13-47

AMD's unique I/O macrocell offers major benefits through its versatile, programmable input/output cell structure, multiple clock choices, flexible Output Enable and feedback selection. Eight I/O macrocells with single feedback contain nine E^2 cells, while the other eight macrocells contain eight E^2 cells for programming the input/output functions (see Table 1).

E^2 cell S1 controls whether the macrocell will be combinatorial or registered/latched. S0 controls the output polarity (active-HIGH or active-LOW). S2 determines whether the input/output is a register or a latch. S3 allows the use of the macrocell as an input register/latch or as an output register/latch. It selects the direction of the data path through the register/latch. If connected to the usual AND-OR array output, the register/latch is an output connected to the I/O pin. If connected to the I/O pin, the register/latch becomes an input register/latch to the AND array using the feedback data path.

Programmable E^2 cells S4 and S5 allow the user to select one of the four CLK/$\overline{LE}$ signals for each macrocell. S6 and S7 are used to control Output Enable as pin controlled, two product term controlled, permanently enabled or permanently disabled. S8 is a feedback multiplexer for the macrocells with a single feedback path only.

Using the programmable E^2 cells S0-S8 various input and output configurations can be selected. Some of the possible configuration options are shown in Figure 3.

In the virgin erased state (charged, disconnected), an architectural cell is said to have a value of "1"; in the programmed state (discharged, connected to GND), an architectural cell is said to have a value of "0".

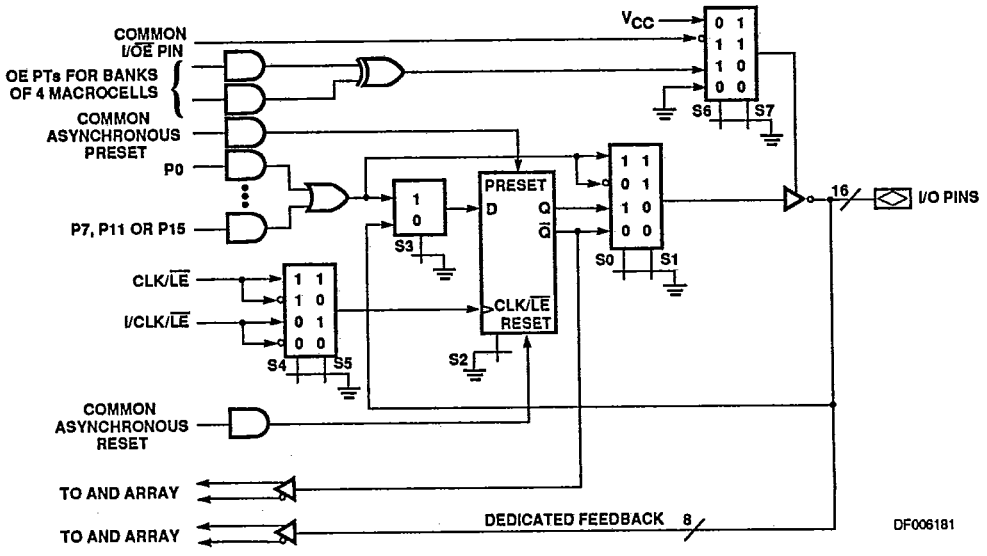


Figure 2a. PALCE29M16H Macrocell (Dual Feedback)

S3	I/O Cell
1	Output Cell
0	Input Cell

S2	Storage Element
1	Register
0	Latch

S1	Output Type
1	Combinatorial
0	Register/Latch

S0	Output Polarity
1	Active LOW
0	Active HIGH

S8	Feedback*
1	Register/Latch
0	I/O

* Applies to macrocells with single feedback only.

TC003961

Table 1. PALCE29M16H I/O Logic Macrocell Architecture Selections

S4	S5	Clock Edge/Latch Enable Level
1	1	CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE
1	0	CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE
0	1	I/CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE
0	0	I/CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE

S6	S7	Output Buffer Control
1	1	Pin-Controlled Three-State Enable
1	0	XOR PT-Controlled Three-State Enable
0	1	Permanently Enabled (Output only)
0	0	Permanently Disabled (Input only)

1 = Erased State (Charged or disconnected).

0 = Programmed State (Discharged or connected).

TC003972

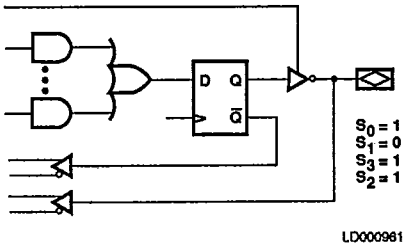
Table 1. PALCE29M16H I/O Logic Macrocell Clock Polarity and Output Enable Selections (Continued)

SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL

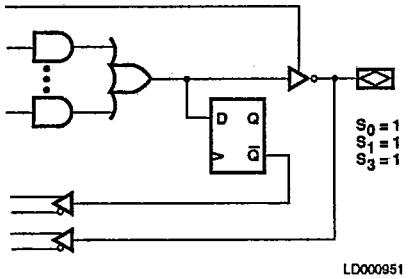
(For other useful configurations, please refer to the macrocell diagrams in Figure 2. All macrocell architecture cells are independently programmable).

T-46-13-47

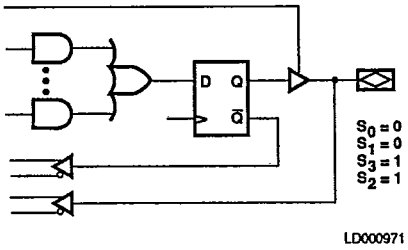
Output Registered/Active Low



Output Combinatorial/Active Low



Output Registered/Active High



Output Combinatorial/Active High

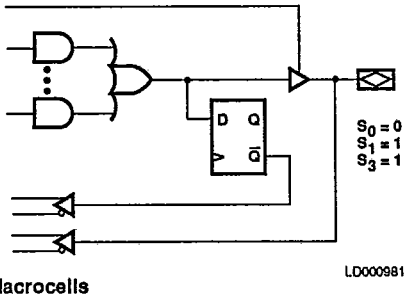
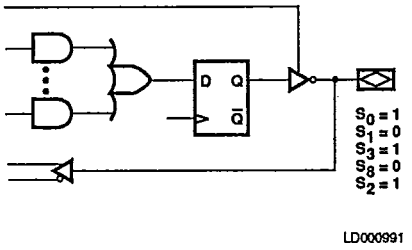
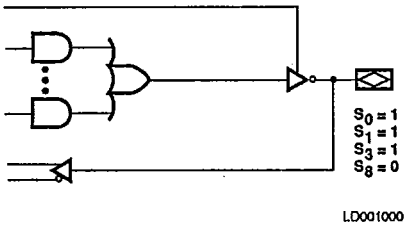


Figure 3a. Dual Feedback Macrocells

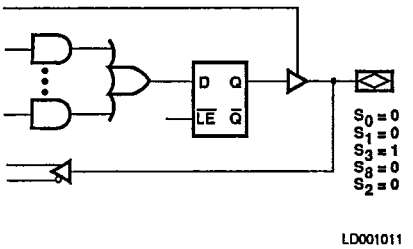
Output Registered/Active Low, I/O Feedback



Output Combinatorial/Active Low, I/O Feedback



Output Latched/Active High, I/O Feedback



Output Combinatorial/Active High, I/O Feedback

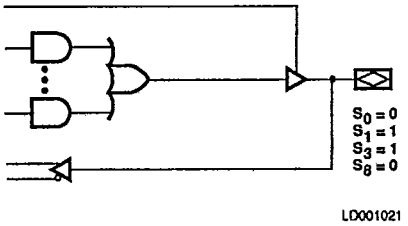
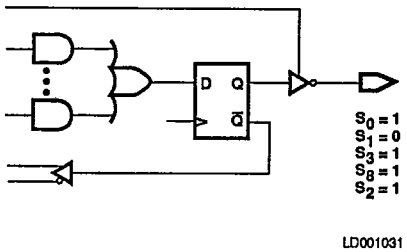


Figure 3b. Single Feedback Macrocells

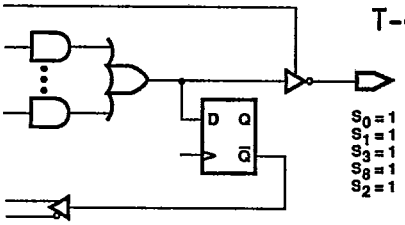
SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL (Continued)

Output Registered/Active Low, Register Feedback



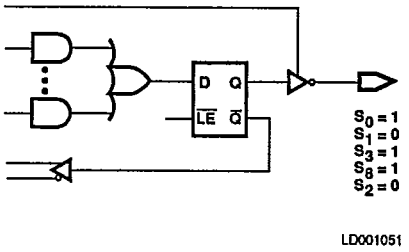
LD001031

Output Combinatorial/Active Low, Register Feedback



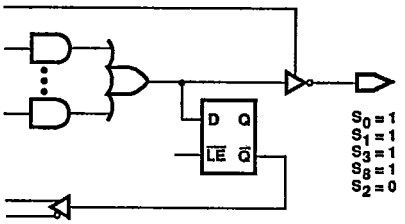
LD001041

Output Latched/Active Low, Latched Feedback



LD001051

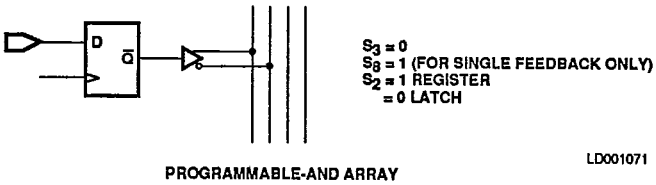
Output Combinatorial/Active Low, Latched Feedback



LD001061

Figure 3b. Single Feedback Macrocells (Continued)

Input Registered/Latched



LD001071

Figure 3c. All Macrocells

DESIGNED-IN TESTABILITY AND DEBUGGING

PRELOAD

To simplify testing, the PALCE29M16H is designed with PRELOAD circuitry that provides an easy method for testing logical functionality. Both product term controlled and supervoltage-enabled PRELOAD modes are available. This offers even more test capability than previously implemented in AMD's PAL devices. The TTL-level PRELOAD product term can be useful during debugging, where supervoltages may not be available.

PRELOAD allows any arbitrary state value to be loaded into the registers/latches of the device. A typical functional-test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device's inputs into any arbitrary "present input" value. Once this is done, the state machine is clocked into a new state, or "next state", which can be checked to validate the transition from the "present state". In this way any transition can be checked.

Since PRELOAD can provide the capability to go directly to any desired arbitrary state, test sequences may be greatly shortened. Also, all possible states can be tested, thus greatly reducing test time and development costs and guaranteeing proper in-system operation.

Observability

The output register/latch observability product term, when asserted, suppresses the combinatorial output data from appearing on the I/O pin and allows the observation of the contents of the register/latch on the output pin for each of the logic macrocells. This unique feature allows for easy debugging and tracing of the buried state machines. In addition, a capability of supervoltage observability is also provided.

Security Cell

A security cell is provided on each device to prevent unauthorized copying of the user's proprietary logic design. Once programmed, the security cell disables the programming, verification, PRELOAD, and the observability modes. The only way to erase the protection cell is by charging the entire array and architecture cells, in which case no proprietary design can be copied. (This cell should be programmed only after the rest of the device has been completely programmed and verified.)

DIP (PLCC) Pinouts

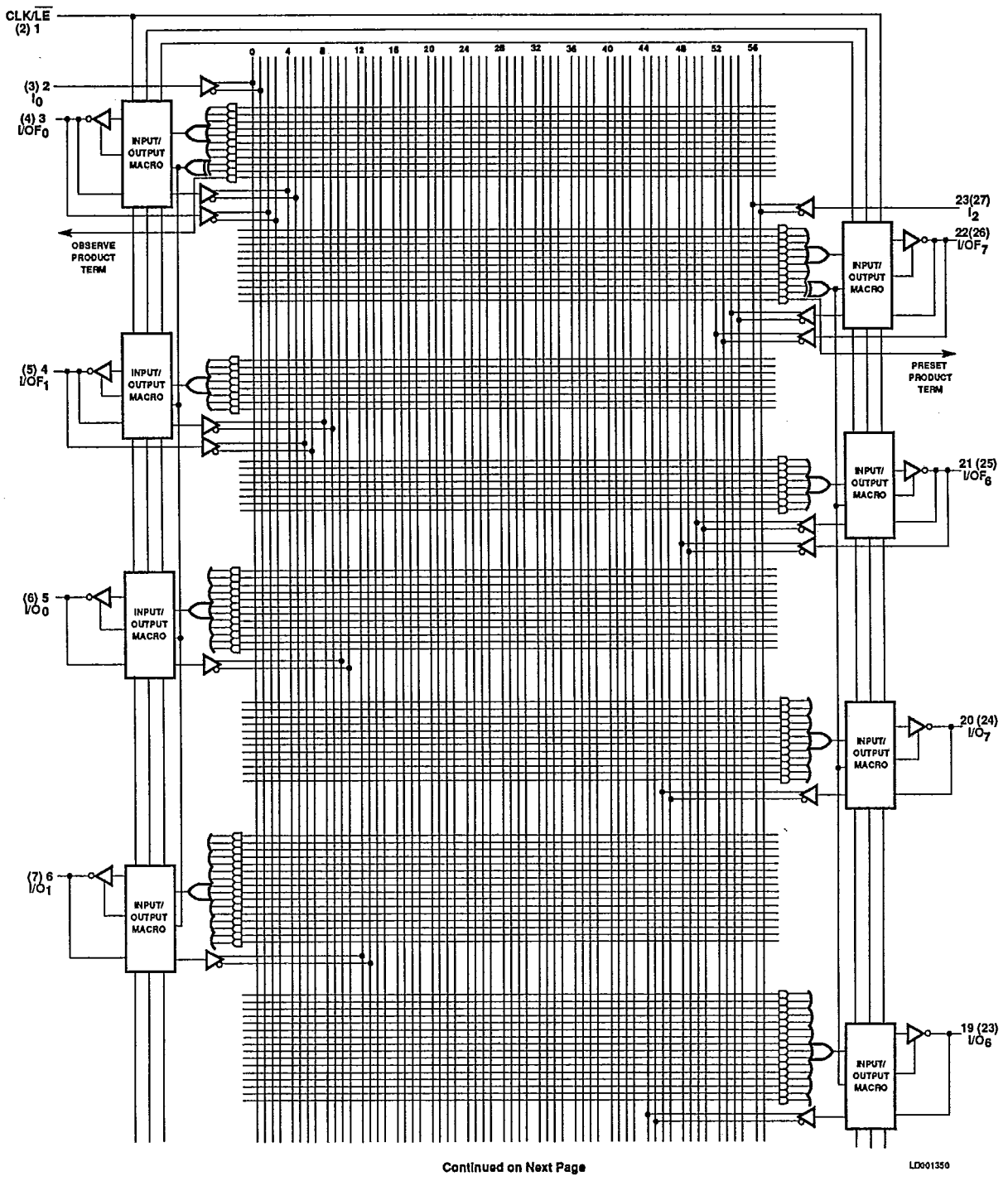


Figure 4. Logic Diagram

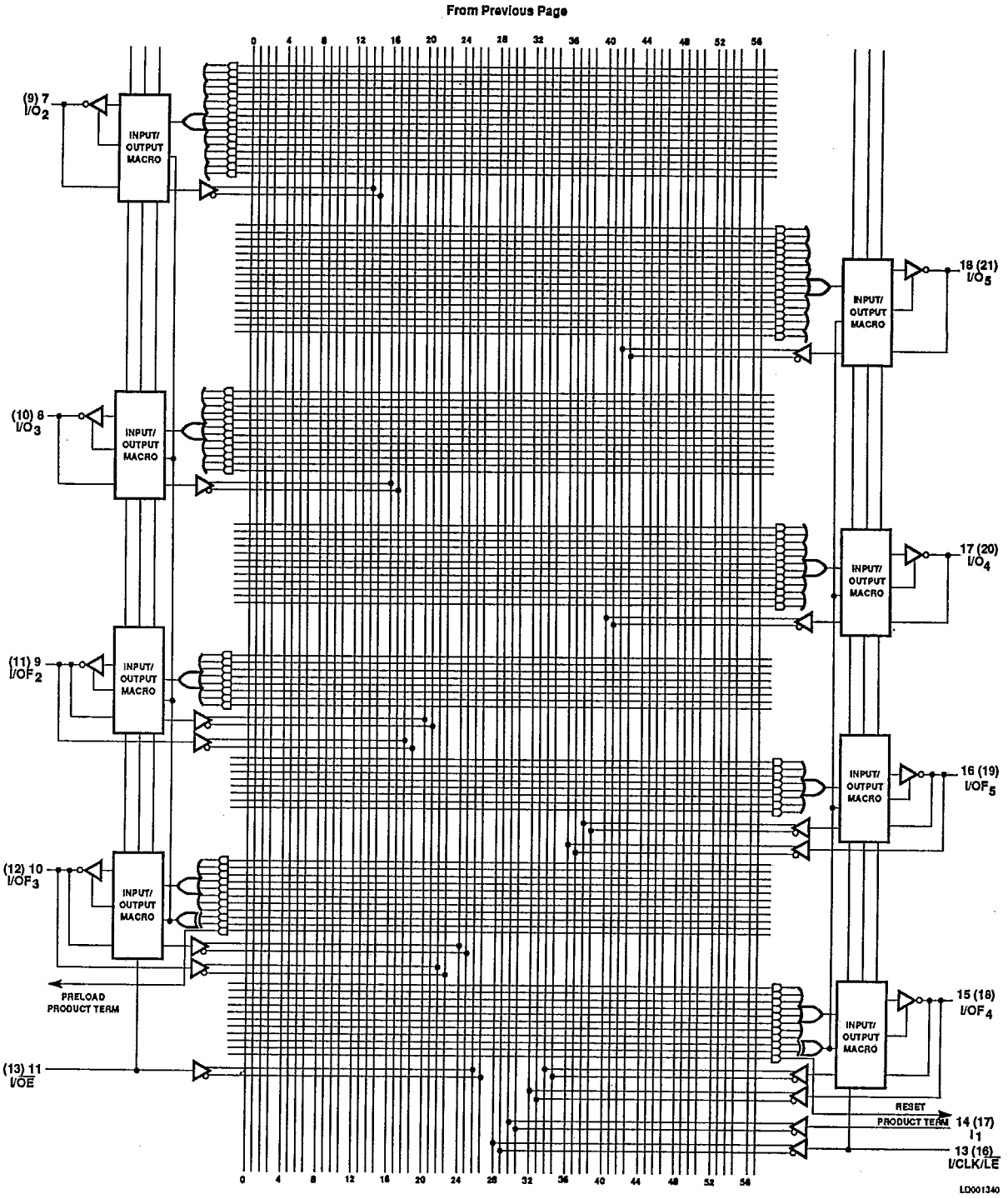


Figure 4. Logic Diagram (Continued)

ABSOLUTE MAXIMUM RATINGS

Storage temperature ..... -65°C to +150°C
Ambient temperature under bias ..... -55°C to +125°C
Supply voltage with respect to ground ..... -0.5 V to +7.0 V
DC output voltage ..... -0.5 V to V_{CC} +0.5 V
DC input voltage (except pin I/$\overline{OE}$) ..... -0.5 V to V_{CC} +0.5 V
DC input voltage (pin I/$\overline{OE}$) ..... -0.6 V to +16 V
DC input current ..... -1 mA to +1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) devices
Temperature (T_A) operating free air ..... 0°C to +75°C
Supply voltage (V_{CC}) ..... +4.75 V to +5.25 V

T-46-13-47

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS Over operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} I_{OH} = -2 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 6 mA		0.5	V
			I_{OL} = 4 mA		0.33	
			I_{OL} = 20 µA		0.1	
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for all Inputs (Note 1)			0.8	V
I_I	Input Leakage Current	V_{IN} = 0 to 5.5 V, V_{CC} = Max.		-10	10	µA
I_O	Output Leakage Current (Note 3)	V_{IN} = 0 to 5.5 V, V_{CC} = Max.		-10	10	µA
I_{CC}	Supply Current	Outputs Open (I_O = 0 mA), V_{IN} = 0 V			100	mA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_O = 0.5 V (Note 2)		-30	-90	mA

Notes:
1. These are absolute values with respect to the ground pin on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
2. No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
3. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.0 V, T_A = 25°C V_{IN} = 0 V at f = 1 MHz	5	pF
C_{OUT}	Output Capacitance		8	

Notes:
1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

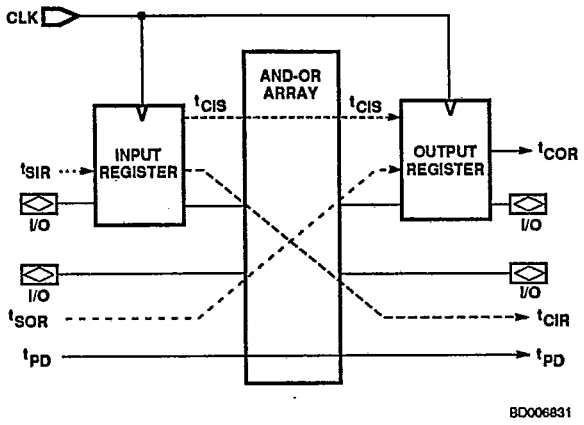
SWITCHING CHARACTERISTICS

T-46-13-47

Over commercial range unless otherwise specified; all values are determined under the loading of one TTL gate and a capacitance of 35 pF

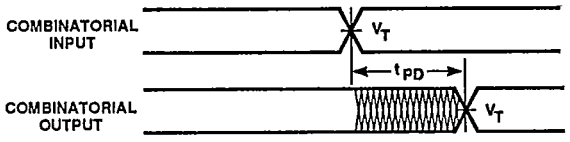
REGISTERED OPERATION

Parameter Symbol	Parameter Description	-25		-35		Unit
		Min.	Max.	Min.	Max.	
Combinatorial Output						
t_{PD}	Input or I/O Pin to Combinatorial Output		25		35	ns
Output Register						
t_{SOR}	Input or I/O Pin to Output Register Setup	15		20		ns
t_{COR}	Output Register Clock to Output		15		20	ns
t_{HOR}	Data Hold Time for Output Register	0		0		ns
Input Register						
t_{SIR}	I/O Pin to Input Register Setup	2		4		ns
t_{CIR}	Register Feedback Clock to Combinatorial Output		28		36	ns
t_{HIR}	Data Hold Time for Input Register	6		8		ns
Clock and Frequency						
t_{CIS}	Register Feedback to Output Register/Latch Setup	20		30		ns
f_{MAX}	Maximum Frequency (Pin Driven) $1/(t_{SOR} + t_{COR})$		33.3		25	MHz
f_{MAXI}	Maximum Internal Frequency (Pin Driven) $1/t_{CIS}$		50		33.3	MHz
t_{CWH}	Pin Clock Width HIGH	8		12		ns
t_{CWL}	Pin Clock Width LOW	8		12		ns

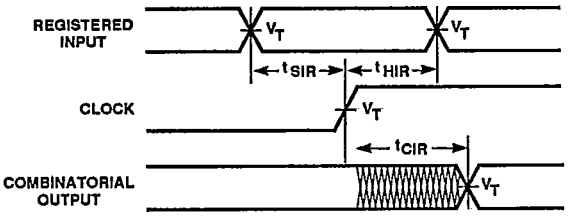


Input/Output Register Specs (Pin CLK Reference)

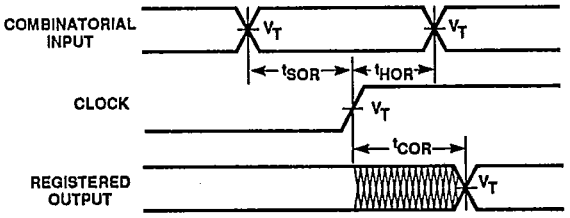
SWITCHING WAVEFORMS



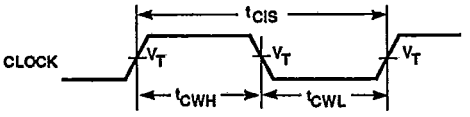
Combinatorial Output



Input Register



Output Register



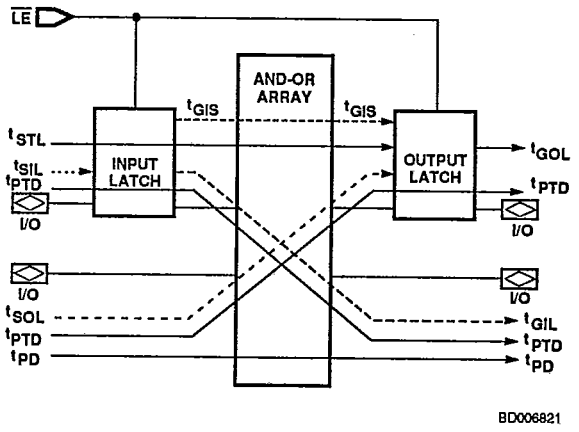
Clock Width

SWITCHING CHARACTERISTICS (Continued)

Over commercial range unless otherwise specified; all values are determined under the loading of one TTL gate and a capacitance of 35 pF

LATCHED OPERATION

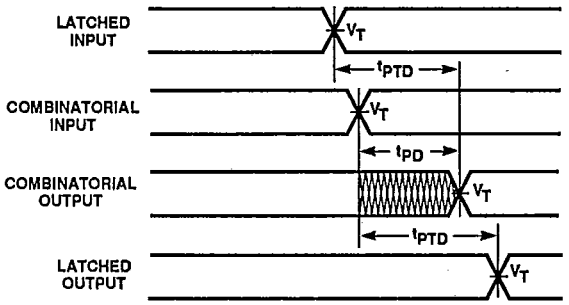
Parameter Symbol	Parameter Description	-25		-35		Unit
		Min.	Max.	Min.	Max.	
Combinatorial Output						
t_{PD}	Input or I/O Pin to Combinatorial Output		25		35	ns
t_{PTD}	Input or I/O Pin to Output via One Transparent Latch		28		36	ns
Output Latch						
t_{SOL}	Input or I/O Pin to Output Latch Setup	15		20		ns
t_{GOL}	Latch Enable to Transparent Mode Output		15		20	ns
t_{HOL}	Data Hold Time for Output Latch	0		0		ns
t_{STL}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	18		25		ns
Input Latch						
t_{SIL}	I/O Pin to Input Latch Setup	2		4		ns
t_{GIL}	Latch Feedback, Latch Enable Transparent Mode to Combinatorial Output		28		36	ns
t_{HIL}	Data Hold Time for Input Latch	6		8		ns
Latch Enable						
t_{GIS}	Latch Feedback to Output Register/Latch Setup	20		30		ns
t_{GWH}	Pin Enable Width HIGH	8		12		ns
t_{GWL}	Pin Enable Width LOW	8		12		ns



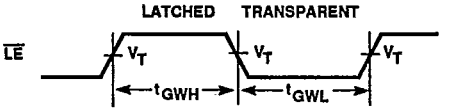
Input/Output Latch Specs (Pin $\overline{LE}$ Reference)

SWITCHING WAVEFORMS (Continued)

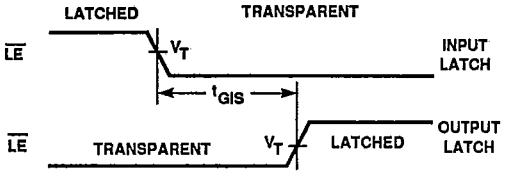
T-46-13-47



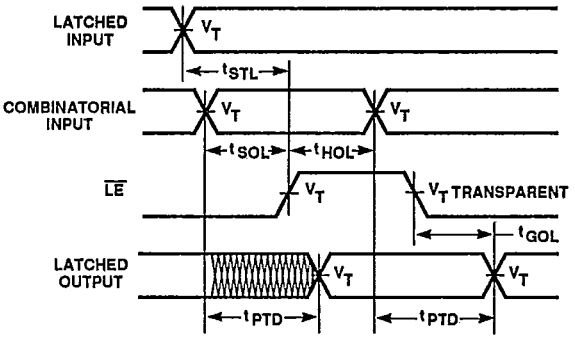
Latch (Transparent Mode)



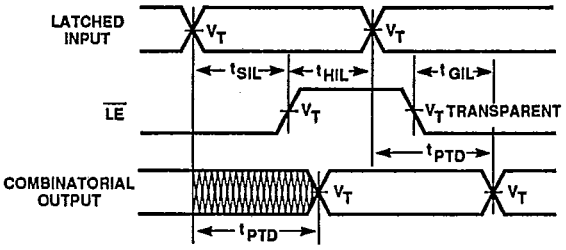
$\overline{LE}$ Width



Input and Output Latch Relationship



Output Latch



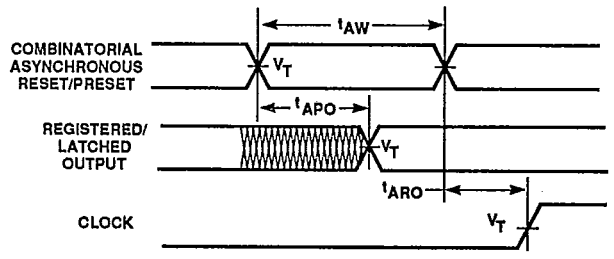
Input Latch (Pin $\overline{LE}$)

RESET/PRESET, ENABLE

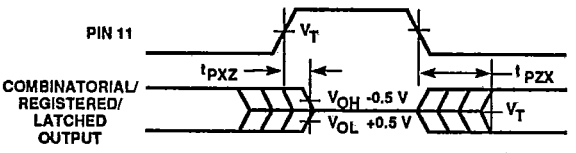
Parameter Symbol	Parameter Description	-25		-35		Unit
		Min.	Max.	Min.	Max.	
t_{APO}	Input or I/O Pin to Output Register/Latch RESET/PRESET		30		40	ns
t_{AW}	Asynchronous RESET/PRESET Pulse Width	15		20		ns
t_{ARO}	Asynchronous RESET/PRESET to Output Register/Latch Recovery	15		20		ns
t_{ARI}	Asynchronous RESET/PRESET to Input Register/Latch Recovery	12		15		ns
Output Enable Operation						
t_{PZX}	I/$\overline{OE}$ Pin to Output Enable		20		30	ns
t_{PXZ}*	I/$\overline{OE}$ Pin to Output Disable		20		30	ns
t_{EA}	Input or I/O to Output Enable via PT		25		35	ns
t_{ER}*	Input or I/O to Output Disable via PT		25		35	ns

* Output disable times do not include test load RC time constants.

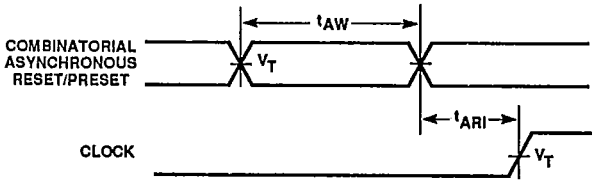
SWITCHING WAVEFORMS (Continued)



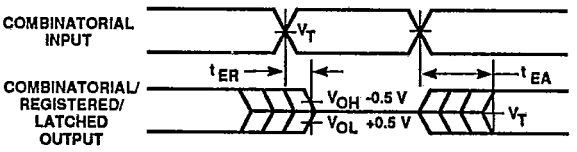
Output Register/Latch Reset/Preset



Pin 11 to Output Disable/Enable



Input Register/Latch Reset/Preset



Input to Output Disable/Enable

POWER-UP RESET

The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		100	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics table		
t_W	Clock Width			
t_R	V_{CC} Rise Time	500		µs

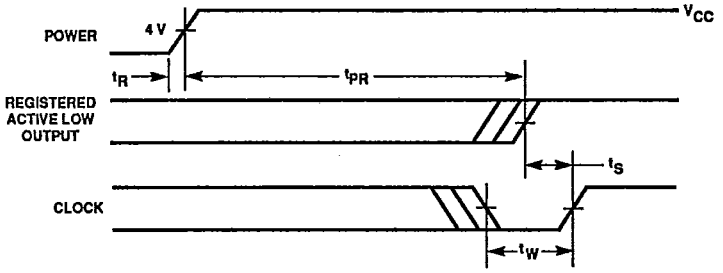
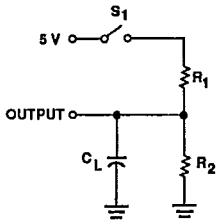
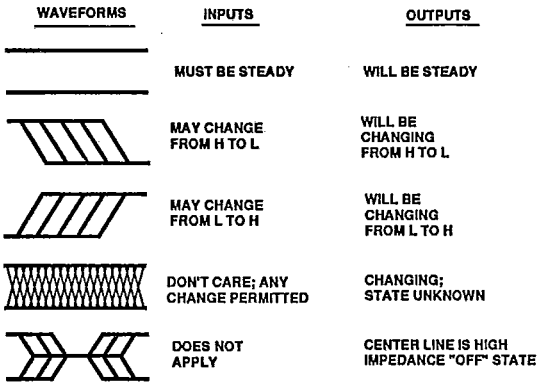


Figure 5. Power-Up Reset Waveform

SWITCHING TEST CIRCUIT



KEY TO SWITCHING WAVEFORMS



Specification	Switch S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{GO}	Closed	35 pF	620 Ω	390 Ω	1.5 V
t_{EA}, t_{PZX}	Z→H: open Z→L: closed	35 pF	620 Ω	390 Ω	1.5 V
t_{ER}, t_{PXZ}	H→Z: open L→Z: closed	5 pF	620 Ω	390 Ω	H→Z: V_{OH} -0.5 V L→Z: V_{OL} +0.5 V

PRELOAD and OBSERVABILITY

The PALCE29M16H has special preload and observability modes designed in. The PRELOAD mode is very useful during structured vector testing after programming, while the observe mode allows the designer to see the contents of any buried registers.

The PRELOAD waveform is shown in Figure 6. The PRELOAD registers mode is selected with the mode-select pins, the desired data to be loaded into the registers is placed on the appropriate I/O pins, and a positive pulse on pin 1 is applied. This clocks the new values into the registers, and the device can then be returned to normal operating mode.

The observability function allows the user to observe the outputs of all sixteen registers. To use the observability mode, simply select the observe registers mode with the mode-select pins. The register output is automatically selected (combinatorial mode is off), and the output will be the true side of the register (Q). The data will be present as long as the mode-select pins access the observe mode (even if pin 11 goes LOW, the output pins will still retain the data out of the registers). To exit the observe mode, simply change the mode-select pins while pin 11 is still at V_{PP}.

During observability, pin 1 should remain LOW. If pin 1 goes HIGH, the device will interpret this as a clock signal, and the previous data may be lost. As long as pin 1 remains LOW, the state of the registers will not change when going from normal-mode operation to observe mode or back.

T-46-13-47

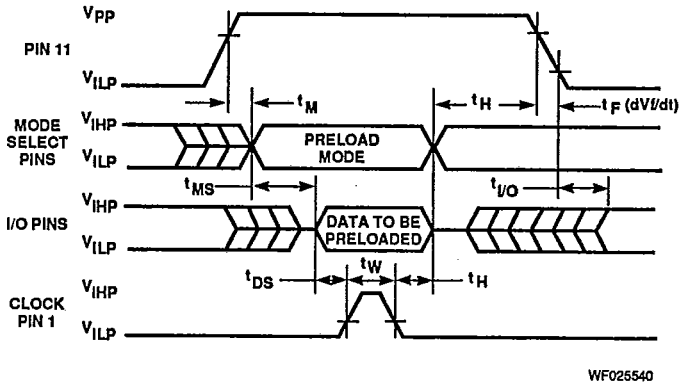


Figure 6. PRELOAD Waveform

PRELOAD DC ELECTRICAL CHARACTERISTICS (T_A = 25°C ±5°C)

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{PP}	PRELOAD Voltage	14.5	15.0	15.5	V
V_{ILP}	Input LOW Level During Prog/Verify	0	0	0.5	V
V_{IHP}	Input HIGH Level During Prog/Verify	3.0	4.0	V_{CC}	V
V_{OL}	Verify LOW		0.2	0.5	V
V_{OH}	Verify HIGH	2.4	3.4		V

Note: AC undershoot on any input should be limited to -1 V.

Table 2.

	Pin 23	Pin 14	Pin 13	Pin 2
Preload	L	H	H	L
Observe	H	L	H	H

Table 3. Mode Pins

PRELOAD AC ELECTRICAL CHARACTERISTICS (T_A = 25°C ±5°C)

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_M	Setup Before Applying Mode	50	50		µs
t_{MS}	Mode Setup Prior to Applying Data	1.0	1.0*		µs
t_{DS}	Data Setup Prior to Applying PRELOAD Latch Pulse	1.0	1.0*		µs
t_H	Data/Mode Hold After Latch Pulse	1.0	1.0*		µs
t_W	Data Latch Pulse Width	1.0	1.0*		µs
$t_{I/O}$	I/O Valid After Pin 11 Drops from V_{PP} to TTL Levels			100	µs
dVr/dt	V_{PP} Rising Slew Rate (Pin 11)	10		100	V/µs
dVf/dt	V_{PP} Falling Slew Rate (Pin 11)		2.0	3.0	V/µs

* Recommended value is as close to 1.0 µs plus tolerance as practical, but not less than 1.0 µs.

Table 4.

ENDURANCE CHARACTERISTICS

All PALCE29M16H devices are given multiple erase cycles (endurance cycles) at the factory.

Parameter Symbol	Parameter Description	Value	Unit	Test Conditions
t_{DR}	Minimum Pattern Data Retention Time	10	Years	Maximum Storage Temperature
N	Minimum Reprogramming Cycles	100	Cycles	Operating Conditions

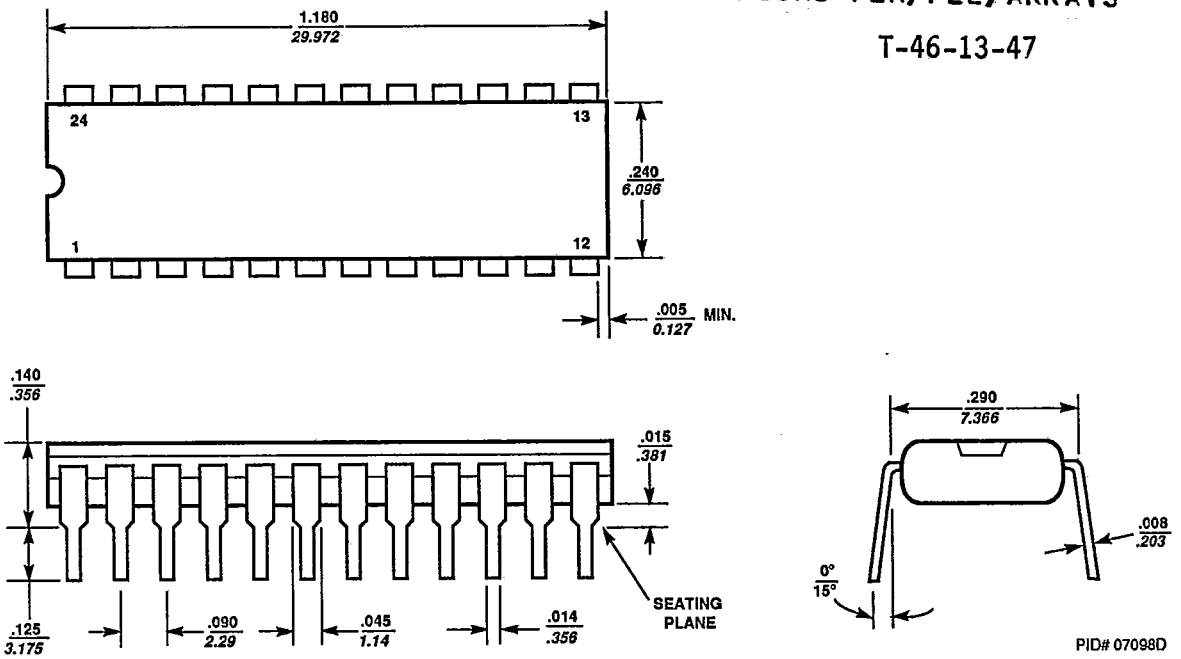
PROGRAMMERS/DEVELOPMENT SYSTEMS (Subject to change)

T-46-13-47

MANUFACTURER	PROGRAMMER CONFIGURATION		
	Programmer Model	Personality Module	Socket Adapter
Adams MacDonald 800 Airport Road Monterey, CA 93940 (408) 373-3607		Contact Manufacturer	
Data I/O Corporation 10525 Willows Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	System 29 Model 60A or 60H-V10 UniSite™ 40 Rev 2.3	LogicPak™ 303A-V04	303A-011A/B V04 Family/Pinout 604B
Digelec Inc. 22736 Vanowen Street Canoga Park, CA 91307 (800) 367-8750 or (818) 887-3755		Contact Manufacturer	
Kontron Electronics Inc. 630 Clyde Avenue Mountain View, CA 94039-7230 (800) 227-8834 or (415) 965-7020		Contact Manufacturer	
Logical Devices Inc. 1201 Northwest 65th Place Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967		Contact Manufacturer	
Microprоss Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq (20) 47.90.40		Contact Manufacturer	
Stag Microsystems Inc. 1600 Wyatt Drive, Suite 3 Santa Clara, CA 95054 (408) 988-1118		Contact Manufacturer	
Varix Corporation 1210 E. Campbell Road, Suite 100 Richardson, TX 75081 (214) 437-0777		Contact Manufacturer	

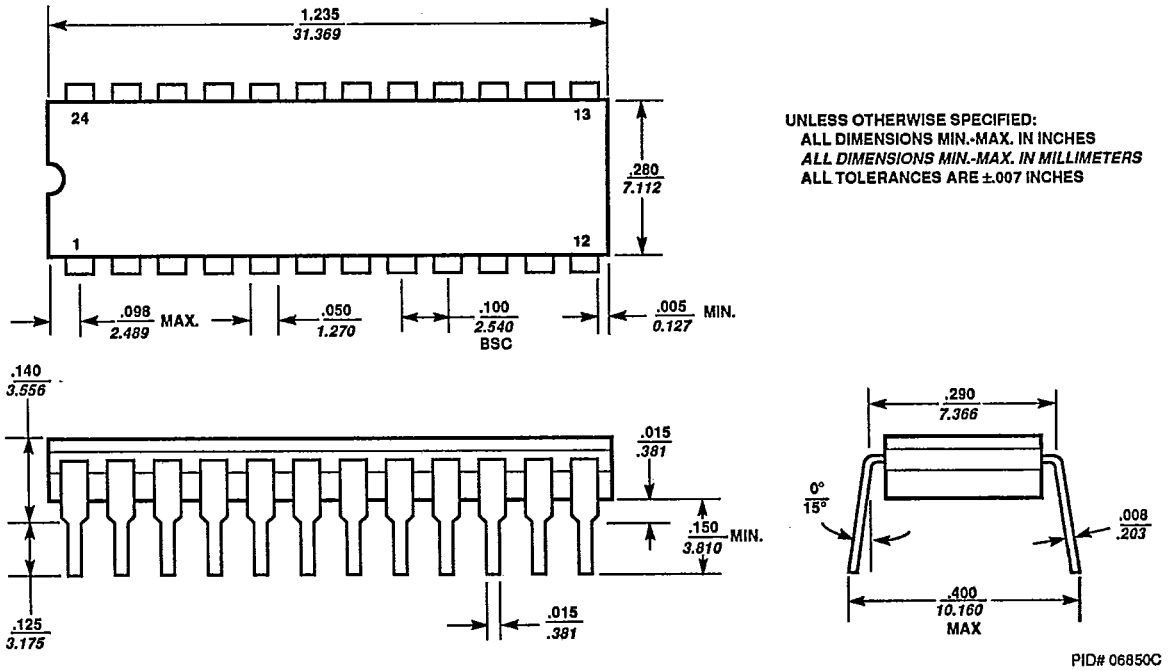
MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEM
Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94088-3453 (800) 222-9323	PALASM®2 Software, rev. 2.24 and later PLPL Software, rev. 2.2 and later
Data I/O Corporation 10525 Willows Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	ABEL™ Software, rev. 3.0 and later
Logical Devices Inc. 1201 Northwest 65th Place Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	CUPL™ Software, rev. 2.15A and later

LogicPak™, UniSite™, and ABEL™ are trademarks of Data I/O Corporation. CUPL™ is a trademark of Logical Devices Inc.



PID# 07098D

CD3024

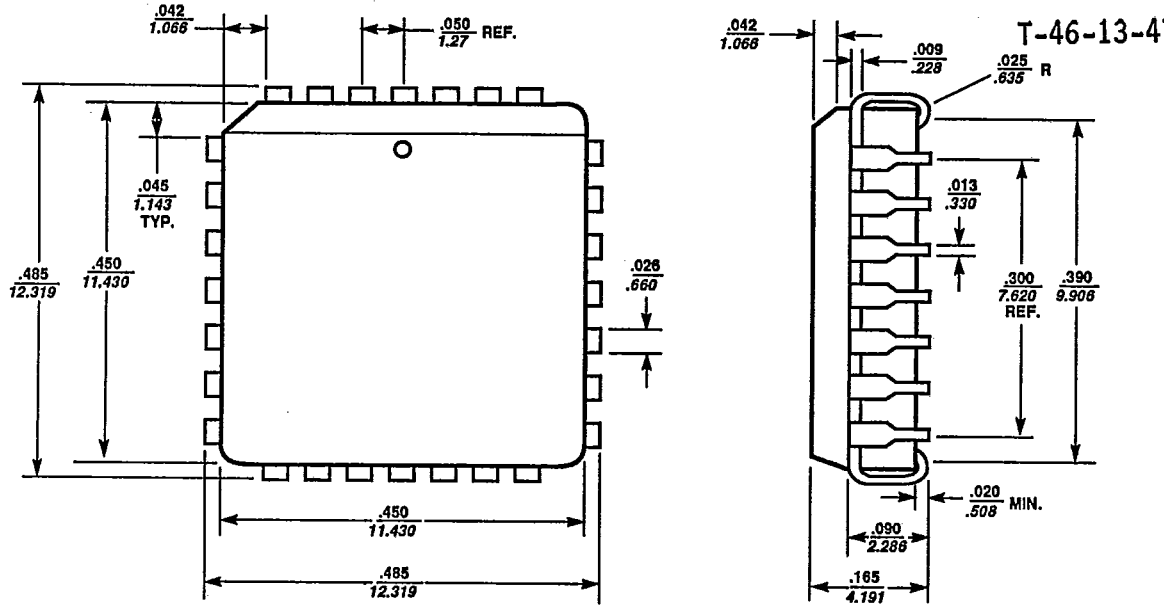


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES

PID# 06850C

*For reference only.

PHYSICAL DIMENSIONS



PID# 06751E

UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES