A10M20A Mask Programmed Gate Array

T-46-19-09

Preliminary

Features

- High Gate Count: 2000 gate array gates (6000 PLD/LCA equivalent gates)
- Pin-for-Pin Compatible with Actel's A1020A FPGA at Lower Cost
- Easy Conversion From FPGA to Mask Programmed Gate Array (MPGA)
- Re-routing Not Required for FPGA to MPGA Conversion
- Automatic Test Generation (ATG) Eliminates Test Vector Generation
- ATG Vectors Provide 100% Test Coverage for all Detectable Faults
- 35–70% Faster than Programmable A1020A FPGA
- Gate Array Architecture Allows Completely Automatic Place and Route
- Short Lead Times to Prototypes and Production
- Low-Power CMOS Technology
- System Level Performance to 50 MHz
- Toggle Rates to 120 MHz
- I/O Drive to 8 mA
- Nonvolatile, Permanent Programming
- Built-In Clock Distribution Network

Product Profile

Device	A10M20A
Capacity	
Gate Array Equivalent Gates	2,000
PLD/LCA Equivalent Gates	6,000
TTL Equivalent Packages	50
20-Pin PAL Equivalent Packages	15
Logic Modules	547
Flip-Flops (maximum)	273
Routing Resources	
Horizontal Tracks/Channel	25
Vertical Tracks/Column	13
User I/Os (maximum)	69
Packages	68-pin PLCC 84-pin PLCC 100-pin PQFP
CMOS Process	1.2 µm

Description

The Actel A10M20A Mask Programmed Gate Array (MPGA) offers a lower cost, faster alternative to the A1020A Field Programmable Gate Array (FPGA). These A10M20A MPGAs are pin-for-pin compatible with the A1020A FPGAs. The devices are manufactured in 1.2 micron, two-level metal CMOS and the Actel PLICE® antifuse is replaced by a metal connection via. Actel's unique architecture offers gate array flexibility and high performance.

Actel's MPGA provides automatic test vector generation and 100% test coverage for all detectable faults. This procedure is automatic. Additional features include an on-chip clock driver with a hard-wired distribution network. The on-chip clock driver provides efficient clock distribution with minimum skew.

The user-definable I/Os can drive TTL and CMOS levels.

The Action Logic System

The MPGA is supported by Actel's Action Logic™ System, which allows logic design to be implemented with minimum effort. The Action Logic System (ALS) interfaces with the resident CAE platform to provide a complete gate array design environment for the ACT 1 MPGA. It allows schematic capture, simulation, fully automatic place and route, timing verification, and device programming. The Action Logic System also provides timing and simulation information for the MPGA device. The Action Logic System is supported on the following platforms: 386/486 PC, and Sun®, HP® and Apollo® workstations. It provides CAE interfaces to the following design environments: Valid™, Viewlogic®, Mentor Graphics™, HP DCS and OrCad™.

The MPGA offers the user the ability to move into volume production much faster than with conventional masked gate arrays. Actel produces prototype devices directly from customer generated design files. The user can employ the Action Logic System to perform all schematic capture, pre-route simulation, place and route, and post-route back-annotated simulation. Since there are no additional routes or simulations needed at the vendor's site, there are no extra CPU charges. This gives the user the opportunity to fully determine the functionality of the device prior to paying any NRE development charges.

Device Structure

The A10M20A MPGA's basic structure is similar to the A1020A FPGA. Logic modules are arranged in horizontal rows separated by horizontal interconnect tracks, with vertical interconnect tracks running over the logic modules. The FPGA has PLICE antifuses, located at the intersection of the horizontal and vertical tracks, which connect its logic module inputs and outputs. During the programming cycle, the software addresses and programs the connections required by the circuit application. The MPGA is designed so that all programmable antifuses are removed.

Antifuses are replaced by low-impedance metal vias. Metal via connections are made according to specific customer designs.

The Actel Logic Module

The Actel Logic Module is an eight-input, one-output logic circuit chosen for its wide range of functions and its efficient use of interconnect routing resources. All of the functions available in the ACT 1 FPGA family are available for the A10M20A device.

The logic module implements the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function has many versions, due to different combinations of active-low inputs. The logic module also implements a variety of D-latches, an exclusivity function, AND-ORs and OR-AND relationships. Dedicated hard-wired latches or flip-flops are not required, since latches and flip-flops may be constructed from logic modules, wherever needed in the application.

I/O Buffers

Each I/O pin can be configured as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications.

Device Organization

The MPGA consists of a matrix of logic modules arranged in rows separated by wiring channels. The number of logic modules and routing resources is identical for the A1020A FPGA and the A10M20A MPGA (14 rows by 44 columns, 547 logic modules and 69 I/O modules). The MPGA has ATG peripheral circuits for generating test vectors. Routing channels, which contain 22 horizontal segmented metal tracks, are between the rows of logic modules. Vertical routing is provided by 13 vertical tracks per logic module column. Metal via connections are made between the routing tracks to implement a customer's design.

Automatic Test Generation

ATG test vectors are generated automatically to verify user design and interconnect wiring, with 100% fault coverage. Testing is facilitated by testability structures incorporated in the MPGA logic module.

Greater details concerning the methods used to generate the ATG test vectors can be found in the technical paper entitled "Array Architecture for ATG with 100% Fault Coverage," included in this datasheet.

Device Performance

Temperature, Voltage and Processing Effects

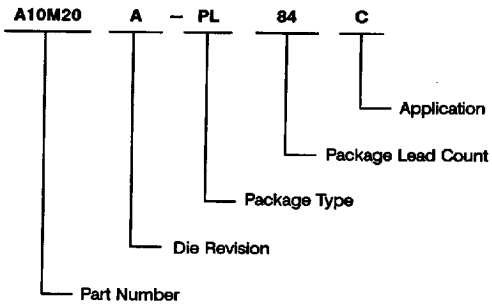
Worst-case delays for the A1020A FPGA device and the A10M20A MPGA device are calculated in the same manner as for conventional masked gate arrays. A typical delay parameter is multiplied by a derating factor to account for temperature, voltage, and processing effects.

The total derating factor from typical to worst-case for the A10M20A MPGA is 1.54 to 1.

Logic Module Size

The logic module size also affects performance. A conventional masked gate array cell with four transistors usually implements only one logic level. In more complex logic modules (similar to the complexity of a gate array macro), of both the A1020A FPGA, and the A10M20A MPGA, it is possible to implement multiple logic levels within a single module. This eliminates inter-level wiring and associated RC delays.

Ordering Information



Product Plan

Package Type	Lead Count	Application
PL	68	C
PL	84	C
PQ	100	C

PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flatpack
C = Commercial

Device Resources

Device Series	Logic Modules	Gates	User I/Os		
			68-Pin	84-Pin	100-Pin
A10M20A	547	2000	57	69	69

Absolute Maximum Ratings

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	-0.5 to +7.0	Volts
V_I	Input Voltage	-0.5 to V_{CC} +0.5	Volts
V_O	Output Voltage	-0.5 to V_{CC} +0.5	Volts
I_{IK}	Input Clamp Current	±20	mA
I_{OK}	Output Clamp Current	±20	mA
I_{OK}	Continuous Output Current	±25	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.

Recommended Operating Conditions

Parameter	Commercial	Units
Temperature Range[1]	0 to +70	°C
Power Supply Tolerance	±5	%V_{CC}

Note:
1. Ambient temperature (T_A).

Power Dissipation

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The following formula is used to calculate total device dissipation.

Total Device Power (mW) = (0.067 x N x F1) + (0.028 x M x F2) + (0.80 x P x F3)

Where:

F1 = Average logic module switching rate in MHz.

F2 = CLKBUF macro switching rate in MHz.

F3 = Average I/O module switching rate in MHz.

M = Number of logic modules connected to the CLKBUF macro.

N = Total number of logic modules used in the design (including M).

P = Number of outputs loaded with 50 pF.

The average switching rate of logic modules and I/O modules is some fraction of the device operating frequency (usually CLKBUF). Logic modules and I/O modules switch states (from low-to-high or from high-to-low) only if the input data changes when the module is enabled. A conservative estimate for average logic module and I/O module switching rates (variables F1 and F3, respectively) is 10% of device clock driver frequency.

If the CLKBUF macro is not used in the design, eliminate the second term (including F2 and M variables) from the formula.

Sample A10M20A Power Dissipation Calculation

This sample design uses 85% of available logic modules on the A10M20A-series device (.85 x 547 = 465 logic modules). The design contains 104 flip-flops (208 logic modules). The design's operating frequency is 16 MHz. The CLKBUF macro drives the clock network. Logic modules and I/O modules switch states at approximately 10% of the clock frequency rate (.10 x 16 MHz = 1.6 MHz). Sixteen outputs are loaded with 50 pF.

To summarize the design described above: N = 465; M = 208; F2 = 16; F1 = 1.6; F3 = 1.6; P = 16. Total device power can be calculated by substituting these values for variables in the device dissipation formula.

Total device power for this example =

(0.067 x 465 x 1.6) + (0.028 x 208 x 16) + (0.80 x 16 x 1.6) = 164 mW

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Electrical Specifications

Parameter		Min.	Max.	Units
V_{OH}[1]	(I_{OH} = -8 mA)	2.4		V
	(I_{OH} = -4 mA)	3.84		V
V_{OH}[1]	(I_{OL} = 8 mA)		0.5	V
	(I_{OL} = 4 mA)		0.33	V
V_{IL}		-0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500	ns
C_{IO} I/O Capacitance[2, 3]			10	pF
Standby Current, I_{CC}[4]			1	mA
Leakage Current[5]		-10	10	µA
I_{OS} Output Short Circuit Current[6]	(V_O = V_{CC})	20	140	mA
	(V_O = GND)	-10	-100	mA

Notes:
1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. Typical standby current = 300 µA. All outputs unloaded. All inputs = V_{CC} or GND.
5. V_O, V_{IN} = V_{CC} or GND.
6. Only one output tested at a time. Min. at V_{CC} = 4.5 V; Max. at V_{CC} = 5.5 V.

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown in the following table, with two different air flow rates.

Package Type	Pin Count	θjc	θja Still air	θja 300 ft/min.	Units
Plastic J-leaded Chip Carrier	68	13	45	35	°C/W
	84	12	44	33	°C/W
Plastic Flatpack	100	13	55	50	°C/W

Timing Characteristics

Timing is design dependent; actual delay values are determined after place and route of the design using the ALS Timer utility. The following delay values use statistical estimates for wiring delays based on 85% to 90% module utilization. Device utilization above 95% will result in performance degradation.

The A10M20A MPGA is 35–70% faster than the A1020A FPGA because the antifuse is replaced by a metal via connection. The designer needs to be aware of these timing differences when converting from an A1020A FPGA to the A10M20A MPGA. These differences can be quickly analyzed at the customer's facility using ALS.

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Logic Module Timing

V_{CC} = 5.0 V; T_A = 25°C; Process = Typical

Single Logic Module Macros (e.g., most gates, latches, multiplexors)[1]

Parameter	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD}	Typical	4.3	4.4	4.5	4.6	4.8	ns

Dual Logic Module Macros (e.g., adders, wide input gates)[1]

Parameter	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD}	Typical	6.9	7.0	7.1	7.3	7.6	ns

Sequential Element Timing Characteristics

Parameter		Fan-Out					Units
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{SU}	Set Up Time, Data Latches	2.7	2.8	3.0	3.3	3.8	ns
t_{SU}	Set Up Time, Flip-Flops	2.8	2.8	2.8	2.8	2.8	ns
t_H	Hold Time	0	0	0	0	0	ns
t_W	Pulse Width, Minimum[2]	6.0	6.3	6.5	7.0	8.0	ns
t_{CQ}	Delay, Typical Net	3.7	3.8	3.9	4.0	4.2	ns
t_{PRE}	Asynchronous Preset to Q	4.3	4.4	4.5	4.6	4.8	ns
t_{CLR}	Asynchronous Clear to Q	4.3	4.4	4.5	4.6	4.8	ns

Notes:
1. Most flip-flops exhibit single module delays.
2. Minimum pulse width, t_W, applies to CLK, PRE, and CLR inputs.

I/O Buffer Timing

PRELIMINARY DATA

V_{CC} = 5.0 V; T_A = 25°C; Process = Typical

INBUF Macros

Parameter	From – To	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PHL}	Pad to Y	2.2	2.3	2.3	2.4	2.6	ns
t_{PLH}	Pad to Y	2.1	2.1	2.2	2.2	2.4	ns

CLKBUF (High Fan-Out Clock Buffer) Macros

Parameter	FO = 40	FO = 160	FO = 320	Units
t_{PLH}	4.1	4.1	4.1	ns
t_{PHL}	4.3	4.3	4.3	ns

Notes:

1. A clock balancing feature is provided to minimize clock skew.
2. There is no limit to the number of loads that may be connected to the CLKBUF macro.

OUTBUF, TRIBUFF & BIBUF Macros

C_L = 50 pF

Parameter	From – To	CMOS	TTL	Units
t_{PHL}	D to Pad	7.0	8.2	ns
t_{PLH}	D to Pad	7.9	6.1	ns
t_{PHZ}	E to Pad	9.1	9.1	ns
t_{PZH}	E to Pad	8.6	6.6	ns
t_{PLZ}	E to Pad	8.9	8.9	ns
t_{PZL}	E to Pad	8.2	9.4	ns

Change in Propagation Delay with Load Capacitance

Parameter	From – To	CMOS	TTL	Units
t_{PHL}	D to Pad	0.05	0.05	ns/pF
t_{PLH}	D to Pad	0.08	0.07	ns/pF
t_{PHZ}	E to Pad	0.11	0.11	ns/pF
t_{PZH}	E to Pad	0.09	0.05	ns/pF
t_{PLZ}	E to Pad	0.11	0.11	ns/pF
t_{PZL}	E to Pad	0.05	0.07	ns/pF

Notes:

1. The BIBUF macro input section exhibits the same delays as the INBUF macro.
2. Load capacitance delay delta can be extrapolated down to 15 pF minimum.

   Example:

   Delay for OUTBUF driving a 100-pF TTL load:

   t_{PHL} = 8.2 + (0.05 x (100–50)) = 10.7 ns

   t_{PLH} = 6.1 + (0.07 x (100–50)) = 9.6 ns

Timing Derating

Operating temperature and voltage and device processing condition account for variations in array timing characteristics.

Timing Derating Factor (x typical)

	Commercial	
Device	**Best Case**	**Worst Case**
A10M20A	0.50	1.64

Note:
Best case reflects maximum operating voltage, minimum operating temperature, and best case processing. Worst case reflects minimum operating voltage, maximum operating temperature, and worst case processing. Best case derating is based on sample data only and is not guaranteed.

These variations are summarized into a derating factor for the A10M20A MPGA typical timing specifications. Derating factors are shown below.

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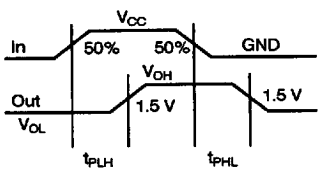
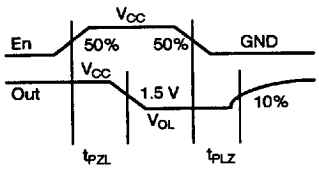
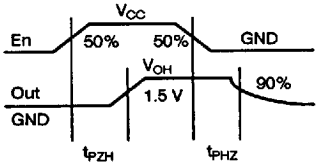
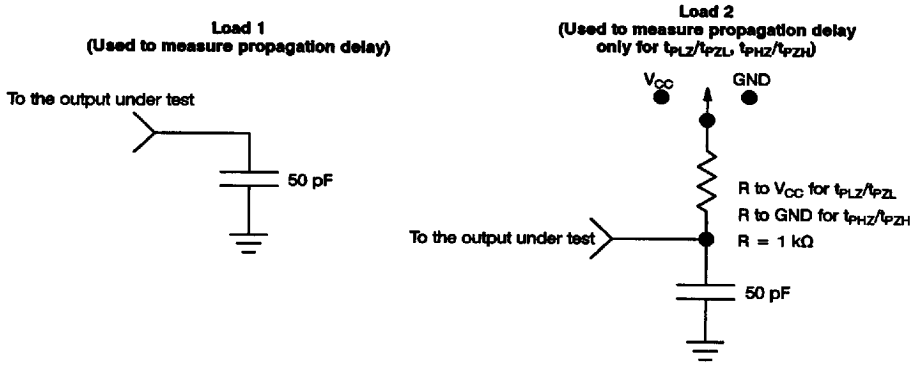
Output Buffer Delays



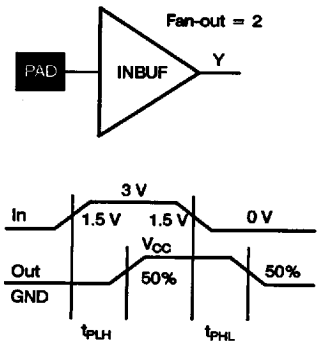




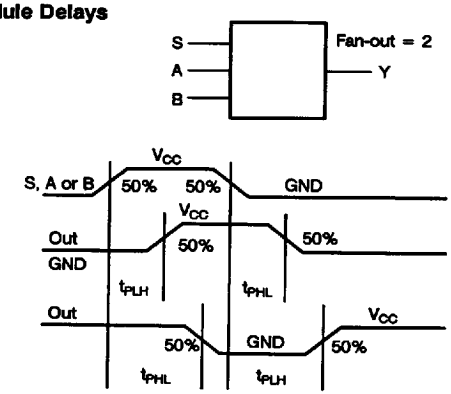
AC Test Loads



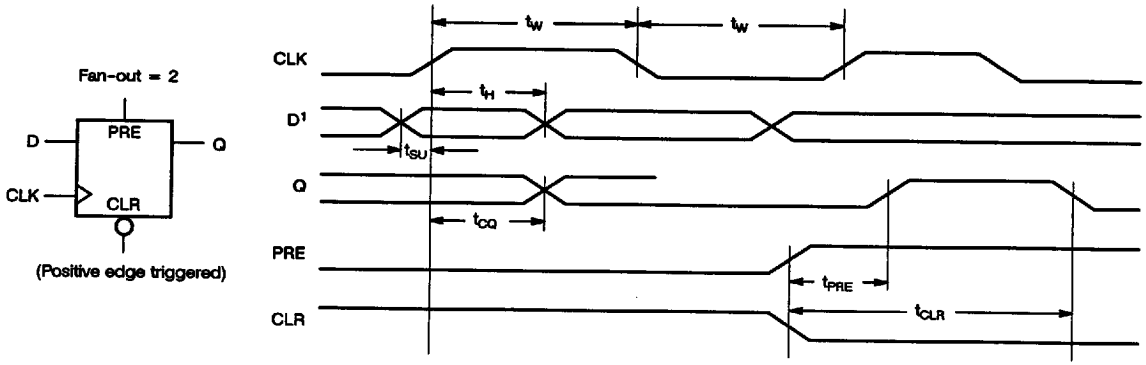
Input Buffer Delays



Module Delays



D-Type Flip-Flop and Clock Delays



Note:

1. For flip-flops with multiplexed inputs, D represents all data functions involving A, B, or S.

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Macro Library

Overview

This selection guide describes ACT 1 macros, which are the same for both FPGA and MPGA devices. These macros are building blocks for designing programmable gate arrays with the Action Logic System (ALS) and your CAE interface.

The macros are divided into four categories: I/O Macros, Hard Macros, Soft Macros and TTL Macros.

Equation Statement Elements

Combinatorial Elements

All equations for combinatorial logic elements use the following operators:

Operator	Symbol
AND	See Note 1
NOT	!
OR	+
XOR	^

Notes:
1. A space between the 'A' and 'B' in the equation Y = A B means **A AND B.**
2. Order of operators in decreasing precedence is: NOT, AND, XOR and OR.
3. Signals expressed in bold have a dual module delay.

Sequential Elements

All equations for sequential logic elements use the following formula:

Q = <!> (<!> CLK or G, <data equation>, <!> CLR, <!> PRE)

<!>	Optional Inversion
CLK	Flip-Flop Clock Pin
G	Latch Gate Pin
CLR	Asynchronous Clear Pin
PRE	Asynchronous Preset Pin

1

MPGA Macro Selections

I/O Macros

Macro Name	No. of Modules I/O	No. of Modules Clock	Description
INBUF	1		Input
BIBUF	1		Bidirectional
CLKBUF	1	1	Input for Dedicated Clock Network
TRIBUF	1		Three State Output
OUTBUF	1		Output

TTL Macros

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Macro Name	Description	Logic Levels	Modules Required
TA138	3 to 8 decoder with enable and active low outputs	2	12
TA139	2 to 4 decoder with enable and active low outputs	1	4
TA151	8 to 1 multiplexor with enable and active low outputs	3	5
TA153	4 to 1 multiplexor Equations: X = (C0 !B !A) + (C1 !B A) + (C2 B !A) + (C3 B A) Y = (!EN X)	2	2
TA157	2 to 1 multiplexor Equation: Y = (!EN !S A) + (!EN S B)	1	1
TA161	4-bit binary counter with clear	3	22
TA164	8-bit shift register with serial in/parallel out	1	18
TA169	4-bit up/down counter	6	25
TA194	4-bit shift register	1	14
TA195	4-bit shift register	1	11
TA269	8-bit up/down binary counter	8	50
TA273	Octal register with clear	1	18
TA280	Parity generator and checker	4	9
TA377	Octel register with enable	1	16

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Soft Macros

Function	Description	Macro Name	Logic Levels	Modules Required
Adders	1-bit adder	FA1	3	3
	8-bit adder	FADD8	4	37
	12-bit adder	FADD12	5	58
	16-bit adder	FADD16	5	79
	24-bit adder	FADD24	6	120
	32-bit adder	FADD32	7	160
Comparators	4-bit identity comparator	ICMP4	2	5
	8-bit identity comparator	ICMP8	3	9
	2-bit magnitude comparator with enable	MCMPC2	3	9
	4-bit magnitude comparator with enable	MCMPC4	4	18
	8-bit magnitude comparator with enable	MCMPC8	6	36
	16-bit magnitude comparator	MCMP16	5	93
Counters	4-bit binary counter with load, clear	CNT4A	4	18
	4-bit binary counter with load, clear, carry in, and carry out	CNT4B	4	15
	4-bit up/down counter with load, carry in, and carry out	UDCNT4A	6	24
Decoders	2 to 4 decoder	DEC2X4	1	4
	2 to 4 decoder with active low outputs	DEC2X4A	1	4
	2 to 4 decoder with enable	DECE2X4	1	4
	2 to 4 decoder with enable and active low outputs	DECE2X4A	1	5
	3 to 8 decoder	DEC3X8	1	8
	3 to 8 decoder with active low outputs	DEC3X8A	1	9
	3 to 8 decoder with enable	DECE3X8	2	11
	3 to 8 decoder with enable and active low outputs	DECE3X8A	2	11
	4 to 16 decoder with active low outputs	DEC4X16A	2	20
Multiplexors	8 to 1 multiplexor	MX8	2	3
	8 to 1 multiplexor with active low output	MX8A	2	3
	16 to 1 multiplexor	MX16	2	5
Multipliers	8 x 8 multiplier	SMULT8		241
Registers	Octal latch with clear	DLC8A	1	8
	Octal latch with enable	DLE8	1	8
	Octal latch with multiplexed data	DLM8	1	8
	Octal with preset, clear, and enable	REGE8A	2	20
	Octal with preset, clear, enable, and active low clock	REGE8B	2	20
	4-bit shift register with clear	SREG4A	2	8
	8-bit shift register with clear	SREG8A	2	18

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Hard Macros

Function	Description	Macro Name	Equation(s)	Modules Required
AND	2-Input	AND2	Y = A B	1
		AND2A	Y = !A B	1
		AND2B	Y = !A !B	1
	3-Input	AND3	Y = A B C	1
		AND3A	Y = !A B C	1
		AND3B	Y = !A !B C	1
		AND3C	Y = !A !B !C	1
	4-Input	AND4	Y = (A B C D)	2
		AND4A	Y = (!A B C D)	2
		AND4B	Y = !A !B C D	1
		AND4C	Y = !A !B !C D	1
		AND4D	Y = (!A !B !C !D)	2
OR	2-Input	OR2	Y = A + B	1
		OR2A	Y = !A + B	1
		OR2B	Y = !A + !B	1
	3-Input	OR3	Y = A + B + C	1
		OR3A	Y = !A + B + C	1
		OR3B	Y = !A + !B + C	1
		OR3C	Y = !(A B C)	2
	4-Input	OR4	Y = A + B + C + D	1
		OR4A	Y = !A + B + C + D	1
		OR4B	Y = !A + !B + C + D	2
		OR4C	Y = !A + !B + !C + D	2
		OR4D	Y = !A + !B + !C + !D	2
NAND	2-Input	NAND	Y = !(A B)	1
		NAND2A	Y = !(A B)	1
		NAND2B	Y = !(!A !B)	1
	3-Input	NAND3	Y = !(A B C)	2
		NAND3A	Y = !(!A B C)	1
		NAND3B	Y = !(!A !B C)	1
		NAND3C	Y = !(!A !B !C)	1
	4-Input	NAND4	Y = !(A B C D)	2
		NAND4A	Y = !(!A B C D)	2
		NAND4B	Y = !(!A !B C D)	2
		NAND4C	Y = !(!A !B !C D)	1
		NAND4D	Y = !(!A !B !C !D)	1
NOR	2-Input	NOR2	Y = !(A + B)	1
		NOR2A	Y = !(!A + B)	1
		NOR2B	Y = !(!A + !B)	1
	3-Input	NOR3	Y = !(A + B + C)	1
		NOR3A	Y = !(!A + B + C)	1
		NOR3B	Y = !(!A + !B + C)	1
		NOR3C	Y = !(!A + !B + !C)	1
	4-Input	NOR4	Y = !(A + B + C + D)	2
		NOR4A	Y = !(!A + B + C + D)	1
		NOR4B	Y = !(!A + !B + C + D)	1
		NOR4C	Y = !(!A + !B + !C + D)	2
		NOR4D	Y = !(!A + !B + !C + !D)	2

Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	Modules Required
Exclusive OR	XOR	XOR	Y = A ^ B	1
		XO1	Y = (A ^ B) + C	1
		XO1A	Y = !(A ^ B) + C	1
	XNOR	XNOR	Y = !(A ^ B)	1
	XOR-AND	XA1	Y = (A ^ B) C	1
		XA1A	Y = !(A ^ B) C	1
	AND-XOR	AX1	Y = (!A B) ^ C	1
		AX1A	Y = !((!A B) ^ C)	1
		AX1B	Y = (!A !B) ^ C	1
AND-OR		AO1	Y = (A B) + C	1
		AO1A	Y = (!A B) + C	1
		AO1B	Y = (A B) + (!C)	1
		AO1C	Y = (!A B) + (!C)	1
		AO2	Y = ((A B) + C + D)	1
		AO2A	Y = ((!A B) + C + D)	1
		AO3	Y = (!A B C) + D	1
		AO4A	Y = (!A B C) + (A C D)	1
		AO5A	Y = (!A B) + (A C) + D	1
		MAJ3	Y = (A B) + (B C) + (A C)	1
AND-OR Invert		AOI1	Y = !(A B + C)	2
		AOI1A	Y = !((!A B) + C)	1
		AOI1B	Y = !((A B) + !C)	1
		AOI2A	Y = !((!A B) + C + D)	1
		AOI2B	Y = !((!A B) + !C + D)	1
		AOI3A	Y = !((!A !B !C) + (!A !D))	1
		AOI4	Y = !(A B + C D)	2
OR-AND		OA1	Y = (A + B) C	1
		OA1A	Y = (!A + B) C	1
		OA1B	Y = (A+ B) (!C)	1
		OA1C	Y = (!A + B) (!C)	1
		OA2	Y = (C + D) (A + B)	1
		OA2A	Y = ((C + D) (!A + B))	1
		OA3	Y = ((A + B) C D)	1
		OA3A	Y = ((A + B) !C D)	1
		OA3B	Y = ((!A + B) !C D)	1
		OA4A	Y = ((A + B + !C) D)	1
		OA5	Y = (A + B + C) (A + D)	1
OR-AND Invert		OAI1	Y = !((A + B) & C)	1
		OAI2A	Y = !((A + B + C) !D)	1
		OAI3	Y = !((A + B) C D)	2
		OAI3A	Y = !((A + B) !C !D)	1
Buffers and Inverters		BUF	Y = A	1
		BUFA	Y = !(!A)	1
		INV	Y = !A	1
		INVA	Y = !A	1

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Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	Modules Required
Multiplexors	2:1	MX2	Y = (A !S) + (B S)	1
		MX2A	Y = (!A !S) + (B S)	1
		MX2B	Y = (A !S) + (!B S)	1
		MX2C	Y= (!A !S) + (!B S)	1
	4:1	MX4	Y = (D0 !S0 !S1) + (D1 S0 !S1) + (D2 !S0 S1) + (D3 S0 S1)	1
Adders	Half	HA1	CO =A B S =A ^ B	2
		HA1A	CO = !A B S = !(A ^ B)	2
		HA1B	CO = !(A B) S = !(A ^ B)	2
		HA1C	CO = !(A B) S = (A ^ B)	
	Full	FA1A	CO = (CI !B !A) + (A !B) + (B CI A) S = (B !A !CI) + (CO !A CI) + (CO A !CI) + (B A CI)	2
		FA1B	CO = !A(!B + B CI) + A(!B CI) S = !A(!CI CO + CI B) + A(!CI B + CI CO)	2
		FA2A	CO = (CI !B !(A0+A1)) + (!B (A0+A1)) + (B CI (A0+A1)) S = (B !(A0+A1) !CI) + (CO !(A0+A1) CI) + (CO (A0+A1) !CI) + (B (A0+A1)CI)	2
		FA3A	CO = (B0 !(A0+A1)!B1)+(!(A0 + A1) B1)+ ((A0 + A1) !B1) +((A0 + A1) B1) S = (B0 !(A0 + A1) !B2) + (!(A0 + A1) B2) + (B0 (A0 + A1) !B1)	2
Boolean		MXCI	Y = (!((!S A) + (S B)) C) + (((!S A) + (S B)) D)	1
		MXT	Y = (!S1 !S0A D0) + (!S1 S0A D1)+ (S1 !S0B D2) + (S1 S0B D3)	1
D-type Flip-Flops	with clear	DF1	Q = (CLK, D, –, –)	2
		DF1A	QN = !(CLK, D, –, –)	2
		DF1B	Q = (!CLK, D, –, –)	2
		DF1C	QN = !(!CLK, D, –, –)	2
		DFC1	Q = (CLK, D, CLR, –)	2
		DFC1A	Q = (!CLK, D, CLR, –)	2
		DFC1B	Q = (CLK, D, !CLR, –)	2
		DFC1C	QN = !(CLK, D, CLR, –)	2
		DFC1D	Q = (!CLK, D, !CLR, –)	2
		DFC1E	QN = !(CLK, D, !CLR, –)	2
		DFC1F	QN = !(!CLK, D, CLR, –)	2
		DFC1G	QN = !(!CLK, D, !CLR, –)	2

Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	Modules Required
D-type Flip-Flops (continued)	with enable	DFE	Q = (CLK, E D + !E Q, –, –)	2
		DFE1B	Q = (CLK, !E D + E Q, –, –)	2
		DFE1C	Q = (!CLK, !E D + E Q, –, –)	2
		DFE2D	Q = (!CLK, !E D + E Q, !CLR, PRE)	2
		DFE3A	Q = (!CLK, E D + !E Q, !CLR, –)	2
		DFE3B	Q = (!CLK, E D + !E Q, !CLR, –)	2
		DFE3C	Q = (CLK, !E D + E Q, !CLR, –)	2
		DFE3D	Q = (!CLK, !E D + E Q, !CLR, –)	2
		DFE4	Q = (CLK, E D + !E Q, –, PRE)	2
		DFE4A	Q = (!CLK, E D + !E Q, –, PRE)	2
		DFE4B	Q =(CLK, !E D + E Q, –, PRE)	2
		DFE4C	Q = (!CLK, !E D + E Q, –, PRE)	2
		DFEA	Q = (!CLK, E D + !E Q, –, –)	2
		DFEB	Q = (CLK, E D + !E Q, !CLR,PRE)	2
		DFEC	Q = (!CLK, E D + !E Q, !CLR, PRE)	2
		DFED	Q = (CLK, !E D + E Q, !CLR, PRE)	2
	with multiplexed data	DFM	Q = (CLK, !S A + S B, –, –)	
		DFM1B	QN = !(CLK, !S A + S B, –, –)	2
		DFM1C	QN = !(!CLK, !S A + S B, –, –)	2
		DFM3	Q = (CLK, !S A + S B, CLR, –)	2
		DFM3B	Q = (!CLK, !S A + S B, !CLR, –)	2
		DFM3E	Q = (!CLK, !S A + S B, CLR, –)	2
		DFM3F	QN = !(CLK, !S A + S B, CLR, –)	2
		DFM3G	QN = !(!CLK, !S A + S B, CLR, –)	2
		DFM4	Q = (CLK, !S A + S B, –, PRE)	2
		DFM4A	Q = (CLK, !S A + S B, –, !PRE)	2
		DFM4B	Q = (!CLK, !S A + S B, –, !PRE)	2
		DFM4C	QN = !(CLK, !S A + S B, –, !PRE)	2
		DFM4D	QN = !(!CLK, !S A + S B, –, !PRE)	2
		DFM4E	Q = (!CLK, !S A + S B, –, PRE)	2
		DFM5A	Q = (CLK, !S A + S B, !CLR, PRE)	2
		DFM5B	Q = (!CLK, !S A + S B, !CLR, PRE)	2
		DFMA	Q = (!CLK, !S A + S B, –, –)	2
		DFMB	Q = (CLK, !S A + S B, !CLR, –)	2
	with multiplexed data and enable	DFME1A	Q = (CLK, !E (!S A + S B) + E Q, –, –)	2
	with preset	DFP1	Q = (CLK, D, –, PRE)	2
		DFP1A	Q = (!CLK, D, –, PRE)	2
		DFP1B	Q = (CLK, D, –, !PRE)	2
		DFP1C	QN = !(CLK, D, –, PRE)	2
		DFP1D	Q = (!CLK, D, –, !PRE)	2
		DFPIE	QN = !(CLK, D, –, !PRE)	2
		DFP1F	QN= !(!CLK, D, –, PRE)	2
		DFP1G	QN = !(!CLK, D, –, !PRE)	2
	with clear and preset	DFPC	Q = (CLK, D, !CLR, PRE)	2
		DFPCA	Q = (!CLK, D, !CLR, PRE)	2

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Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	Modules Required
JK Flip-Flops		JKF	Q = (CLK, (!Q J + Q K)), –, –)	2
		JKF1B	Q = (!CLK, (!Q J + Q K), –, –)	2
		JKF2A	Q = (CLK, (!Q J + Q K), !CLR, –)	2
		JKF2B	Q = (!CLK, (!Q J + Q K), !CLR, –)	2
		JKF2C	Q = (CLK, (!Q J + Q K), CLR, –)	2
		JKF2D	Q = (!CLK, (!Q J + Q K), CLR, –)	2
		JKF3A	Q = (CLK, (!Q J + Q K), – !PRE)	2
		JKF3B	Q = (!CLK, (!Q J + Q K), –, !PRE)	2
		JKF3C	Q = (CLK, (!Q J + Q K), –, PRE)	2
		JKF3D	Q = (!CLK, (!Q J + Q K), –, PRE)	2
		JKF4B	Q = (!CLK, (!Q J + Q K), !CLR, PRE)	2
		JKFPC	Q = (CLK, (!Q J + Q K), !CLR, PRE)	2
Data Latches		DL1	Q = (G, D, –, –)	1
		DL1A	QN = !(G, D, –, –)	1
		DL1B	Q = (!G, D, –, –)	1
		DL1C	QN = !(!G, D, –, –)	1
	with clear	DLC	Q = (G, D, !CLR, –)	1
		DLC1	Q = (G, D, CLR, –)	1
		DLC1A	Q = (!G, D, CLR, –)	1
		DLC1F	QN = !(G, D, CLR, –)	1
		DLC1G	QN = !(!G, D, CLR, –)	1
		DLCA	Q = (!G, D, !CLR, –)	1
		DLE	Q = (G, (E D + !E Q), –, –)	1
		DLE1D	QN = !(!G, (!E D + E Q), –, –)	1
		DLE2A	Q = (!G, (E D + !E Q), CLR, –)	1
		DLE2B	Q = (!G, (!E D + E Q), !CLR, –)	1
		DLE2C	Q = (!G, (!E D + E Q), CLR, –)	1
	with enable	DLE3A	Q = (!G, (E D + !E Q), –, PRE)	1
		DLE3B	Q = (!G, (!E D + E Q), –, PRE)	1
		DLE3C	Q = (!G, (!E D + E Q), –, !PRE)	1
		DLEA	Q = (G, (!E D + E Q), –, –)	1
		DLEB	Q = (!G, (E D + !E Q), –, –)	1
		DLEC	Q = (!G, (!E D + E Q), –, –)	1
	with multiplexed data	DLM	Q = (G, (A !S + B S), –, –)	1
		DLM2A	Q = (!G, (A !S + B S), CLR, –)	1
		DLMA	Q = (!G, (A !S + B S), –, –)	1
	with multiplexed data and enable	DLME1A	Q = (!G, !E (A !S + B S) + E Q, –, –)	1
	with preset	DLP1	Q = (G, D, –, PRE)	1
		DLP1A	Q = (!G, D, –, PRE)	1
		DLP1B	Q = (G, D, –, !PRE)	1
		DLP1C	Q = (!G, D, –, !PRE)	1
		DLP1D	QN = !(G, D, –, !PRE)	1
		DLP1E	QN = !(!G, D, –, !PRE)	1
	with preset and clear	DL2A	Q = (G, D, !CLR, PRE)	1
		DL2B	QN = !(!G, D, CLR, !PRE)	1
		DL2C	Q = (!G, D, !CLR, PRE)	1
		DL2D	QN = !(G, D, CLR, !PRE)	1

Hard Macros (continued)

Function	Description	Macro Name	Equation(s)	Modules Required
Clock Net Interface Macros		GAND2	Y = A G	1
		GMX4	Y = (D0 !S0 !G) + (D1 !G S0) + (D2 G !S0) + (D3 S0 G)	1
		GNAND2	Y = !(A G)	1
		GNOR2	Y = !(A + G)	
		GOR2	Y = A + G	1
		GXOR	Y = A ^ G	1
Logical Tieoff Macros		GND		
		VCC		

Hard Macro Library Overview

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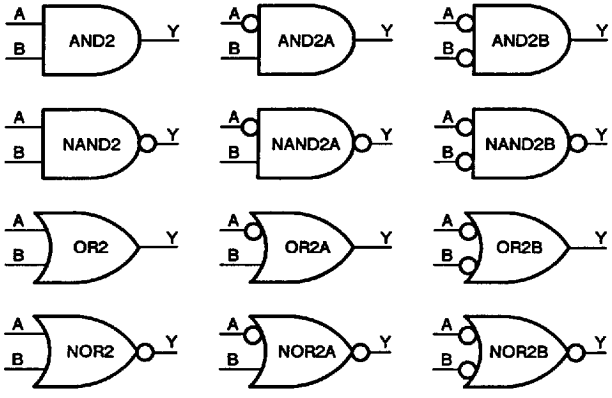
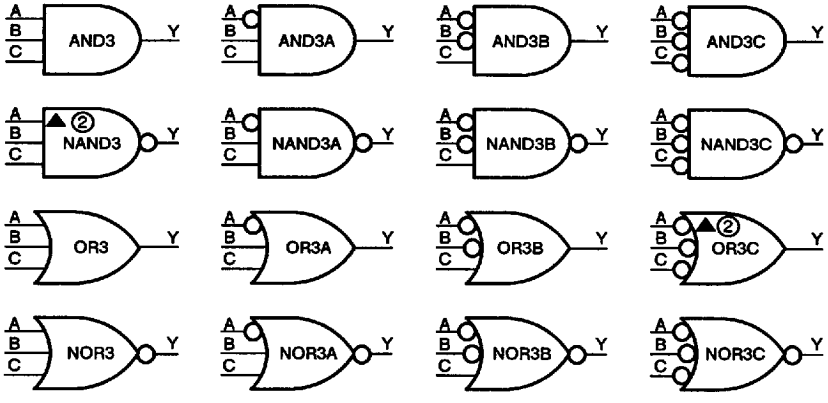
The following illustrations show all the available Hard Macros.

2-Input Gates (Module Count = 1)



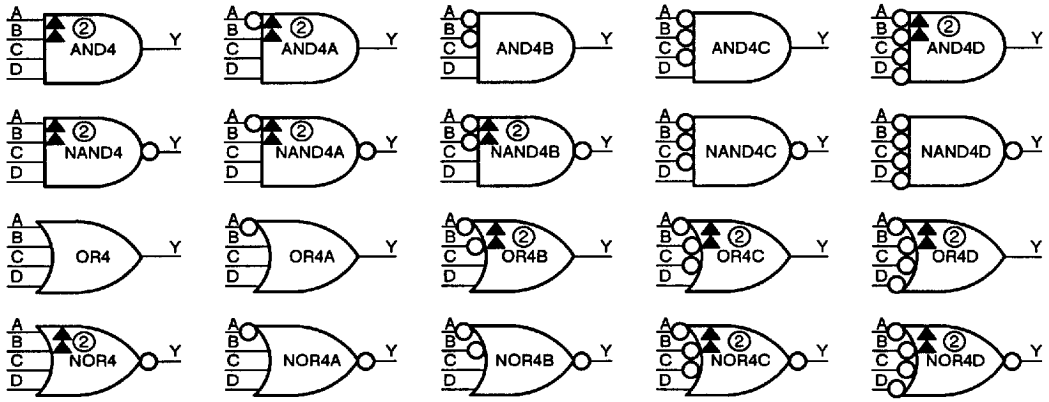
3-Input Gates (Module Count = 1, unless indicated otherwise)

② Indicates 2-module macro
▲ Indicates extra delay input



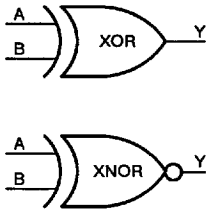
4-Input Gates (Module Count = 1, unless indicated otherwise)

② Indicates 2-module macro
▲ Indicates extra delay input

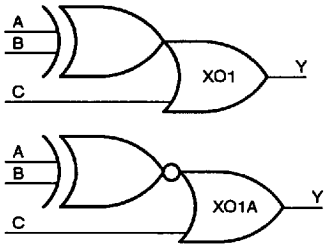


1

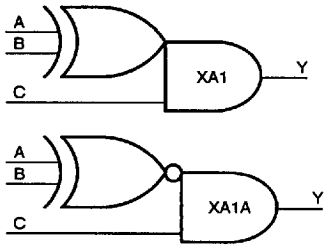
XOR Gates
(Module Count = 1)



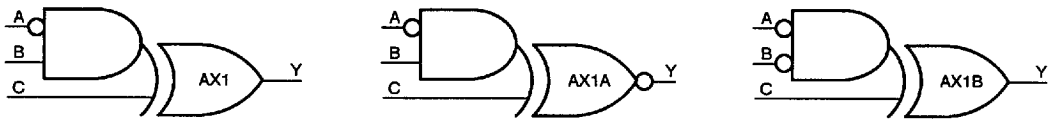
XOR OR Gates
(Module Count = 1)



XOR AND Gates
(Module Count = 1)



AND XOR Gates
(Module Count = 1)



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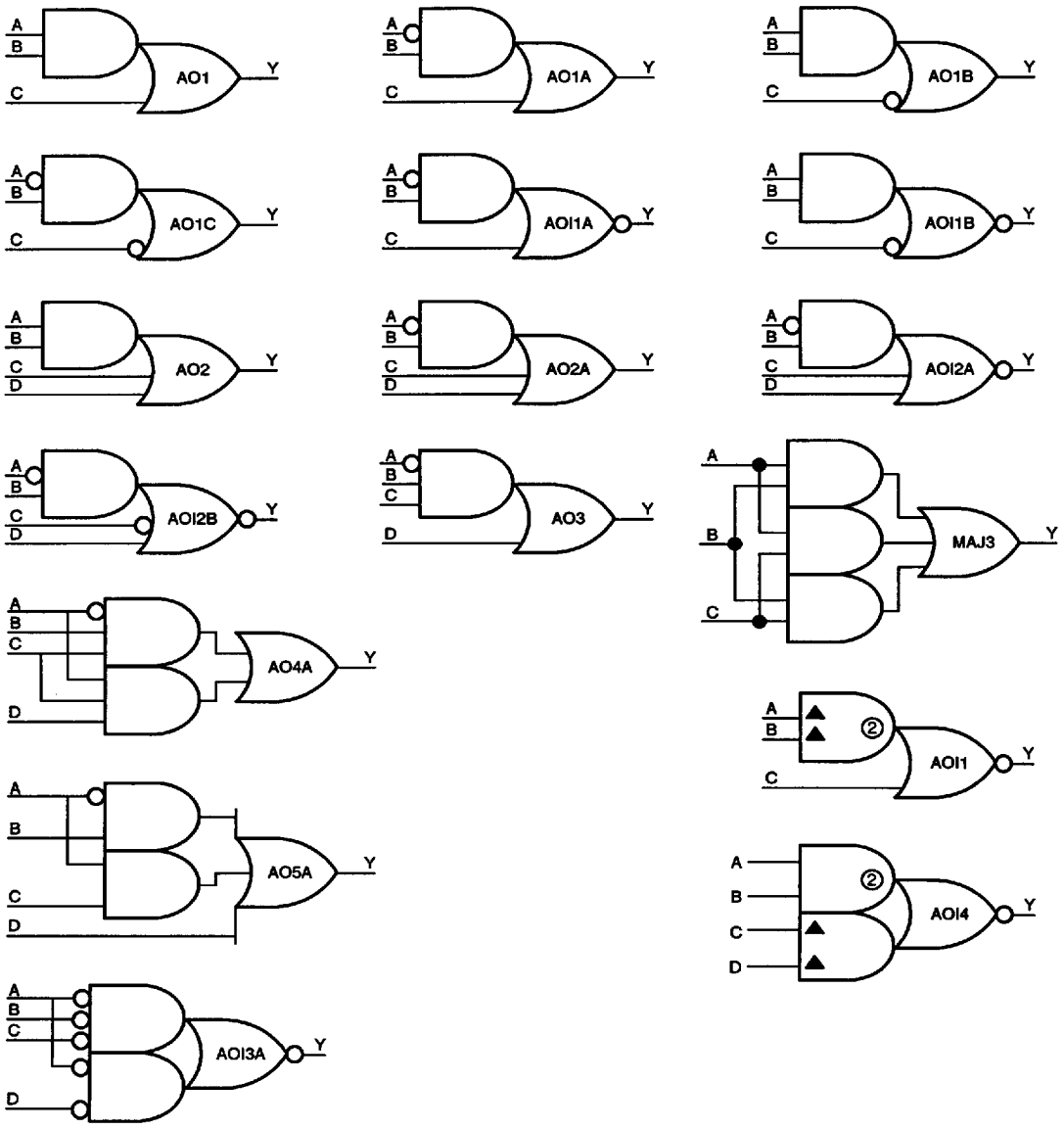
AND OR Gates (Module Count = 1)

② Indicates 2-module macro
▲ Indicates extra delay input



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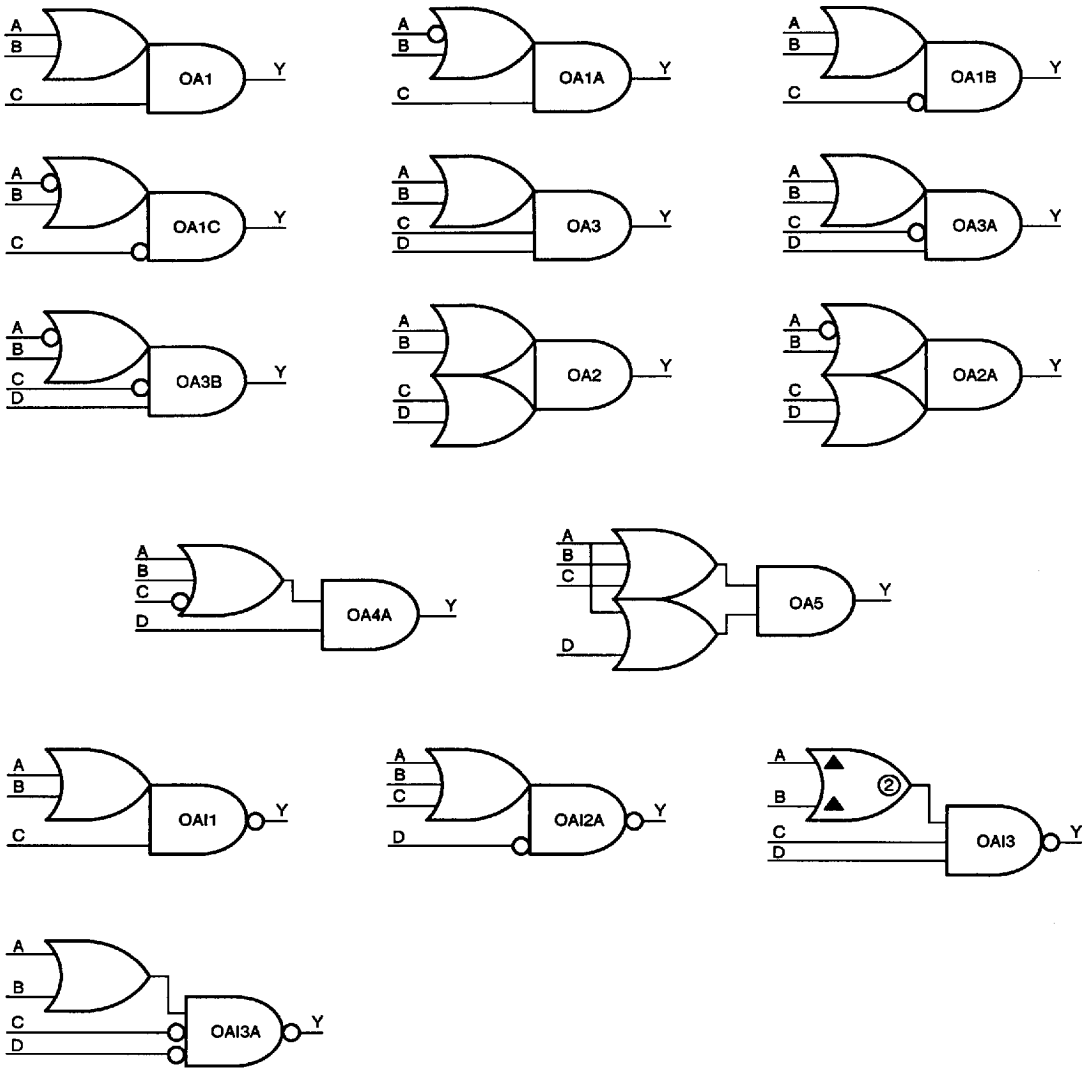
OR AND Gates (Module Count = 1)

② Indicates 2-module macro
▲ Indicates extra delay input



1

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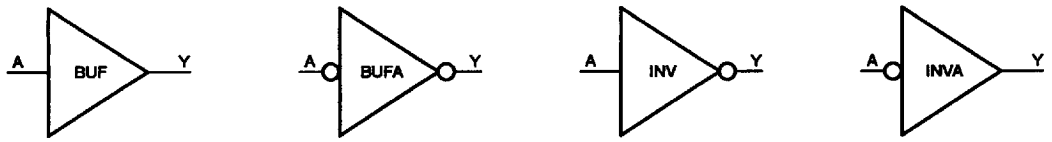
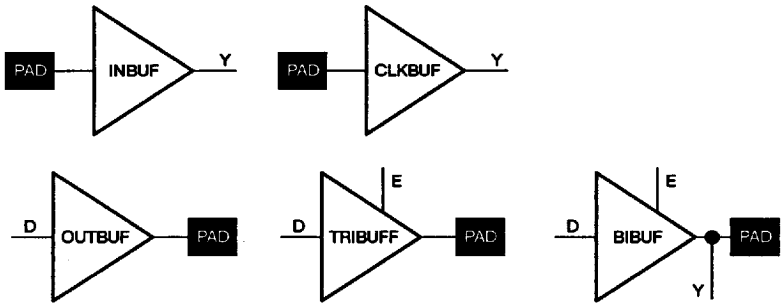
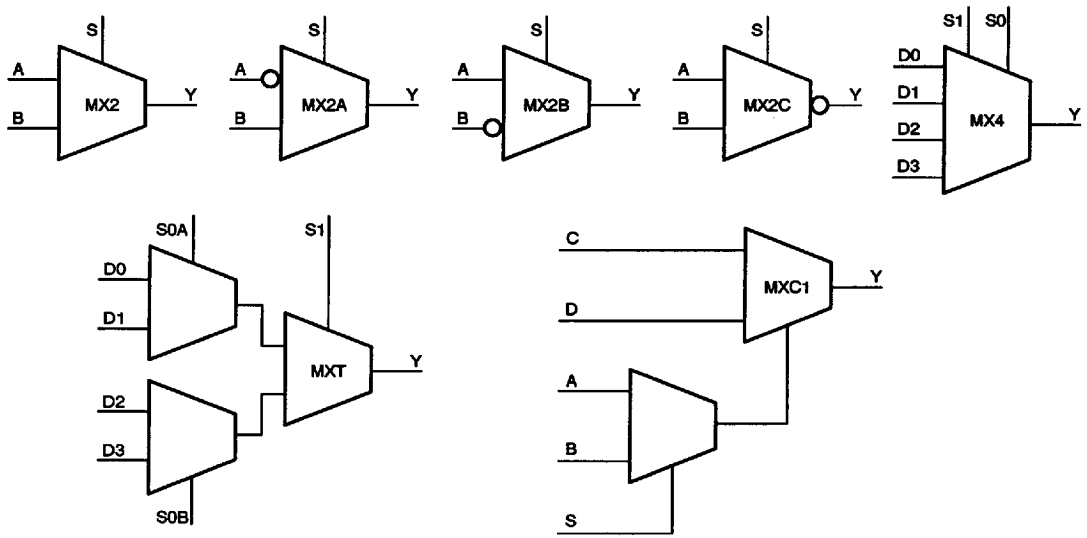
Buffers (Module Count = 1)



I/O Buffers (I/O Module Count = 1)



Multiplexors (Module Count = 1)



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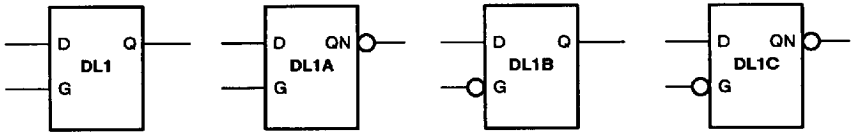
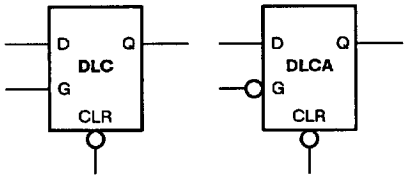
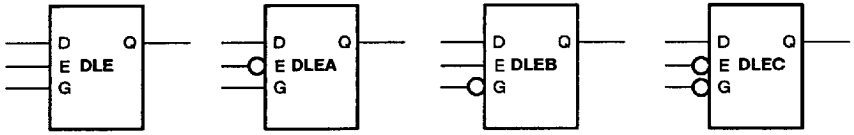
Latches (Module Count = 1)



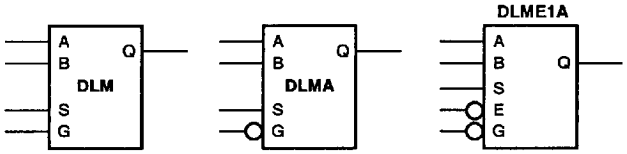
D Latches with Clear (Module Count = 1)



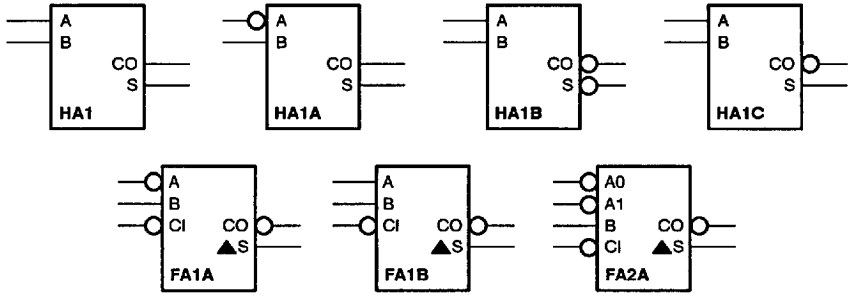
D Latches with Enable (Module Count = 1)



Mux Latches (Module Count = 1)



Adders (Module Count = 2)



Macros FA1A, FA1B, and FA2A have two level delays from the inputs to the S outputs, as indicated by the▲

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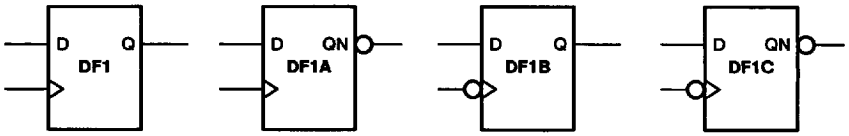
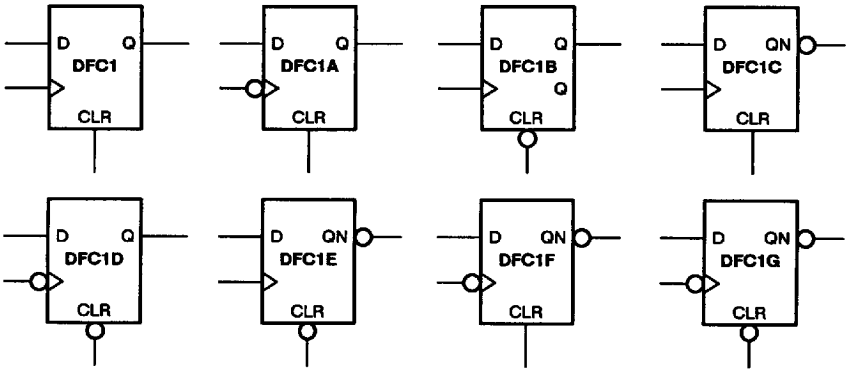
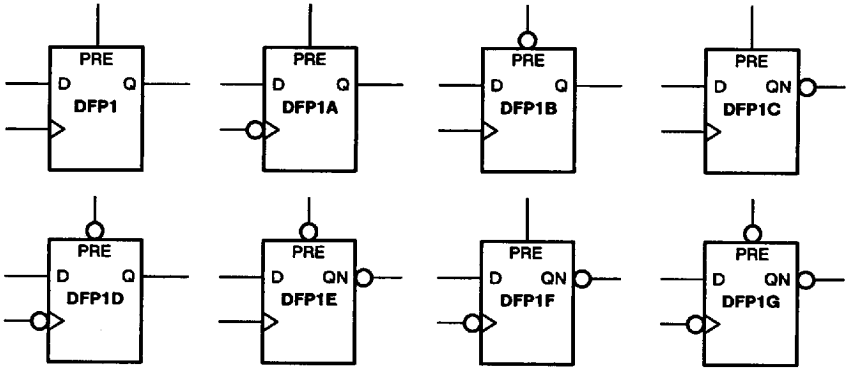
D-type Flip-Flops (Module Count = 2)



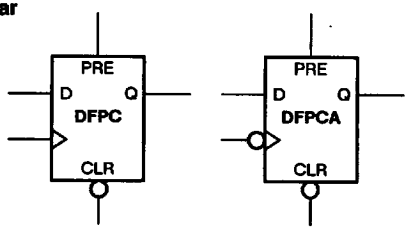
D-type Flip-Flops with Clear



D-type Flip-Flops with Preset



D-type Flip-Flops with Preset and Clear



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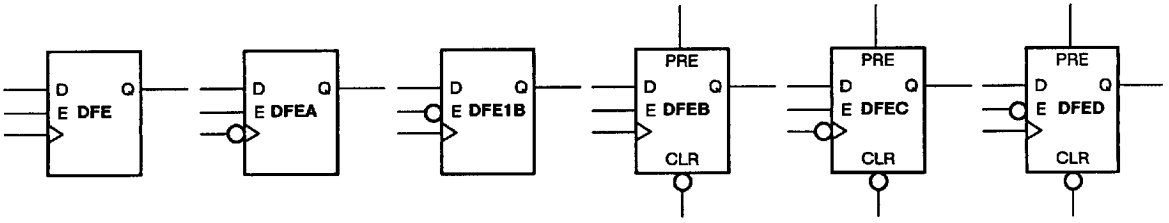
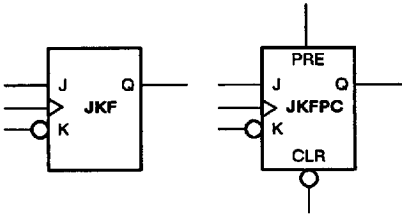
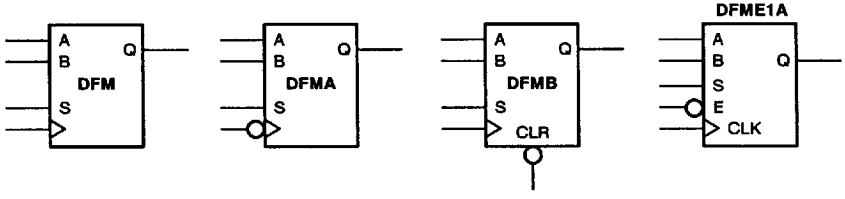
D-type Flip-Flops with Enable (Module Count = 2)



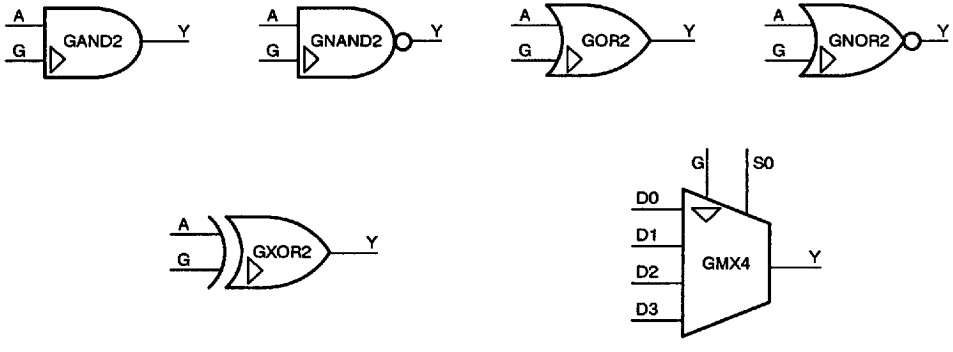
JK Flip-Flops (Module Count = 2)



MUX Flip-Flops (Module Count = 2)



CLKBUF Interface Macros (Module Count = 1)



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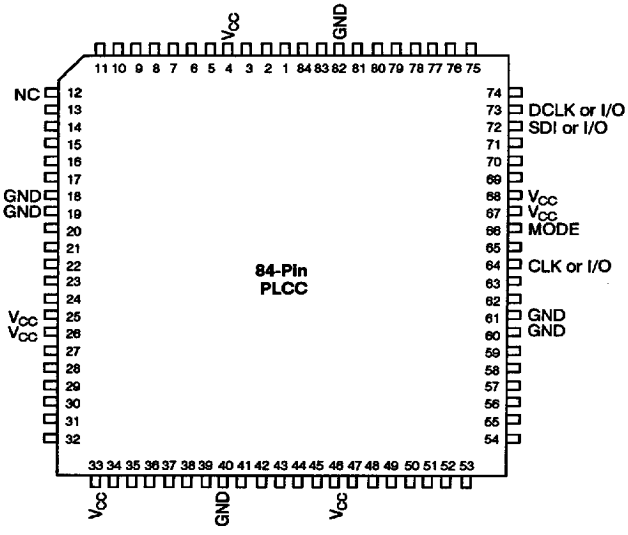
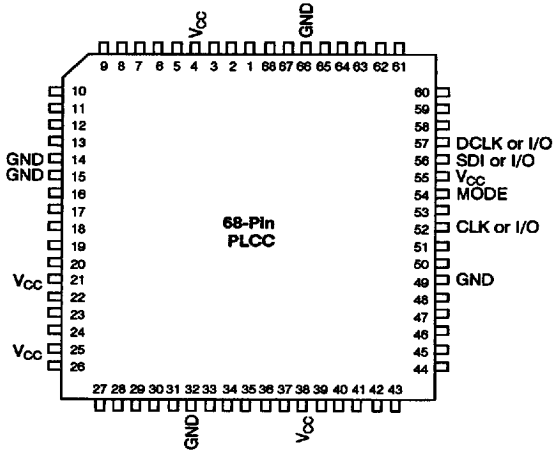
Package Pin Assignments: 84-Pin PLCC
(Top View)



Package Pin Assignments: 68-Pin PLCC
(Top View)



Notes:
1. MODE must be terminated to circuit ground.
2. All unassigned pins are available for use as I/Os.

Package Pin Assignments: 100-Pin PQFP (Top View)

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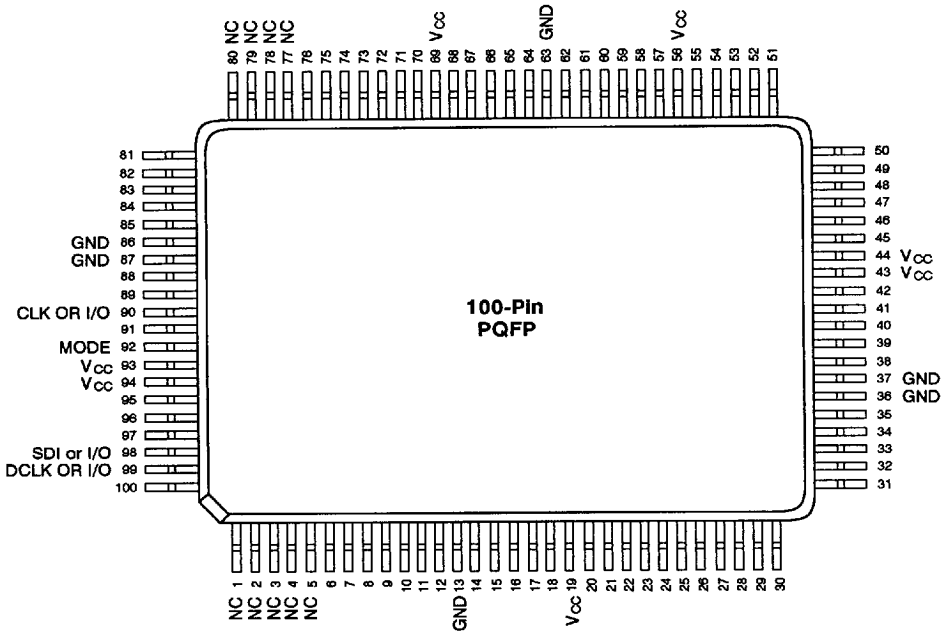

Notes:
1. MODE must be terminated to circuit ground.
2. All unassigned pins are available for use as I/Os.

Package Mechanical Details

Plastic J-Leaded Chip Carrier

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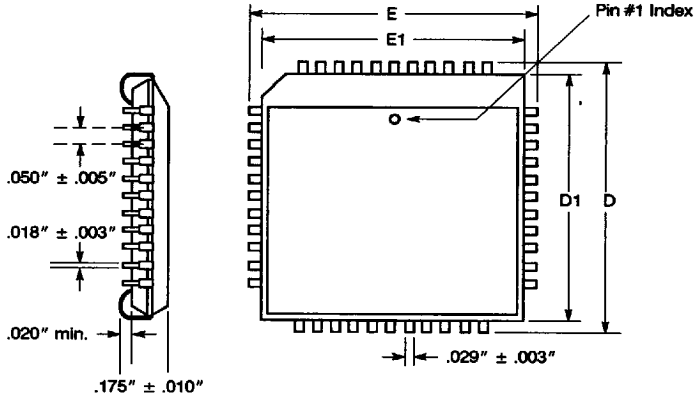

Lead Count	D, E	D1, E1
68	.990" ± .005"	.955" ± .005"
84	1.190" ± .005"	1.155" ± .005"

Package Mechanical Details (continued)

Plastic Quad Flatpack

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Dimensions in millimeters