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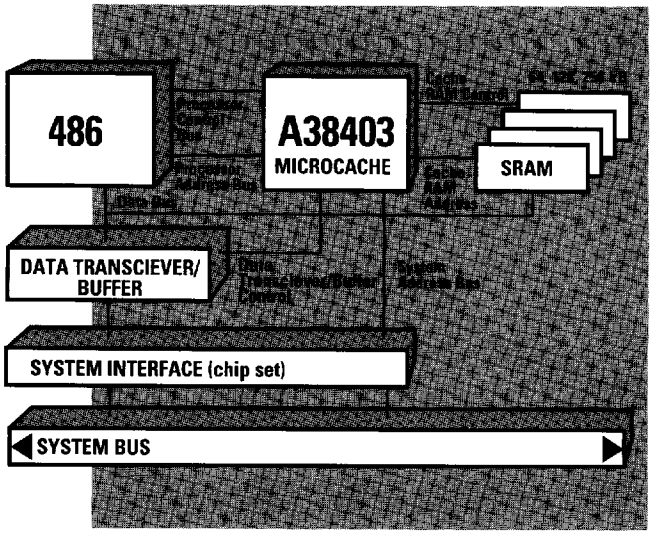
MICROCACHE® HIGH PERFORMANCE

***An effective second level cache memory can significantly increase the performance of a 486 system. Austek's A38403 write-back cache memory controller for the 486 maximizes cache performance, allows product differentiation, and can be optimally configured for Windows, OS/2, UNIX and networking environments.***




# 486

## A38403 MICROCACHE FOR 486 SYSTEMS

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*The A38403 is a write-back cache controller for cache sizes of 64-kBytes, 128-kBytes and 256-kBytes. The cache memory can be configured as two-way or four-way set associative for highest performance. The A38403 operates at 25-MHz, 33-MHz and 50-MHz. It may easily be incorporated into a design with the 486 microprocessor to interface to the AT, EISA or MCA bus.*

*The A38403 has 1048 on-chip tags, eliminating the need for external high speed tag SRAMs. Performance is maximized by zero wait state read and write hits, high hit rates and low write miss penalties. Multiple on-chip programmable registers allow optimum configuration for the end user environment. Cache data memory is implemented with standard SRAMs, burst reads to the 486 are implemented by the A38403 and burst SRAMs are not required. The device allows caching of BIOS and ROM code, which can provide over 30% performance improvement for ROM-intensive routines such as video. A separate clock reset, which synchronizes but does not flush the cache on reset, improves performance with Windows, OS/2 and network operating systems. Performance in systems with alternate bus masters such as network and SCSI cards is improved by using a snoop bus to maintain cache coherency; this allows the 486 to continue execution during DMA, refresh and master operations.*

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# A38403 MICROCACHE FOR 486 SYSTEMS

### Key Features

- Directly interfaces to 486 microprocessor and 486 chip sets
- Configuration options programmable by BIOS
- Supports three cache sizes – *64-kByte, 128-kByte and 256-kByte*
  - *64-kByte cache size may be supported by reducing address space to 2-GByte*
  - *System may be populated with minimum cache and easily expanded to larger sizes and associativity by the end user*
- Caches full 486 address space
- Two-way or four-way set associative
- Selectable write-back or write-through memory update policies
- Write buffer control for increased write-through update performance
- True least recently used (LRU) replacement algorithm
- Full bandwidth support for 486 burst mode
- Burst mode support for DRAM reads and writes
- On-chip high speed tag SRAMs
- The A38403 interfaces directly to standard x8 and x16 cache data SRAMs or to x9 and x18 SRAMs when parity support is required

### Cache Data SRAM Options

| | Two-way | Four-way |
|---|---|---|
| *64-kByte cache* | *8 4Kx16*<br>*8 8Kx8* | *8 4Kx16* |
| *128-kByte cache* | *4 16Kx16*<br>*8 8Kx16* | *8 8Kx16* |
| *256-kByte cache* | *8 16Kx16*<br>*8 32Kx8* | *8 16Kx16* |

- On-chip programmable configuration options
  - *Cache size and associativity*
  - *Thirty two 16-kByte blocks in the second half megabyte address space (80000 to FFFFF) which may each be defined as non-cache, cache read-only, cache read/write or cache write-back*
  - *Six regions of any multiple of 64-kByte locatable on any 64-kByte boundary which may each be defined as non-cache, cache read-only, cache read/write, cache write-back or local*
  - *Control of the number of T states between I/O cycles on the system bus*
  - *Decode or ignore local bus cycles (e.g. Weitek 4167)*
  - *Enable/disable second level caching/freeze cache content*
- Cache input provides for additional noncache regions
- Separate functional (PWRRESET) and clock (RESET) reset inputs - RESET synchronizes, but does not flush the cache, this increases performance in Windows, OS/2 and network operating systems
- Cache coherency functions
  - Snoop bus monitors system address bus
    - *Increases system performance by allowing the processor to continue execution during DMA, refresh and other bus master activity.*
    - *Inhibits DRAM cycle and substitutes cache data when address is present and dirty in the cache*
  - Coherency maintained with 486 internal cache, A38403 filters out unnecessary invalidations
- On-chip diagnostic mode to test cache data SRAM
- On-chip fault detection to help system debug
- 25 MHz, 33 MHz, and 50 MHz speeds
- Low power CMOS
- 208 lead plastic quad flat pack (EIAJ)

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