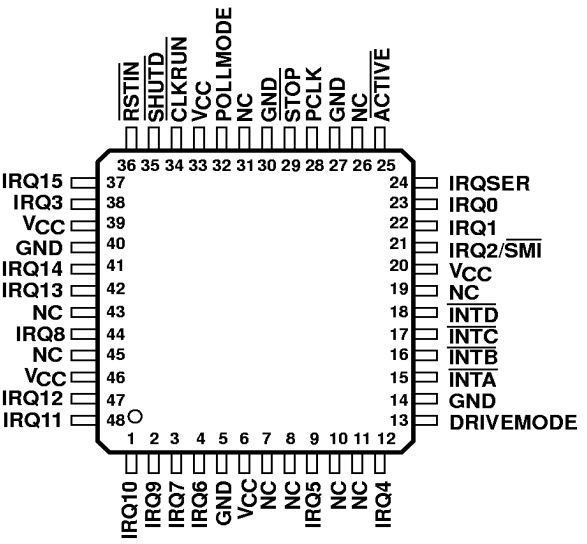
SCPS015A – JULY 1997 – REVISED JANUARY 1998

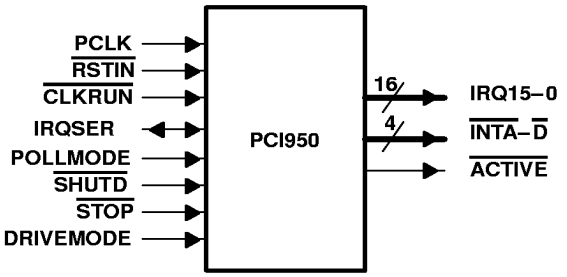
- 5-V Core Logic With PCI Interface
- Supports PCI Clock Frequencies up to 33 MHz
- Accepts IRQSER Serial Interrupt Stream Input From TI™ PC Card Controllers
- Provides System Access to All 15 ISA-Style IRQs and 4 PCI-Style Interrupts
- Offered in 48-Pin TQFP Package



description

The PCI950 is an IRQSER interrupt deserializer that interfaces with existing and future TI PC Card controllers. The PCI950 accepts the IRQSER output of a TI PC Card controller and converts it to 16 ISA-style interrupts and 4 PCI-style interrupts. Interfacing the PC Card controller with the PCI950 permits system access of all available interrupts and features of the PC Card controller.

functional block diagram



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PCI bus

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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
$\overline{\text{ACTIVE}}$	25	O	Device active. When the PCI950 is busy, this output is low and when the PCI950 is idle, this output is high.
$\overline{\text{CLKRUN}}$	34	I/O	PCI clock run. $\overline{\text{CLKRUN}}$ is used by the central resource to request permission to stop the PCI clock or to slow the PCI clock rate. When the PCI950 is busy and $\overline{\text{CLKRUN}}$ is sampled high, then $\overline{\text{CLKRUN}}$ is driven low for two clock cycles. If $\overline{\text{CLKRUN}}$ is not used, it can be tied low. See Note 1.
DRIVEMODE	13	I	Drive mode. When this input is high and the PCI950 samples a low on the IRQSER line during the sample phase of the IRQ data frame, then the PCI950 drives the IRQSER line high during the recovery phase. When this input is low and the PCI950 samples a low level on the IRQSER line during the sample phase of the IRQ data frame, then the PCI950 three-states the IRQSER line during the recovery phase.
GND	5, 14, 27, 30, 40	—	Device ground terminals
$\overline{\text{INTA}}$, $\overline{\text{INTB}}$, $\overline{\text{INTC}}$, $\overline{\text{INTD}}$	15, 16, 17, 18	O	PCI-style interrupts. These are four parallel PCI-style Interrupts, $\overline{\text{INTA}}$–$\overline{\text{INTD}}$. The PCI950 provides the PCI interrupts in an open-drain environment, which requires the system vendor to implement a pullup resistor on each implemented interrupt.
IRQ0, IRQ1, IRQ3–15	23, 22, 38,12, 9, 4, 3, 44, 2, 1, 48, 47, 42, 41, 37	O	ISA-style interrupts. These are 15 parallel ISA interrupts, IRQ0, 1, 3–15. The PCI950 provides the ISA interrupts in an open-drain environment, which requires the system vendor to implement a pullup resistor on each implemented interrupt.
IRQ2/$\overline{\text{SMI}}$	21	O	System management interrupt. The PCI950 provides the $\overline{\text{SMI}}$ interrupt in an open-drain environment, which requires the system vendor to implement a pullup resistor on each implemented interrupt.
IRQSER	24	I/O	Serial interrupt stream from PC Card controller. This input is connected to the IRQSER output from the TI PC Card controller.
NC	7, 8, 10, 11, 19, 26, 31, 43, 45	—	No connection
PCLK	28	I	PCI-bus clock. The PCI-bus clock operates at frequencies ranging from 0–33 MHz.
POLLMODE	32	I	Poll mode. Selects between quiet mode and continuous mode. When this input is low, the PCI950 is in quiet mode. When this input is high, the PCI950 is in continuous mode. The POLLMODE signal is sampled during the rising edge of a start frame. After reset, the PCI950 generates the first cycle, and the stop-frame width in this cycle is set based on the POLLMODE input level. Any change in POLLMODE input causes the PCI950 to generate a start pulse.
$\overline{\text{RSTIN}}$	36	I	Device reset. When $\overline{\text{RSTIN}}$ is asserted low, the internal counters are reset and all output buffers are put in a high-impedance state (three stated). After $\overline{\text{RSTIN}}$ is deasserted, the PCI950 defaults to continuous mode.
$\overline{\text{SHUTD}}$	35	I	Shutdown. When $\overline{\text{SHUTD}}$ input is low, the internal clock is stopped and the outputs are placed in a high-impedance state (three stated). When $\overline{\text{SHUTD}}$ input is high, the device is in normal operation. During continuous mode of operation, the recommended use of $\overline{\text{SHUTD}}$ is to first assert $\overline{\text{STOP}}$ input, check that $\overline{\text{ACTIVE}}$ is high, and then assert $\overline{\text{SHUTD}}$ to stop the clock. During quiet mode of operation, the $\overline{\text{SHUTD}}$ input can be asserted after $\overline{\text{ACTIVE}}$ is sampled high.
$\overline{\text{STOP}}$	29	I	Stop continuous mode. The default number of idle clocks between stop and start frame in continuous mode is one. But the $\overline{\text{STOP}}$ pin can be used to insert more than one idle state. If the PCI950 is in continuous mode and if during an IRQSER cycle the $\overline{\text{STOP}}$ input is driven low, then after completion of the IRQSER cycle any number of idle states can be inserted. The next start frame is initiated by PCI950 when $\overline{\text{STOP}}$ is driven high. If $\overline{\text{STOP}}$ is not to be used, then it must be tied high. See Note 1.
V_{CC}	6, 20, 33, 39, 46	—	Device 5-V power-supply terminals

NOTE 1: Unused active-low inputs must be pulled up to V_{CC} using a 43 kΩ resistor, and unused active-high inputs must be pulled down to GND using a 43 kΩ resistor.

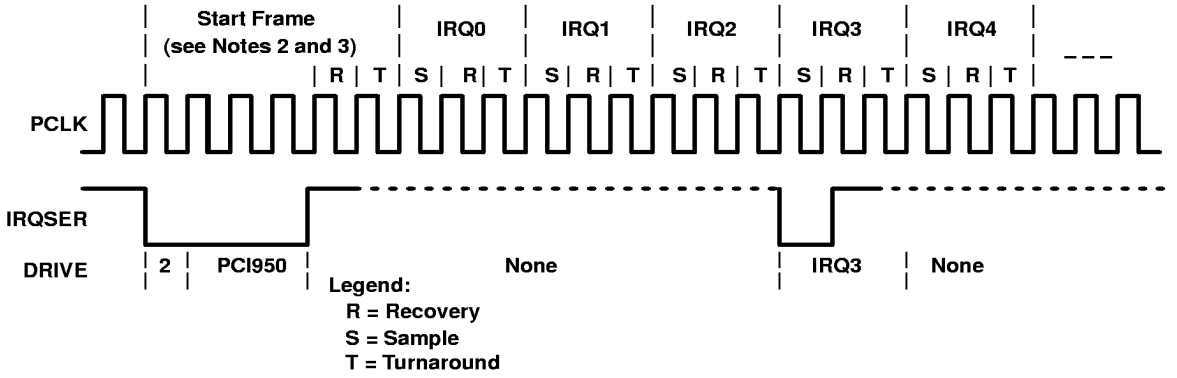
functional description

The PCI950 accepts the serialized IRQ stream from the PC Card controller for conversion to discrete ISA and PCI interrupts. The serialized IRQ protocol is defined in the document *Serialized IRQ Protocol for PCI Systems*, revision 6.0. This protocol uses a serial packet consisting of one start frame, several IRQ/data frames, and one stop frame.

Start frame: There are two modes of operation for the IRQSER start frame – quiet mode and continuous mode. During continuous mode the PCI950 initiates the start frame. A low level on the POLLMODE input pin selects the quiet mode and a high level selects continuous mode for the PCI950. The total low-pulse width on a start frame is eight clocks. After reset the PCI950 defaults to continuous mode.

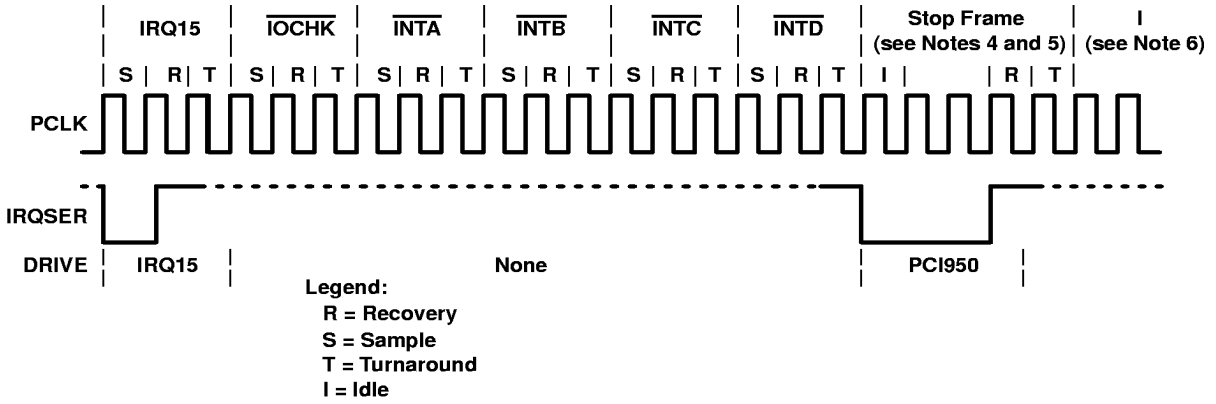
IRQ/data frame: The PCI950 is designed to decode a fixed length of 21 IRQ/data frames that are sampled in the following sequence: IRQ0, IRQ1, $\overline{\text{SMI}}$, IRQ3 through IRQ15, $\overline{\text{IOCHK}}$, $\overline{\text{INTA}}$, $\overline{\text{INTB}}$, $\overline{\text{INTC}}$, and $\overline{\text{INTD}}$.

Stop frame: After the completion of a start frame and 21 IRQ data frames, the PCI950 generates a stop frame. The pulse width of the stop pulse is determined by the status of the POLLMODE input pin sampled during the start frame.



NOTES: 2. Start frame is eight clocks in duration.
3. Slave or host initiated: POLLMODE is level dependent.

Figure 1. IRQSER Start-Frame Timing



NOTES: 4. The PCI950 stop pulse is two or three clocks in duration.
5. There may be none, one, or more idle states during the stop frame.
6. When the PCI950 is in continuous mode, there are 17 idle states between the stop frame and the start frame.

Figure 2. IRQSER Stop-Frame Timing

functional description (continued)

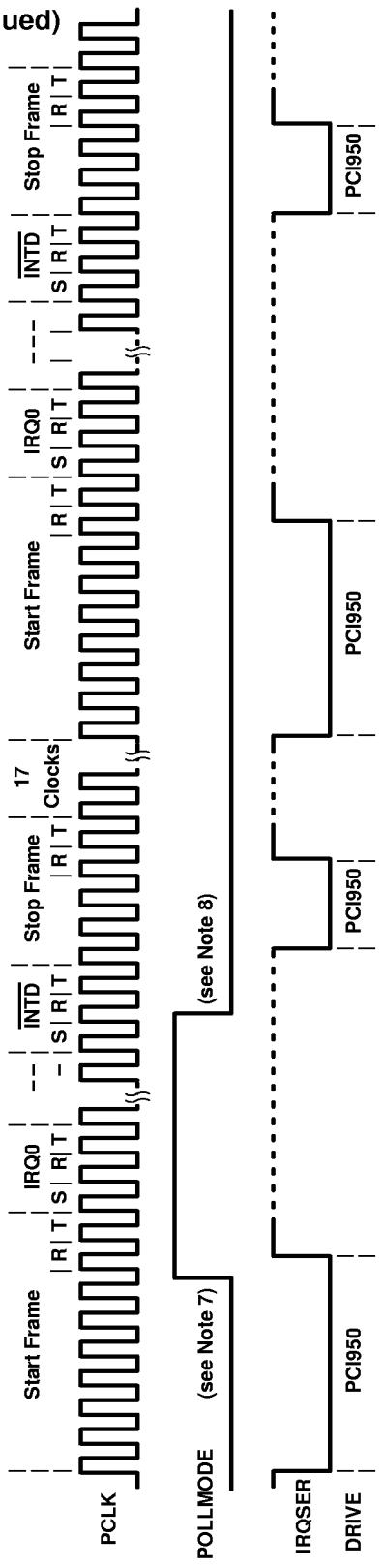
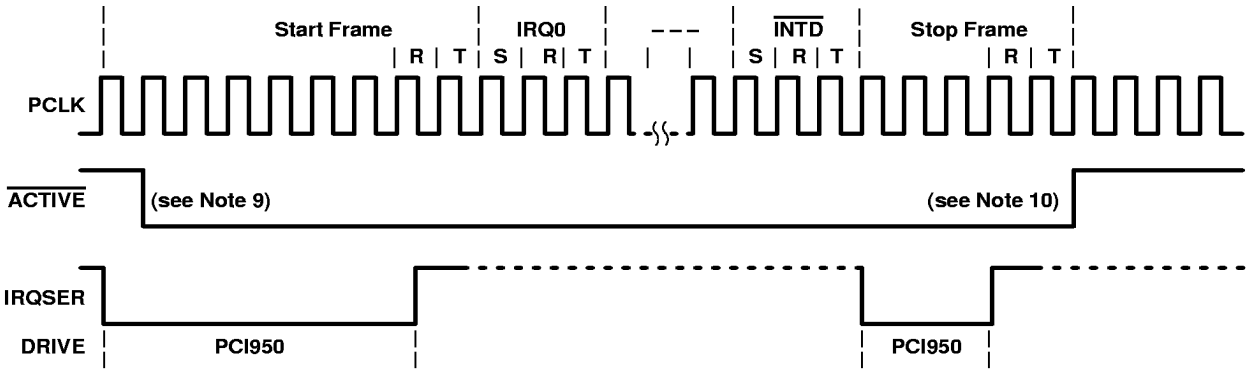


Figure 3. POLLMODE Level Change During an IRQSER Cycle

NOTES: 7. When the POLLMODE input level changes before the rising edge of the start frame, then the stop-frame width in the current IRQSER cycle reflects the change in mode.
8. Any change in the POLLMODE input level after the start frame is complete is reflected in the next IRQSER cycle.

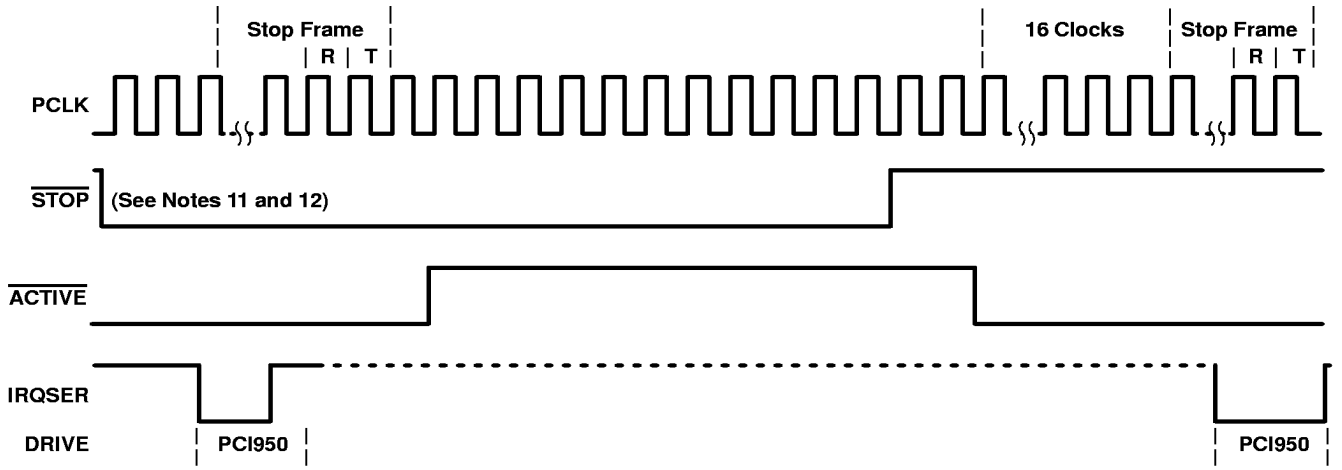
functional description (continued)



Legend:
R = Recovery
S = Sample
T = Turnaround

NOTES: 9. $\overline{\text{ACTIVE}}$ goes low one clock cycle after the beginning of the PCI950 start pulse.
10. $\overline{\text{ACTIVE}}$ is set high two clock pulses after the PCI950 stop pulse.

Figure 4. $\overline{\text{ACTIVE}}$ Output Timing During Quiet Mode



Legend:
R = Recovery
T = Turnaround

NOTES: 11. $\overline{\text{STOP}}$ can only be used to insert idle states in continuous mode.
12. The recommended sequence for using $\overline{\text{SHUTD}}$ is to:
A. Assert $\overline{\text{STOP}}$.
B. Ensure that $\overline{\text{ACTIVE}}$ is not asserted.
C. Assert $\overline{\text{SHUTD}}$.

Figure 5. Using $\overline{\text{STOP}}$ During Continuous Mode

APPLICATION INFORMATION

system-level implementation

A typical PCI950 system implementation is shown in Figure 6. The PCI950 allows software access to interrupts that may not exist on the periphery of the PC Card controller, thus increasing the overall interrupt resources that can be utilized.

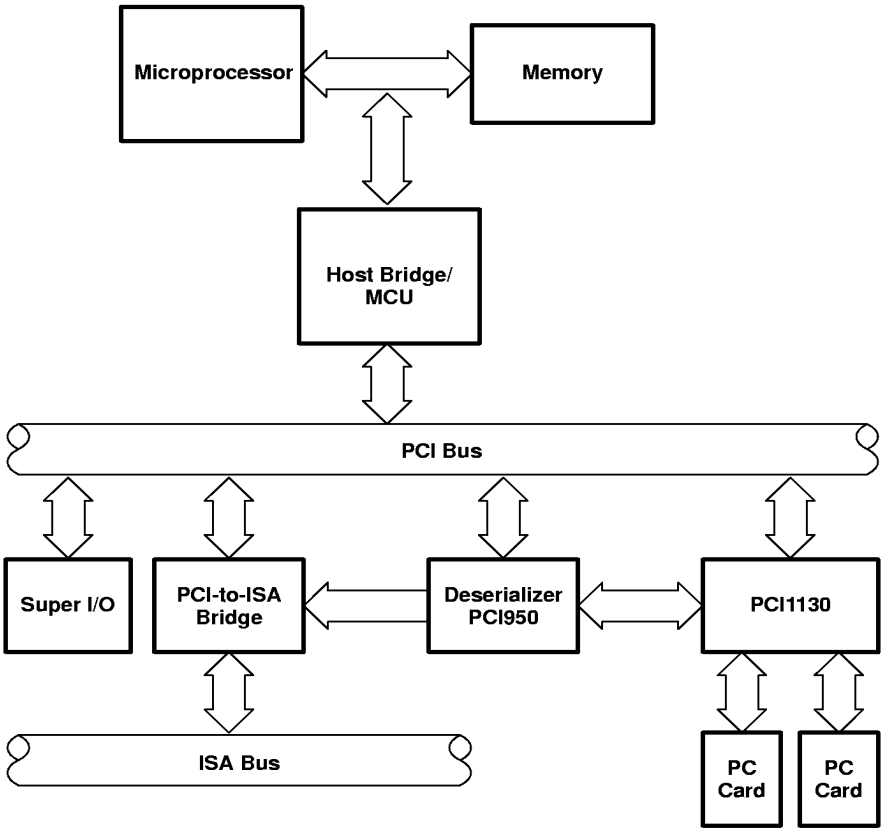


Figure 6. Typical System Installation

absolute maximum ratings over operating temperature ranges (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 6 V
Input voltage range, V_I . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 13) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 14) . . . . . ±20 mA
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Virtual junction temperature, T_J . . . . . 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 13. Applies to external input and bidirectional buffers
14. Applies to external output and bidirectional buffers

recommended operating conditions (see Note 15)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Commercial	4.75	5	5.25	V
V_{IH}‡	High-level input voltage		2		V_{CC}	V
V_{IL}‡	Low-level input voltage		0		0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O§	Output voltage		0		V_{CC}	V
t_t	Input transition time [rise time (t_r) and fall time (t_f), see Figure 7]		0		25	ns
T_A	Operating ambient temperature range		0	25	70	°C
T_J¶	Virtual junction temperature		0	25	115	°C

‡ Applies to external inputs and bidirectional buffers without hysteresis
§ Applies to external output buffers
¶ These junction temperatures reflect simulation conditions. The customer is responsible for verifying junction temperature.
NOTE 15: Unused pins (input or I/O) must be forced or tied high or low to prevent them from floating.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		PINS	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	PCI#	I_{OH} = −2 mA	2.4		V
		Standard	I_{OH} = −4 mA	2.1		
V_{OL}	Low-level output voltage	PCI#	I_{OL} = 6 mA		0.55	V
		Standard	I_{OL} = 4 mA		0.5	
I_{OZL}	3-state output, high-impedance state current	Output pins	V_I = GND		−10	µA
I_{OZH}	3-state output, high-impedance state current	Output pins	V_I = V_{CC}		10	µA
I_{IL}	Low-level input current	Input pins	V_I = GND		−1	µA
		I/O pins‖	V_I = GND		−10	
I_{IH}	High-level input current	Input pins	V_I = V_{CC}		1	µA
		I/O pins‖	V_I = V_{CC}		10	

PCI pins are $\overline{INTA}$, $\overline{INTB}$, $\overline{INTC}$, $\overline{INTC}$, and SERIRQ.
‖ For I/O pins, input leakage (I_{IL} and I_{IH}) includes I_{OZ} leakage of the disabled output.

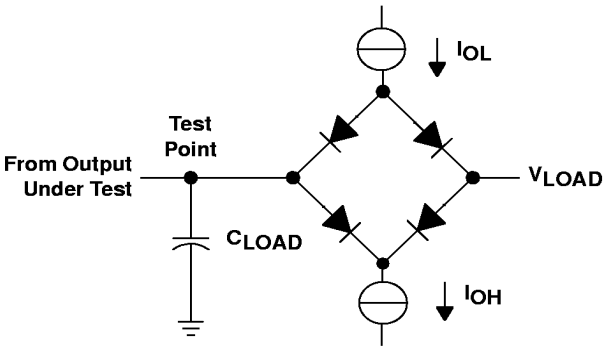
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT PARAMETERS

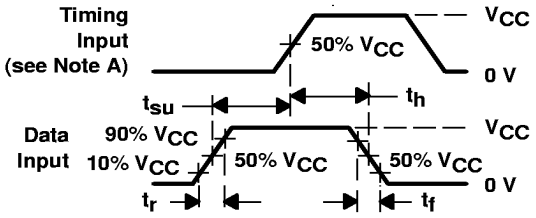
TIMING PARAMETER		C_{LOAD}† (pF)	I_{OL} (mA)	I_{OH} (mA)	V_{LOAD} (V)
t_{en}	t_{PZH}	50	8	–8	0
	t_{PZL}				3
t_{dis}	t_{PHZ}	50	8	–8	1.5
	t_{PLZ}				
t_{pd}		50	8	–8	‡

† C_{LOAD} includes the typical load-circuit distributed capacitance.

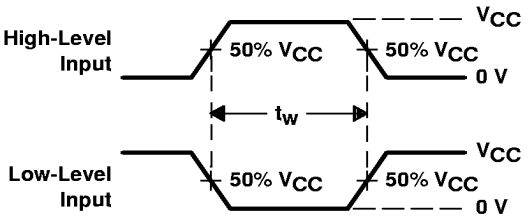
‡ $\frac{V_{LOAD} - V_{OL}}{I_{OL}}$ = 50 Ω, where V_{OL} = 0.6 V, I_{OL} = 8 mA



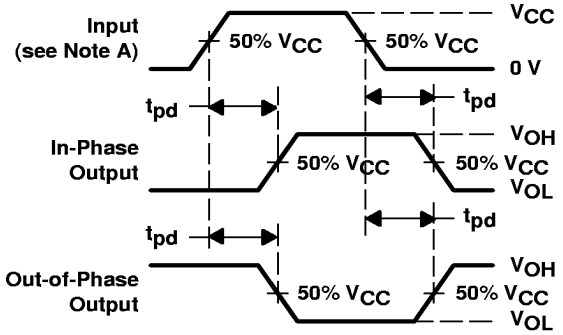
LOAD CIRCUIT



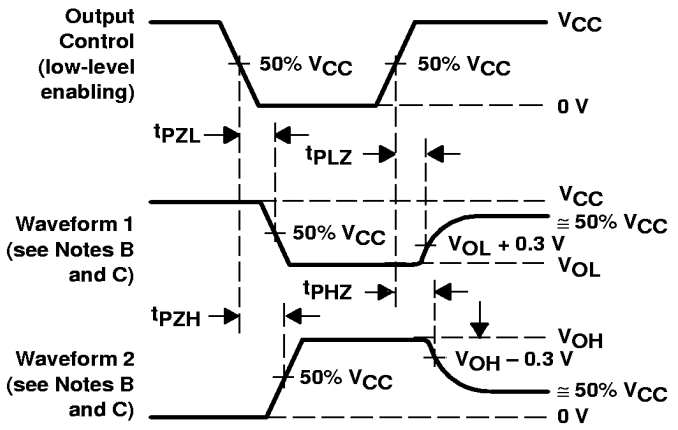
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



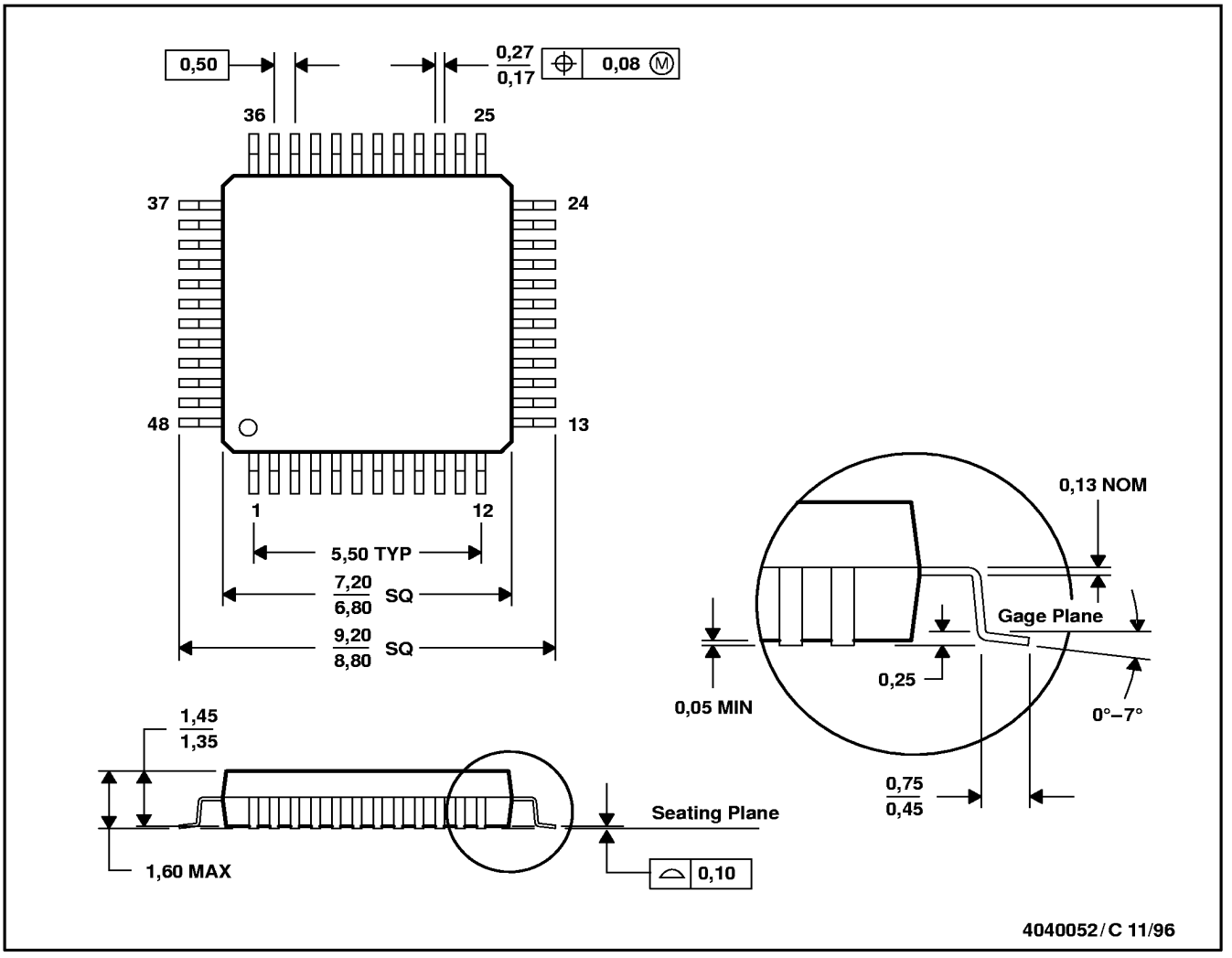
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, t_r = 6 ns.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. For t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are measured values.

Figure 7. Load Circuit and Voltage Waveforms

MECHANICAL DATA

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026