## ProASIC ${ }^{\text {TM }}$ 500K Family

## Features and Benefits

## High Capacity

- 98,000 to 1.1 Million System Gates
- 14 k to 138 k Bits of Two-Port SRAM
- 210 to 623 User I/Os


## Performance

- 33 MHz PCI 32-Bit
- Internal System Performance up to 250 MHz
- External System Performance up to 100 MHz


## Low Power

- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small Efficient Logic Cells

High Performance Routing Hierarchy

- Ultra Fast Local Network
- Efficient Long Line Network
- High Speed Bus Network
- High Performance Global Network


## Nonvolatile and Reprogrammable Flash Technology

- Live at Power-Up
- No Configuration Boot Device Required
- Retains Programmed Design During Power-Down/ Power-Up Cycles


## $1 / 0$

- Mixed 2.5/3.3 Volt Support
- 3.3V, 33 MHz PCI Compliance (PCI Revision 2.2)
- Individually Selectable 2.5 V or 3.3 V I/0s and Slew Rate ( 25,50 , and $100 \mathrm{~mA} / \mathrm{nsec}$ )


## Secure Programming

- Security Bit Prevents Read Back of Programming Bit Stream


## Standard FPGA and ASIC Design FIow

- Flexibility to Choose Vendor-Specific Front-End Tools
- Provide Efficient Design Through Front-End Timing and Gate Optimization


## ISP Support

- In-System Programming (ISP) with Silicon Sculptor and Silicon Explorer II


## Embedded Memory Netlist Generator for SRAMs and FIFOs

- Ensures Optimal Usage of Embedded Memory Blocks
- Up to 133 MHz Synchronous and Asynchronous Operation


## JTAG Support

- IEEE Std. 1149.1 (JTAG) Compliant

Individual ProASIC Device ID

- Control and Restrict IP Delivery to Individual ProASIC Device


## ProASIC Product Profile

| Device | A500K050 | A500K130 | A500K180 | A500K270 | A500K350 | A500K440 | A500K510 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum System Gates | 98,000 | 287,000 | 369,000 | 473,000 | 638,000 | 956,000 | $1,100,000$ |
| Typical Gates | 43,000 | 105,000 | 150,000 | 215,000 | 280,000 | 350,000 | 410,000 |
| Maximum Flip-Flops | 5,376 | 12,800 | 18,432 | 26,880 | 34,816 | 43,776 | 51,200 |
| Embedded RAM Bits | 14 k | 46 k | 55 k | 65 k | 74 k | 124 k | 138 k |
| Embedded RAM Blocks (256 X 9) | 6 | 20 | 24 | 28 | 32 | 54 | 60 |
| Logic Tiles | 5,376 | 12,800 | 18,432 | 26,880 | 34,816 | 43,776 | 51,200 |
| Global Clocks | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Maximum User I/Os | 210 | 312 | 368 | 446 | 496 | 570 | 623 |
| JTAG | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| PCI | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Package (by Pin Count) | 208 | 208 | 208 | 208 |  |  |  |
| PQFP | 272 | 272,456 | 456 | 456 |  | 580 | 580 |
| PBGA |  | 580 | 580 | 580 | 580 |  |  |
| FBGA |  |  |  |  |  |  |  |

## General Description

The ProASIC 500 K family combines the advantages of ASICs with the benefits of programmable devices through its nonvolatile Flash technology. ProASIC 500K devices make it possible to create high-density systems using existing ASIC or FPGA design flows and tools, shortening time-to-production. ASIC migration is not necessary for any volume because the family offers cost effective reprogrammable solutions, ideal for applications in the networking, telecom, computer, and consumer markets.

The ProASIC 500K family offers seven devices with 98 k to 1.1M system gates and includes up to 138 k bits of embedded
two-port memory. These memory blocks include hardwired FIFO circuitry as well as circuits to generate or check parity. This minimizes external logic gate count and complexity while maximizing flexibility and utility.

Process Technology
The ProASIC 500K family achieves its non-volatility and reprogrammability through an advanced 4LM Flash-based $0.25 \mu$ channel length LVCMOS technology process. Standard CMOS design techniques are used to implement logic and control functions resulting in highly predictable performance and gate array compatibility.

## Ordering Information



## Product Plan

|  | Speed Grade |  | Application |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Std | -1* | C | I |
| A500K050 Device |  |  |  |  |
| 208-Pin Plastic Quad Flat Pack (PQFP) | $\checkmark$ | P | P | P |
| 272-Pin Plastic Ball Grid Array (PBGA) | $\checkmark$ | P | P | P |
| A500K130 Device |  |  |  |  |
| 208-Pin Plastic Quad Flat Pack (PQFP) | $\checkmark$ | P | P | P |
| 272-Pin Plastic Ball Grid Array (PBGA) | $\checkmark$ | P | P | P |
| 456-Pin Plastic Ball Grid Array (PBGA) | $\checkmark$ | P | P | P |
| A500K180 Device |  |  |  |  |
| 208-Pin Plastic Quad Flat Pack (PQFP) | $\checkmark$ | P | P | P |
| 456-Pin Plastic Ball Grid Array (PBGA) | $\checkmark$ | P | P | P |
| 580-Pin Fine Ball Grid Array (FBGA) | P | P | P | P |
| A500K270 Device |  |  |  |  |
| 208-Pin Plastic Quad Flat Pack (PQFP) | $\checkmark$ | P | P | P |
| 456-Pin Plastic Ball Grid Array (PBGA) | $\checkmark$ | P | P | P |
| 580-Pin Fine Ball Grid Array (FBGA) | P | P | P | P |
| A500K350 Device |  |  |  |  |
| 580-Pin Fine Ball Grid Array (FBGA) | P | P | P | P |
| A500K440 Device |  |  |  |  |
| 580-Pin Fine Ball Grid Array (FBGA) | P | P | P | P |
| A500K510 Device |  |  |  |  |
| 580-Pin Fine Ball Grid Array (FBGA) | P | P | P | P |

Contact your Actel sales representative for package availability.

| Applications: | $C=$ Commercial | Availability: $\quad \boldsymbol{V}=$ Limited Availability. Contact your Actel Sales representative for the latest |  |
| :--- | :--- | :--- | :--- |
|  | $I=$ Industrial |  | availability information. |
|  |  |  |  |
|  | Speed Grade: | $-1=T B D$ | $P$ |

Plastic Device Resources

|  | User I/Os |  |  |  |
| :--- | :---: | :---: | :---: | :---: |
| Device | PQFP <br> 208-Pin | PBGA <br> 272-Pin | PBGA <br> 456-Pin | FBGA <br> 580-Pin |
| A500K050 | 170 | 210 | - | - |
| A500K130 | 170 | 210 | 312 | - |
| A500K180 | 170 | - | 368 | 368 |
| A500K270 | 170 | - | 368 | 446 |
| A500K350 | - | - | - | 496 |
| A500K440 | - | - | - | 496 |
| A500K510 | - | - | - | 496 |

Package Definitions (Contact your Actel sales representative for product availability.)
$P Q F P=$ Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Ball Grid Array

## ProASIC 500K Architecture

The ProASIC 500K family utilizes a proprietary architecture that results in granularity comparable to gate arrays. Unlike SRAM-based FPGAs, ProASIC devices do not utilize look-up tables or architectural mapping during design. Instead, designs are directly synthesized to gates that streamline the design flow, increase design productivity, and eliminate dependencies on vendor-specific design tools.
The ProASIC 500 K device core consists of a Sea-of-Tiles ${ }^{\text {TM }}$ (Figure 1). Each tile (Figure 2) can be configured into a 3-input logic function (i.e. NAND gate, D-Flip-Flop, etc.) by programming the appropriate interconnect Flash switches, shown in Figure 3 on page 5. Gates and larger functions are connected together, utilizing the four levels of routing
hierarchy. Flash memory bits are distributed throughout each device providing non-volatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew clock distribution throughout the core. Maximum core utilization is possible for virtually any design.

The ProASIC 500 K devices also contain embedded two-port SRAM blocks that have built in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking. Table 2 on page 9 lists the 24 basic memory configurations.


Figure 1 - The ProASIC Device Architecture


## Figure 2 •Core Logic Tile



## Figure 3 • Flash Switch

## Routing Resources

The routing structure of the ProASIC 500 K devices is designed to provide high performance through routing flexibility. It is composed of four levels of hierarchical resources: ultra fast local resources, efficient long line resources, high speed bus resources, and high performance global networks.
The ultra fast local resources are high speed dedicated lines that allow the output of each tile to directly connect to every input of the eight surrounding tiles (Figure 4).
The efficient long line resources provide routing for longer distance and higher fanout connections. These resources vary in length (spanning 1,2 , or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC device (Figure 5 on page 6). Each tile can drive signals onto the efficient long line resources, and the resources can access every input of a tile. Active buffers are inserted automatically by the ASICmaster software to limit the effects of loading due to distance and fanout.

The high speed bus resources span across the entire device with minimal delay and are used to route very long or very high fanout nets. These resources run vertically and horizontally, and provide multiple access to each group of tiles throughout the device (Figure 6 on page 6).
The high performance global networks are low skew, high fanout nets that are accessible from four dedicated pins or from internal logic (Figure 7 on page 7). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be used hierarchically, with signals accessing every input on all tiles.


Figure 4 - Ultra Fast Local Resources

## Acte!



Figure 5-Efficient Long Line Resources


Figure 6 • High Speed Bus Resources


Figure 7 • High Performance Global Network

## Input/Output Blocks

To meet the needs of complex system designs, the ProASIC 500 K family offers devices with a large number of I/0 pins, with the A500K510 device offering up to 623 user I/0 pins. If the I/0 pad is powered at 3.3 V , each $\mathrm{I} / 0$ can be selectively configured at 2.5 V and 3.3 V compliant threshold levels. Table 1 shows the various supply voltage configurations available in the ProASIC devices. Figure 8 illustrates I/0 interfaces with other devices. All I/Os also include an ESD protection circuit. Each I/O is tested according to the following models:

```
Human Body Model (HBM)
1500V
    (Per Mil Std 883 Method 3015)
Machine Model
200V
```

Table 1 • ProASIC Power Supply Voltages

| $\mathrm{V}_{\text {DDP }}$ | 2.5 V | 3.3 V |
| :--- | :--- | :---: |
| Input Tolerance | 2.5 V | $3.3 \mathrm{~V}, 2.5 \mathrm{~V}$ |
| Output Drive | 2.5 V | $3.3 \mathrm{~V}, 2.5 \mathrm{~V}$ |

Note: $\quad V_{D D L}$ is always 2.5 V .
The I/0 pads are fully configurable to provide the maximum flexibility and speed. Each pad can be configured as an input, an output, a three-state driver, or a bi-directional buffer (Figure 9). I/0 pads configured as inputs have the following features:

- Individually selectable 2.5 V or 3.3 V compliant threshold levels ${ }^{1}$
- Optional pull-up resistor

I/O pads configured as outputs have the following features:

- Individually selectable 2.5 V or 3.3 V compliant output signals ${ }^{1}$
- 3.3 V PCI compliant
- Ability to drive LVTTL and LVCMOS levels
- Selectable drive strengths
- Selectable slew rates $(25 \mathrm{~mA} / \mathrm{s}, 50 \mathrm{~mA} / \mathrm{s}, 100 \mathrm{~mA} / \mathrm{s})$
- Three-state enable

I/O pads configured as bi-directional buffers have the following features:

- Individually selectable 2.5 V or 3.3 V compliant output signals and threshold levels ${ }^{1}$
- 3.3V PCI compliant
- Ability to drive LVTTL and LVCMOS levels
- Optional pull-up resistor

[^0]- Selectable drive strengths
- Selectable slew rates ( $25 \mathrm{~mA} / \mathrm{s}, 50 \mathrm{~mA} / \mathrm{s}, 100 \mathrm{~mA} / \mathrm{s}$ )
- Three-state enable


Figure 8 - I/O Interfaces


Figure 9 • I/O Block Schematic Representation

## User Security and Traceability ${ }^{2}$

The ProASIC 500K devices have a read-protect bit that, once programmed, prevents the programmed contents from being read from the part. To clear the read-protect bit, the entire part must be erased. This capability lets you secure the programmed design and prevent it from being read back and duplicated. For traceability a 12 -character alphanumeric user part number field allows the user to assign a user part ID, which can subsequently be read back by the programmer.

[^1]
## Embedded Memory Floorpian

The embedded memory is located across the top of the device (see Figure 1 on page 4). Depending upon the device, 6 to 60 ( 256 x 9 ) blocks of memory are available to support a variety of possible memory configurations. Each block can be programmed as an independent memory or combined, using dedicated memory routing resources, to form larger and more complex memories.

## Embedded Memory Configurations

The embedded memory in the ProASIC 500K family offers great flexibility in memory configuration. Whereas other programmable vendors typically provide single port memories that can be transformed into a two-port memory at the loss of half the memory, each ProASIC block is designed and optimized as a two-port memory (1rlw). This provides 138 k total memory bits for two-port and single port memory usage in the A500K510 device.

Each memory can be configured as a FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports (Table 2). However, multiple write ports are not supported. Additional characteristics include programmable FIFO flags and selectable depth, and parity check and generation. Figure 10 and Figure 11 on page 10
show the block diagram of the basic SRAM and FIFO blocks. These memories are designed to operate at up to 133 MHz when operated individually. Each block contains a 256 word deep by 9 -bit wide (1r, 1w) memory. The memory blocks, shown in Figure 12 on page 11, may be combined in parallel to form wider memories or stacked to form deeper memories. This provides optimal bit widths of 9 ( 1 block), 18,36 , and 72 , and optimal depths of $256,572,768$, and 1024. Refer to the ProASIC Macro Library Guide for more information.

Figure 13 on page 11 shows an example of optimal memory usage. Three memories have been compiled with various widths and depths using 10 blocks and consuming all 23,040 bits. Figure 14 on page 11 shows an example of doubling up memory to create extra read ports. In this example, 10 out of 60 blocks of the A 500 K 510 are fully used, but yield an effective 6,912 bits of multiple port memories. The MEMORYmaster ${ }^{\text {TM }}$ software facilitates an easy means of building wider and deeper memories for optimal memory usage.

Table 2 • Basic Memory Configurations

| Type | Write Access | Read Access | Parity | Library Cell Name |
| :--- | :--- | :--- | :--- | :--- |
| RAM | Asynchronous | Asynchronous | Checked | RAM256x9AA |
| RAM | Asynchronous | Asynchronous | Generated | RAM256x9AAP |
| RAM | Asynchronous | Synchronous Transparent | Checked | RAM256xAST |
| RAM | Asynchronous | Synchronous Transparent | Generated | RAM256xASTP |
| RAM | Asynchronous | Synchronous Pipelined | Checked | RAM256x9ASR |
| RAM | Asynchronous | Synchronous Pipelined | Generated | RAM256x9ASRP |
| RAM | Synchronous | Asynchronous | Checked | RAM256x9SA |
| RAM | Synchronous | Asynchronous | Generated | RAM256xSAP |
| RAM | Synchronous | Synchronous Transparent | Checked | RAM256x9SST |
| RAM | Synchronous | Synchronous Transparent | Generated | RAM256x9SSTP |
| RAM | Synchronous | Synchronous Pipelined | Checked | RAM256x9SSR |
| RAM | Synchronous | Synchronous Pipelined | Generated | RAM256x9SSRP |
| FIFO | Asynchronous | Asynchronous | Checked | FIFO256xAA |
| FIFO | Asynchronous | Asynchronous | Generated | FIFO256x9AAP |
| FIFO | Asynchronous | Synchronous Transparent | Checked | FIFO256xAST |
| FIFO | Asynchronous | Synchronous Transparent | Generated | FIFO256x9ASTP |
| FIFO | Asynchronous | Synchronous Pipelined | Checked | FIFO256x9ASR |
| FIFO | Asynchronous | Synchronous Pipelined | Generated | FIFO256x9ASRP |
| FIFO | Synchronous | Asynchronous | Checked | FIFO256x9SA |
| FIFO | Synchronous | Asynchronous | Generated | FIFO256xSAP |
| FIFO | Synchronous | Synchronous Transparent | Checked | FIFO256x9SST |
| FIFO | Synchronous | Synchronous Transparent | Generated | FIFO256x9SSTP |
| FIFO | Synchronous | Synchronous Pipelined | Checked | FIFO256x9SSR |
| FIFO | Synchronous | Synchronous Pipelined | Generated | FIFO256x9SSRP |



Figure 10 • Example SRAM Block Diagrams


Figure 11 • Basic FIFO Block Diagrams
$\qquad$


Figure 12 • A500K510 Memory Block Architecture
Tordal Memory Blocks Used = 10 Width
Total Memory Bits = 23,040

Figure 13 • Memories with Different Width and Depth


Figure 14 • Multiport Memory Usage

## Design Environment

ProASIC devices are supported by Actel's ASICmaster and MEMORYmaster software, as well as third party CAE tools. Using the standard VHDL or Verilog HDL descriptions, no special HDL design techniques, as required by some FPGA vendors, are needed. This allows designers to use technology independent HDL code for ProASIC devices. This and the ProASIC design flow ensure a seamless transition to an ASIC, should production volumes warrant a migration to a gate array or a standard cell product (Figure 15).

MEMORYmaster automatically generates memories from inputs given by the designer. The designer can select the depth and width, usage of parity generation or check, and synchronous or asynchronous functionality of the ports. If it is a synchronous read port, the designer can choose whether the output is pipelined or transparent. MEMORYmaster allows any bit width up to 252 (for the A500K270 device), but if an intermediate bit width is chosen, such as 16 bits, the remaining two bits are no longer accessible for other
memories. MEMORYmaster also enables optimal memory stacking in 256 word increments. However, any word depth may be compiled for up to 7,168 words.

Place and route is performed by Actel's ASICmaster software. Available for Sun0S ${ }^{\circledR}$, Solaris ${ }^{\circledR}$, $\mathrm{HP}^{\circledR}$, and Windows $\mathrm{NT}^{\circledR}$, it accepts standard netlists in Verilog, VHDL, and in EDIF 2.0.0, performs place and route of the design into the selected device, and provides post layout delay information for back annotation simulation or static timing analysis. The ASICmaster software also contains very powerful interactive layout capabilities for the experienced user.
Once the design is finalized, the programming bitstream is downloaded into the device programmer for ProASIC part programming. ProASIC 500 K devices can be programmed with the Silicon Sculptor programmer. In-system programming is also available using the Silicon Sculptor programmer or Silicon Explorer II.


Figure 15 • Design Flow

## Package Thermal Characteristics

The ProASIC 500 K family is available in a number of package types. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

The ability of a package to conduct heat away from the silicon, through the package, to the surrounding air is expressed in terms of thermal resistance. This junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja $\left(\Theta_{\mathrm{j}}\right)$. The lower this thermal resistance, the easier it is for the package to dissipate heat.
The maximum allowed power (P) for a package is a function of the maximum junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ), the maximum ambient operating temperature $\left(\mathrm{T}_{\mathrm{A}}\right)$, and the
junction-to-ambient thermal resistance $\Theta_{\mathrm{j} \mathrm{a}}$. Maximum junction temperature is the maximum temperature on the active surface of the IC and is $110^{\circ} \mathrm{C}$. P is defined as:

$$
P=\frac{T_{J}-T_{A}}{\Theta_{j a}}
$$

$\Theta_{\mathrm{ja}}$ is a function of the rate of airflow in contact with the package, in linear feet per minute (lfpm). When the estimated power consumption exceeds the maximum allowed power, other means of cooling must be used, such as increasing the airflow rate.

| Package Type | Pin Count | $\Theta_{\mathbf{j c}}$ | $\Theta_{\mathbf{j a}}$ Still Air | $\Theta_{\mathbf{j a}} \mathbf{3 0 0} \mathbf{~ t t / m i n}$ | Units |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Plastic Quad Flat Pack (PQFP) | 208 | 3.5 | 20 | 17 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Plastic Ball Grid Array (PBGA) | 272 | 3 | 20 | 16.5 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Plastic Ball Grid Array (PBGA) | 456 | 3 | 18 | 14.5 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## Calculating Power Dissipation

ProASIC device power is calculated in the same manner as LVCMOS gate arrays and includes both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. ASICmaster provides an automatic power calculator that can be used to quickly and easily calculate power dissipation. Power dissipation can also be calculated using the following formula:

$$
\mathrm{P}=\mathrm{V}_{\mathrm{DD}} * \mathrm{I}_{\mathrm{DD}}
$$

where:

$$
\mathrm{I}_{\mathrm{DD}}=\mathrm{I}_{\mathrm{STATIC}}+\mathrm{I}_{\text {OUTPUT }}+\mathrm{I}_{\mathrm{LOGIC}}
$$

and

$$
\mathrm{I}_{\text {STATIC }}=\mathrm{I}_{\text {STATIC CORE }}+\mathrm{I}_{\text {STATIC } / / 0}
$$

$\mathrm{I}_{\text {OUTPUT }}$ is the current due to the outputs switching.
$\mathrm{I}_{\text {LOGIC }}$ is the current due to the internal logic signals switching.
The static power ( $\mathrm{I}_{\text {STATIC }}$ ) is the amount of current drawn when no inputs are switching. This is equal to the Quiescent Supply Current $\mathrm{I}_{\mathrm{DDQ}}$ specified under DC Electrical Specifications beginning on page 16 .
Active power includes both the current due to outputs switching and the current due to internal logic signals switching.

$$
I_{\text {OUTPUT }}=\sum_{i=1}^{n}\left(C_{i} \cdot V_{i} \cdot f_{i}+I_{D C i}\right)
$$

where:
$\mathrm{C}_{\mathrm{i}} \quad=$ Capacitance on the $i$ th output pad
$\mathrm{V}_{\mathrm{i}} \quad=$ Voltage swing on the $i$ th output pad
$\mathrm{f}_{\mathrm{i}} \quad=$ Switching frequency on the $i$ th output pad
$\mathrm{n} \quad=$ Number of outputs
$\mathrm{I}_{\mathrm{DCi}}=$ Average DC load on each pad, if any
In most cases $\mathrm{I}_{\text {OUTPUT }}$ can be approximated by the following formula, measured in mA :

$$
\mathrm{I}_{\text {OUTPUT }}=\mathrm{n} * \mathrm{C}_{\text {typ }} * \mathrm{~V} * \mathrm{f}_{\text {avg }}
$$

where:
$\mathrm{n} \quad=$ Number of active outputs
$\mathrm{C}_{\text {typ }}=$ Typical capacitance load on an output
$\mathrm{V} \quad=$ Average voltage swing
$\mathrm{f}_{\text {avg }}=$ Average switching frequency of the outputs. Typically this is less than $25 \%$ of the clock frequency
$\mathrm{I}_{\text {LOGIC }}$ is represented by this formula, measured in mA:

$$
\mathrm{I}_{\mathrm{LOGIC}}=\mathrm{I}_{\mathrm{E}} * \mathrm{G} * \mathrm{f} * \mathrm{~F}
$$

where:

$$
\begin{aligned}
\mathrm{I}_{\mathrm{E}} & = \\
& \text { Effective } \mu \mathrm{A} \text { per gate per MHz of the Actel parts. } \\
& \text { For the ProASIC products the value is } 1.2 \\
\mathrm{G} & =\text { Number of gates used in the design, in thousands }
\end{aligned}
$$

$\mathrm{f} \quad=$ Operating frequency in MHz
$\mathrm{F} \quad=$ Fraction of devices active on each clock edge. F varies for different designs, but 0.15 is a conservative and commonly used value.

For an A500K130 design that has 47,000 used gates, 20 memory blocks, 150 active outputs, an average load of 20 pF , and a 66 MHz clock, resulting in an average switching frequency of 16.5 MHz , the power calculation appears below.

| $\mathrm{I}_{\text {OUTPUT }}$ | $=150 * 20 * 10^{-12} * 3.6 * 16.5 * 10^{6} \mathrm{~mA}$ |
| :--- | :--- |
|  | $=140 \mathrm{~mA}$ |
| $\mathrm{P}_{\text {OUTPUT }}$ | $=3.6 \mathrm{~V} * 140 \mathrm{~mA}=.5 \mathrm{~W}$ |
| $\mathrm{I}_{\text {LOGIC }}$ | $=1.2 * 47 * 66 * 0.15 \mathrm{~mA}$ |
|  | $=558 \mathrm{~mA}$ |

Therefore
$\mathrm{I}_{\text {LOGIC }} \quad=558 \mathrm{~mA}$
$\mathrm{P}_{\text {Logic }} \quad=2.75 \mathrm{~V} * 558 \mathrm{~mA}$

$$
=1.5 \mathrm{~W}
$$

Assumptions .5 k gates per 256 x 9 block
$\mathrm{I}_{\text {memory }} \quad=1.2 * .5 * 66 * .15 * 20 \mathrm{~mA}$ $=118 \mathrm{~mA}$

$$
\begin{array}{ll}
\mathrm{P}_{\text {memory }} & =2.75 \mathrm{~V} * 143 \mathrm{~mA}=.326 \\
\mathrm{P} & =1.5 \mathrm{~W}+.5 \mathrm{~W}+.32 \mathrm{~W}=2.32 \mathrm{~W}
\end{array}
$$

$\mathrm{I}_{\text {STATIC CORE }}$ and $\mathrm{I}_{\text {STATIC }}$ I/O are not included in this calculation.


Figure 16 - Power Consumption of a 500 K Device

## Operating Conditions

## Absolute Maximum Ratings

| Parameter | Condition | Minimum | Maximum | Units |
| :--- | :---: | :---: | :---: | :---: |
| Supply Voltage Core (V VDL ) |  | -0.3 | 3.0 | V |
| Supply Voltage IO Ring (VDP) |  | -0.3 | 4.0 | V |
| DC Input Voltage |  | -0.3 | $\mathrm{~V}_{\mathrm{DDP}}+0.3$ | V |
| PCI DC Input Voltage |  | -0.5 | $\mathrm{~V}_{\mathrm{DDP}}+0.5$ | V |
| DC Input Clamp Current (IIK) | $\mathrm{V}_{\mathrm{IN}}<0$ or $>\mathrm{V}_{\mathrm{DDP}}$ | -10 | +10 | mA |

Note: $\quad$ Stresses beyond those listed under Absolute Maximum ratings can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can adversely affect device reliability. Operation of the device at these conditions or any others beyond those listed in the Recommended Operating Conditions table on page 15 is not implied.

Temperature Maximums

| Parameter | Min. | Max. | Units | Program <br> Retention |
| :--- | :---: | :---: | :---: | :---: |
| Storage Temperature | -65 | +150 | ${ }^{\circ} \mathrm{C}$ | N/A |
| Storage Temperature—Programmed | -65 | +110 | ${ }^{\circ} \mathrm{C}$ | 20 years |

Programming Limits and Recommended Operating Conditions

| Product Grade | Programming <br> Cycles | Program <br> Retention | Junction Temperature |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | $0^{\circ} \mathrm{C}$ | $110^{\circ} \mathrm{C}$ |
| Commercial | 50 Max. |  |  |
| Industrial | 500 | 20 years | $-40^{\circ} \mathrm{C}$ | $110^{\circ} \mathrm{C}$ |

## Supply Voltages

| Mode | $\mathbf{V}_{\text {DDL }}$ | $\mathbf{V}_{\text {DDP }}$ | $\mathbf{V}_{\mathbf{P P}}$ | $\mathbf{V}_{\text {PN }}$ |
| :---: | :---: | :---: | :---: | :---: |
| Single Voltage | 2.5 V | 2.5 V | $2.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{PP}} \leq 16.5 \mathrm{~V}$ | $-12 \mathrm{~V} \leq \mathrm{V}_{\mathrm{PN}} \leq 0 \mathrm{~V}$ |
| Mixed Voltage | 2.5 V | 3.3 V | $3.3 \mathrm{~V} \leq \mathrm{V}_{\mathrm{PP}} \leq 16.5 \mathrm{~V}$ | $-12 \mathrm{~V} \leq \mathrm{V}_{\mathrm{PN}} \leq 0 \mathrm{~V}$ |

Recommended Operating Conditions

| Parameter | Symbol | Limits |
| :---: | :---: | :---: |
| Commercial |  |  |
| DC Supply Voltage (2.5V I/Os) | $\mathrm{V}_{\text {DDL }}$ \& $\mathrm{V}_{\mathrm{DDP}}$ | 2.3 V to 2.7V |
| DC Supply Voltage (3.3V, 2.5 V I/Os) | $V_{\text {DDP }}$ <br> $V_{\text {DDL }}$ | $\begin{aligned} & 3.0 \mathrm{~V} \text { to } 3.6 \mathrm{~V} \\ & 2.3 \mathrm{~V} \text { to } 2.7 \mathrm{~V} \end{aligned}$ |
| Operation Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ |
| Operation Junction Temperature (maximum) | $\mathrm{T}_{J}$ | $\leq 110^{\circ} \mathrm{C}$ |
| Industrial |  |  |
| DC Supply Voltage (2.5V I/Os) | $\mathrm{V}_{\text {DDL }}$ \& $\mathrm{V}_{\mathrm{DDP}}$ | 2.3 V to 2.7V |
| DC Supply Voltage (2.5V, 3.3V I/Os) | $V_{\text {DDP }}$ <br> $V_{\text {DDL }}$ | $\begin{aligned} & \hline 3.0 \mathrm{~V} \text { to } 3.6 \mathrm{~V} \\ & 2.3 \mathrm{~V} \text { to } 2.7 \mathrm{~V} \end{aligned}$ |
| Operation Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ |
| Operation Junction Temperature (maximum) | $\mathrm{T}_{J}$ | $\leq 110^{\circ} \mathrm{C}$ |

DC Electrical Specifications ( $\mathrm{V}_{\text {DDP }}=2.5 \mathrm{~V}$ )

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {DDR }} \mathrm{V}_{\text {DDL }}$ | Supply Voltage |  | 2.3 |  | 2.7 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Output High Voltage High Drive <br> Low Drive | $\begin{aligned} & \mathrm{l}_{\mathrm{OH}}=-2.0 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-4.0 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-8.0 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-1.0 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-2.0 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-4.0 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 2.1 \\ & 2.0 \\ & 1.7 \\ & 2.1 \\ & 2.0 \\ & 1.7 \end{aligned}$ |  |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Output Low Voltage High Drive <br> Low Drive | $\begin{aligned} & \mathrm{l}_{\mathrm{OL}}=5.0 \mathrm{~mA} \\ & \mathrm{l}_{\mathrm{OL}}=10.0 \mathrm{~mA} \\ & \mathrm{l}_{\mathrm{OL}}=15.0 \mathrm{~mA} \\ & \mathrm{l}_{\mathrm{OL}}=2.0 \mathrm{~mA} \\ & \mathrm{l}_{\mathrm{OL}}=3.5 \mathrm{~mA} \\ & \mathrm{l}_{\mathrm{OL}}=5.0 \mathrm{~mA} \end{aligned}$ |  |  | $\begin{aligned} & 0.2 \\ & 0.4 \\ & 0.7 \\ & 0.2 \\ & 0.4 \\ & 0.7 \end{aligned}$ | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input High Voltage |  | 1.7 |  | $\mathrm{V}_{\text {DDP }}+0.3$ | V |
| $\mathrm{V}_{\text {IL }}$ | Input Low Voltage |  | -0.3 |  | . 7 | V |
| $\mathrm{I}_{\mathrm{IN}}$ | Input Current Input Current | with pull-up without pull-up | $\begin{aligned} & \hline-20 \\ & -10 \end{aligned}$ |  | $\begin{gathered} -100 \\ 10 \end{gathered}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {DDQ }}$ | Quiescent Supply Current | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {SS }}{ }^{\dagger}$ or $\mathrm{V}_{\text {DDL }}$ |  | 1.0 | 10 | mA |
| $\mathrm{I}_{\mathrm{Oz}}$ | 3-State Output Leakage Current | $\mathrm{V}_{\mathrm{OH}}=\mathrm{V}_{\mathrm{SS}}$ or $\mathrm{V}_{\mathrm{DDL}}$ | -10 |  | +10 | $\mu \mathrm{A}$ |
| IOSH | Output Short Circuit Current High High Drive Low Drive |  |  |  | $\begin{aligned} & -120 \\ & -100 \end{aligned}$ | mA |
| IOSL | Output Short Circuit Current Low High Drive Low Drive |  |  |  | $\begin{gathered} 100 \\ 30 \end{gathered}$ | mA |
| $\mathrm{C}_{1 / \mathrm{O}}$ | I/O Pad Capacitance |  |  |  | 8 | pF |
| $\mathrm{C}_{\text {CLK }}$ | Clock Input Pad Capacitance |  |  |  | 8 | pF |

Notes: All process conditions. Junction Temperature: -40 to $+110^{\circ} \mathrm{C}$.
$\dagger$ No pull-up resistor.

DC Electrical Specifications ( $V_{\text {DDP }}=\mathbf{3 . 3 V}$ )

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {DDP }}$ | Supply Voltage |  | 3.0 |  | 3.6 | V |
| $\mathrm{V}_{\text {DDL }}$ | Supply Voltage, Logic Array |  | 2.3 |  | 2.7 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Output High Voltage 3.3V I/O, High Drive 3.3V I/O, Low Drive | $\begin{aligned} & \mathrm{l}_{\mathrm{OH}}=-3.0 \mathrm{~mA} \\ & \mathrm{l}_{\mathrm{OH}}=-5.0 \mathrm{~mA} \\ & \mathrm{l}_{\mathrm{OH}}=-10.0 \mathrm{~mA} \\ & \mathrm{l}_{\mathrm{OH}}=-2.0 \mathrm{~mA} \\ & \mathrm{l}_{\mathrm{OH}}=-3.0 \mathrm{~mA} \\ & \mathrm{IOH}_{\mathrm{OH}}=-6.0 \mathrm{~mA} \end{aligned}$ | $\begin{gathered} V_{D D P}-0.2 \\ 0.9 * V_{D D P} \\ 2.4 \\ V_{D D P}-0.2 \\ 0.9 * V_{D D P} \\ 2.4 \end{gathered}$ |  |  | V |
|  | 2.5V I/O, High Drive <br> 2.5V I/O, Low Drive | $\begin{aligned} & \mathrm{l}_{\mathrm{OH}}=-0.5 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-1.0 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-2.0 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-0.5 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-1.0 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-2.0 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & \hline 2.1 \\ & 2.0 \\ & 1.7 \\ & 2.1 \\ & 2.0 \\ & 1.7 \end{aligned}$ |  |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Output Low Voltage 3.3V I/O, High Drive 3.3V I/O, Low Drive | $\begin{aligned} & \mathrm{I}_{\mathrm{OL}}=7.5 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OL}}=12.0 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OL}}=15.0 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OL}}=2.5 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OL}}=4.0 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OL}}=5.0 \mathrm{~mA} \end{aligned}$ |  |  | $\begin{gathered} 0.2 \\ 0.1 * V_{\mathrm{DDP}} \\ 0.4 \\ 0.2 \\ 0.1 * \mathrm{~V}_{\mathrm{DDP}} \\ 0.4 \end{gathered}$ | V |
|  | 2.5 V I/O, High Drive <br> 2.5V I/O, Low Drive | $\begin{aligned} \mathrm{I}_{\mathrm{OL}} & =7.5 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{OL}} & =15.0 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{OL}} & =24.0 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{OL}} & =2.5 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{OL}} & =5.0 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{OL}} & =8.0 \mathrm{~mA} \end{aligned}$ |  |  | $\begin{aligned} & \hline 0.2 \\ & 0.4 \\ & 0.7 \\ & 0.2 \\ & 0.4 \\ & 0.7 \end{aligned}$ | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input High Voltage <br> LVTTL/LVCMOS <br> 2.5V Mode |  | $\begin{gathered} 2 \\ 1.7 \end{gathered}$ |  | $\begin{aligned} & \mathrm{V}_{\mathrm{DDP}}+0.3 \\ & \mathrm{~V}_{\mathrm{DDP}}+0.3 \end{aligned}$ | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Input Low Voltage <br> LVTTL/LVCMOS <br> 2.5V Mode |  | $\begin{aligned} & -0.3 \\ & -0.3 \end{aligned}$ |  | $\begin{aligned} & 0.8 \\ & 0.7 \end{aligned}$ | V |
| $\mathrm{I}_{\mathrm{IN}}$ | Input Current <br> LVTTL/LVCMOS <br> LVTTL/LVCMOS | with pull-up without pull-up | $\begin{aligned} & -40 \\ & -10 \end{aligned}$ |  | $\begin{gathered} -200 \\ 10 \end{gathered}$ | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {DDQ }}$ | Quiescent Supply Current | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\text {SS }}{ }^{\dagger}$ or $\mathrm{V}_{\mathrm{DD}}$ |  | 1.0 | 10 | mA |

Notes: Refer to PCI Specifications Revision 2.2. for 3.3V high drive, high slew-rate output pads, and all 3.3V input/clock pads. $\dagger$ No pull-up resistor.

## DC Electrical Specifications ( $\left.V_{\text {DDP }}=3.3 \mathrm{~V}\right)$ (Continued)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {Oz }}$ | 3-State Output Leakage Current | $\mathrm{V}_{\mathrm{OH}}=\mathrm{V}_{\mathrm{SS}}{ }^{\dagger}$ or $\mathrm{V}_{\mathrm{DD}}$ | -10 |  | +10 | $\mu \mathrm{A}$ |
| IOSH | Output Short Circuit Current High <br> 3.3V I/O, High Drive <br> 3.3V I/O, Low Drive <br> 2.5V I/O, High Drive <br> 2.5V I/O, Low Drive |  |  |  | $\begin{aligned} & -200 \\ & -140 \\ & -100 \\ & -100 \end{aligned}$ | mA |
| IOSL | Output Short Circuit Current Low <br> 3.3V I/O, High Drive <br> 3.3V I/O, Low Drive <br> 2.5V I/O, High Drive <br> 2.5V I/O, Low Drive |  |  |  | $\begin{gathered} 160 \\ 50 \\ 160 \\ 50 \end{gathered}$ | mA |
| $\mathrm{C}_{\text {I/O }}$ | I/O Pad Capacitance |  |  |  | 8 | pF |
| $\mathrm{C}_{\text {CLK }}$ | Clock Input Pad Capacitance |  |  |  | 8 | pF |

Notes: Refer to PCI Specifications Revision 2.2. for 3.3V high drive, high slew-rate output pads, and all 3.3V input/clock pads. $\dagger$ No pull-up resistor.

## Timing Characteristics



Figure 17 • Tri-State Buffer Delays
Table 3 - Tri-State Buffer Delays
(Worst-Case Commercial Conditions, $V_{D D P}=3.0 \mathrm{~V}, V_{D D L}=2.3 \mathrm{~V}, 35 \mathrm{pF}$ load, $T_{J}=70^{\circ} \mathrm{C}$ )

| Macro Type | Description | Max <br> $t_{\text {DLH }}$ | $\begin{aligned} & \text { Max } \\ & \mathbf{t}_{\mathrm{DHL}} \end{aligned}$ | Max <br> $t_{\text {ENZH }}$ | Max <br> tenzl | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OTB33PH | $3.3 \mathrm{~V}, \mathrm{PCI}$ Output Current, High Slew Rate | 4.41 | 4.28 | 4.40 | 3.71 | ns |
| OTB33PN | 3.3V, PCI Output Current, Nominal Slew Rate | 4.91 | 6.08 | 4.90 | 5.46 | ns |
| OTB33PL | 3.3V, PCI Output Current, Low Slew Rate | 5.51 | 7.41 | 5.50 | 6.86 | ns |
| OTB33LH | 3.3V, Low Output Current, High Slew Rate | 6.23 | 6.90 | 6.24 | 6.09 | ns |
| OTB33LN | 3.3V, Low Output Current, Nominal Slew Rate | 6.98 | 9.63 | 6.98 | 9.26 | ns |
| OTB33LL | 3.3V, Low Output Current, Low Slew Rate | 7.80 | 12.56 | 7.80 | 12.28 | ns |
| OTB25HH | 2.5V, High Output Current, High Slew Rate | 7.15 | 3.73 | 7.15 | 3.48 | ns |
| OTB25HN | 2.5 V , High Output Current, Nominal Slew Rate | 7.54 | 5.41 | 7.54 | 5.14 | ns |
| OTB25HL | 2.5 V , High Output Current, Low Slew Rate | 8.45 | 6.66 | 8.45 | 6.38 | ns |
| OTB25LH | 2.5 V , Low Output Current, High Slew Rate | 10.77 | 5.74 | 10.76 | 5.37 | ns |
| OTB25LN | 2.5V, Low Output Current, Nominal Slew Rate | 11.54 | 8.60 | 11.52 | 8.35 | ns |
| OTB25LL | 2.5V, Low Output Current, Low Slew Rate | 12.39 | 11.37 | 12.38 | 11.12 | ns |
| OTB25LPHH | 2.5V, Low Power, High Output Current, High Slew Rate | 5.30 | 5.29 | 5.27 | 4.57 | ns |
| OTB25LPHN | 2.5V, Low Power, High Output Current, Nominal Slew Rate | 6.27 | 7.99 | 6.24 | 7.46 | ns |
| OTB25LPHL | 2.5V, Low Power, High Output Current, Low Slew Rate | 7.15 | 10.20 | 7.12 | 9.74 | ns |
| OTB25LPLH | 2.5 V , Low Power, Low Output Current, High Slew Rate | 7.74 | 9.02 | 7.71 | 8.10 | ns |
| OTB25LPLN | 2.5V, Low Power, Low Output Current, Nominal Slew Rate | 8.96 | 13.11 | 8.93 | 12.76 | ns |
| OTB25LPLL | 2.5V, Low Power, Low Output Current, Low Slew Rate | 10.24 | 17.72 | 10.21 | 17.38 | ns |

## Notes:

1. $t_{\text {DLH }}=$ Data-to-Pad HIGH
2. $t_{D H L}=$ Data-to-Pad LOW
3. $t_{E N Z H}=$ Enable-to-Pad, Z to HIGH
4. $t_{E N Z L}=$ Enable-to-Pad, Z to LOW



Figure 18 • Output Buffer Delays
Table 4 - Output Buffer Delays
(Worst-Case Commercial Conditions, $V_{D D P}=3.0 \mathrm{~V}, V_{D D L}=2.3 \mathrm{~V}, 35 \mathrm{pF}$ load, $T_{J}=70^{\circ} \mathrm{C}$ )

| Macro Type | Description | Max. $\mathbf{t}_{\text {DLH }}$ | Max. $_{\text {DHL }}$ | Units |
| :--- | :--- | :---: | :---: | :---: |
| OB33PH | 3.3V, PCI Output Current, High Slew Rate | 4.41 | 4.28 | ns |
| OB33PN | 3.3V, PCI Output Current, Nominal Slew Rate | 4.91 | 6.08 | ns |
| OB33PL | 3.3V, PCI Output Current, Low Slew Rate | 5.51 | 7.41 | ns |
| OB33LH | 3.3V, Low Output Current, High Slew Rate | 6.23 | 6.90 | ns |
| OB33LN | 3.3V, Low Output Current, Nominal Slew Rate | 6.98 | 9.63 | ns |
| OB33LL | 3.3V, Low Output Current, Low Slew Rate | 7.80 | 12.56 | ns |
| OB25HH | 2.5V, High Output Current, High Slew Rate | 7.15 | 3.73 | ns |
| OB25HN | 2.5V, High Output Current, Nominal Slew Rate | 7.54 | 5.41 | ns |
| OB25HL | 2.5V, High Output Current, Low Slew Rate | 8.45 | 6.66 | ns |
| OB25LH | 2.5V, Low Output Current, High Slew Rate | 10.77 | 5.74 | ns |
| OB25LN | 2.5V, Low Output Current, Nominal Slew Rate | 11.54 | 8.60 | ns |
| OB25LL | 2.5V, Low Output Current, Low Slew Rate | 12.39 | 11.37 | ns |
| OB25LPHH | 2.5V, Low Power, High Output Current, High Slew Rate | 5.30 | 5.29 | ns |
| OB25LPHN | 2.5V, Low Power, High Output Current, Nominal Slew Rate | 6.27 | 7.99 | ns |
| OB25LPHL | 2.5V, Low Power, High Output Current, Low Slew Rate | 7.15 | 10.20 | ns |
| OB25LPLH | 2.5V, Low Power, Low Output Current, High Slew Rate | 7.74 | 9.02 | ns |
| OB25LPLN | 2.5V, Low Power, Low Output Current, Nominal Slew Rate | 8.96 | 13.11 | ns |
| OB25LPLL | 2.5V, Low Power, Low Output Current, Low Slew Rate | 10.24 | 17.72 | ns |

Notes:

1. $t_{\text {DLH }}=$ Data-to-Pad HIGH
2. $t_{D H L}=$ Data-to-Pad LOW


## Figure 19 - Input Buffer Delays

## Table 5 • Input Buffer Delays

(Worst-Case Commercial Conditions, $V_{D D P}=3.0 \mathrm{~V}, V_{D D L}=2.3 \mathrm{~V}, T_{J}=70^{\circ} \mathrm{C}$ )

| Macro Type | Description | Max. <br> $\mathbf{t}_{\text {INYH }}$ | Max. <br> $\mathbf{t}_{\text {INYL }}$ | Units |
| :--- | :--- | :---: | :---: | :---: |
| IB25 | 2.5 V, CMOS Input Levels, No Pull-up Resistor | 2.26 | 0.70 | ns |
| IB25LP | 2.5 V, CMOS Input Levels, Low Power | 2.25 | 1.51 | ns |
| IB33 | 3.3 V, CMOS Input Levels, No Pull-up Resistor | 1.98 | 1.02 | ns |

Notes:

1. $t_{\text {INYH }}=$ Input Pad-to- $Y$ HIGH
2. $t_{\text {INYL }}=$ Input Pad-to-Y LOW

Table 6 • Global Input Buffer Delays
(Worst-Case Commercial Conditions, $V_{D D P}=3.0 \mathrm{~V}, V_{D D L}=2.3 \mathrm{~V}, T_{J}=70^{\circ} \mathrm{C}$ )

| Macro Type | Description | Max. <br> $\mathbf{t}_{\mathbf{I N Y H}}$ | Max. <br> $\mathbf{t}_{\mathbf{I N Y L}}$ | Units |
| :--- | :--- | :---: | :---: | :---: |
| GL25 | 2.5 V, CMOS Input Levels | 2.17 | 1.74 | ns |
| GL25LP | 2.5V, CMOS Input Levels | 2.38 | 2.37 | ns |
| GL33 | 3.3V, CMOS Input Levels | 3.97 | 1.17 | ns |
| GL25U | 2.5 V, CMOS Input Levels, with Pull-up Resistor | 2.17 | 1.74 | ns |
| GL25LPU | 2.5V, CMOS Input Levels, Low Power, with Pull-up Resistor | 2.38 | 2.37 | ns |
| GL33U | $3.3 V$, CMOS Input Levels, with Pull-up Resistor | 3.97 | 1.17 | ns |

Table 7 • Predicted Global Routing Delay*
(Worst-Case Commercial Conditions, $V_{D D P}=3.0 \mathrm{~V}, V_{D D L}=2.3 \mathrm{~V}, T_{J}=70^{\circ} \mathrm{C}$ )

| Parameter | Description | Max. | Units |
| :--- | :--- | :---: | :---: |
| $t_{\text {RCKH }}$ | Input Low to High (fully loaded row-32 inputs) | 1.19 | ns |
| $\mathrm{t}_{\mathrm{RCKL}}$ | Input High to Low (fully loaded row-32 inputs) | 1.1 | ns |
| $\mathrm{t}_{\mathrm{RCKH}}$ | Input Low to High (minimally loaded row-1 input) | 0.89 | ns |
| $\mathrm{t}_{\mathrm{RCKL}}$ | Input High to Low (minimally loaded row—1 input) | 0.85 | ns |

* The timing delay difference between tile locations is less than 15ps.

Table 8 • Global Routing Skew
(Worst-Case Commercial Conditions, $V_{D D P}=3.0 \mathrm{~V}, V_{D D L}=2.3 \mathrm{~V}, T_{J}=70^{\circ} \mathrm{C}$ )

| Parameter | Description | Max. | Units |
| :--- | :--- | :--- | :---: |
| $t_{\text {RCKSWH }}$ | Maximum Skew Low to High | 0.30 | ns |
| $t_{\text {RCKSH }}$ | Maximum Skew High to Low | 0.26 | ns |



Figure 20 • Module Delays

## Table 9 • Sample Macrocell Library Listing

(Worst-Case Commercial Conditions, $V_{D D L}=2.3 \mathrm{~V}, T_{J}=70^{\circ} \mathrm{C}$ )

| Cell Name | Description | Maximum <br> Intrinsic Delay | Minimum <br> Setup/Hold | Units |
| :--- | :--- | :---: | :---: | :---: |
| NAND2 | 2-Input NAND | 0.42 |  | ns |
| AND2 | 2-Input AND | 0.40 |  | ns |
| NOR3 | 3-Input NOR | 0.42 |  | ns |
| MUX2L | 2-1 Mux with Active Low Select | 0.42 |  | ns |
| OA21 | 2-Input OR into a 2-Input AND | 0.40 |  | ns |
| XOR2 | 2-Input Exclusive OR | 0.34 |  | ns |
| LDL | Active Low Latch (LH/HL) | D: $0.26 / 0.21$ | $\mathrm{t}_{\text {setup }} 0.54$ | ns |
| DFFL | Negative Edge-Triggered D-type Flip-Flop (LH/HL) | CLK-Q: | $\mathrm{t}_{\text {hold }} 0.20$ |  |
|  |  | $0.42 / 0.37$ | $\mathrm{t}_{\text {hold }} 0.20$ | ns |

Note: Assumes fanout of two.

## Embedded Memory Specifications

This section focuses on the embedded memory of the ProASIC 500K family. It describes the SRAM and FIFO interface signals and includes timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks (Table 10). Refer to Table 2 on page 9 for basic RAM configurations.

## Enclosed Timing Diagrams-SRAM Mode:

- Asynchronous RAM Read, Address Controlled, RDB=0
- Asynchronous RAM Read, RDB Controlled
- Asynchronous RAM Write
- Synchronous RAM Read, Access Timed Output Strobe (Synchronous Transparent)
- Synchronous RAM Read, Pipeline Mode Outputs (Synchronous Pipelined)
- Synchronous RAM Write
- Synchronous Write \& Read to the Same Location
- Asynchronous Write \& Synchronous Read to the Same Location
- Asynchronous Write \& Read to the Same Location
- Synchronous Write \& Asynchronous Read to the Same Location

Note: The difference between synchronous transparent and pipeline modes is the timing of all the output signals from the memory. In transparent mode the outputs will change within the same clock cycle to reflect the data requested by the currently valid access to the memory. However, if clock cycles are short (high clock speed) the data requires most of the clock cycle to change to valid values (stable signals). This makes processing of this data in the same clock cycle nearly impossible. Most designers solve this problem by adding registers at all outputs of the memory to push the data processing into the next clock cycle. In this setup, the whole cycle time can be used to process the data. To simplify the use of this kind of memory setup these registers have been implemented as part of the memory primitive and are available to the user in the synchronous pipeline mode. In this mode the output signals will change shortly after the second rising edge following the initiation of the read access.

Table 10 • Memory Block SRAM Interface Signals

| SRAM Signal | Bits |  | In/Out |
| :--- | :---: | :---: | :--- |
| Description |  |  |  |
| WCLKS | 1 | IN | Write clock used on synchronization on write side |
| RCLKS | 1 | IN | Read clock used on synchronization on read side |
| RADDR<0:7> | 8 | IN | Read address |
| RBLKB | 1 | IN | Negative true read block select |
| RDB | 1 | IN | Negative true read pulse |
| WADDR<0:7> | 8 | IN | Write address |
| WBLKB | 1 | IN | Negative true write block select |
| DI<0:8> | 9 | IN | Input data bits $<0: 8>,<8>$ will be generated if PARGEN is true |
| WRB | 1 | IN | Negative true write pulse |
| DO<0:8> | 9 | OUT | Output data bits <0:8> |
| RPE | 1 | OUT | Read parity error |
| WPE | 1 | OUT | Write parity error |
| PARODD | 1 | IN | Selects odd parity generation/detect when high, even when low |

[^2]
## Synchronous RAM Read, Access Timed Output Strobe (Synchronous Transparent)


$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol t $\mathbf{x x x ~}$ | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :--- |
| CCYC | Cycle time | 7.5 |  | ns |  |
| CMH | Clock high phase | 3.0 |  | ns |  |
| CML | Clock low phase | 3.0 |  | ns |  |
| OCA | New RDATA access from RCLK $\uparrow$ | 7.5 |  | ns |  |
| OCH | Old RDATA valid from RCLK $\uparrow$ |  | 3.0 | ns |  |
| RACH | RADDR hold from RCLK $\uparrow$ | 0.5 |  | ns |  |
| RACS | RADDR setup to RCLK $\uparrow$ | 1.0 |  | ns |  |
| RDCH | RDB hold from RCLK $\uparrow$ | 0.5 |  | ns |  |
| RDCS | RDB setup to RCLK $\uparrow$ | 1.0 |  | ns |  |
| RPCA | New RPE access from RCLK $\uparrow$ | 9.5 |  | ns |  |
| RPCH | Old RPE valid from RCLK $\uparrow$ |  | 3.0 | ns |  |

## Synchronous RAM Read, Pipeline Mode Outputs (Synchronous Pipelined)


$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol t | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :--- |
| CCYC | Cycle time | 7.5 |  | ns |  |
| CMH | Clock high phase | 3.0 |  | ns |  |
| CML | Clock low phase | 3.0 |  | ns |  |
| OCA | New RDATA access from RCLK $\uparrow$ | 2.0 |  | ns |  |
| OCH | Old RDATA valid from RCLK $\uparrow$ |  | .75 | ns |  |
| RACH | RADDR hold from RCLK $\uparrow$ | 0.5 |  | ns |  |
| RACS | RADDR setup to RCLK $\uparrow$ | 1.0 |  | ns |  |
| RDCH | RDB hold from RCLK $\uparrow$ | 0.5 |  | ns |  |
| RDCS | RDB setup to RCLK $\uparrow$ | 1.0 |  | ns |  |
| RPCA | New RPE access from RCLK $\uparrow$ | 4.0 |  | ns |  |
| RPCH | Old RPE valid from RCLK $\uparrow$ |  | 1.0 | ns |  |

## Asynchronous RAM Write


$\mathbf{T}_{\mathbf{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $\mathrm{t}_{\mathbf{x x}}$ | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :--- |
| AWRH | WADDR hold from WB $\uparrow$ | 1.0 |  | ns |  |
| AWRS | WADDR setup to WB $\downarrow$ | 0.5 |  | ns |  |
| DWRH | WDATA hold from WB $\uparrow$ | 1.5 |  | ns |  |
| DWRS | WDATA setup to WB $\uparrow$ | 0.5 |  | ns | PARGEN is inactive |
| DWRS | WDATA setup to WB $\uparrow$ | 2.5 |  | ns | PARGEN is active |
| WPDA | WPE access from WDATA | 3.0 |  | ns | WPE is invalid while |
| WPDH | WPE hold from WDATA |  | 1.0 | ns | PARGEN is active |
| WRCYC | Cycle time | 7.5 |  | ns |  |
| WRMH | WB high phase | 3.0 |  | ns | Inactive |
| WRML | WB low phase | 3.0 |  | ns | Active |

## Asynchronous RAM Read, Address Controlled, RDB=0


$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $_{\mathbf{x x x}}$ | Description | Min. | Max. | Units | Notes |
| :---: | :--- | :---: | :---: | :---: | :--- |
| ACYC | Read cycle time | 7.5 |  | ns |  |
| OAA | New RDATA access from RADDR stable | 7.5 |  | ns |  |
| OAH | Old RDATA hold from RADDR stable |  | 3.0 | ns |  |
| RPAA | New RPE access from RADDR stable | 10.0 |  | ns |  |
| RPAH | Old RPE hold from RADDR stable |  | 3.0 | ns |  |

## Asynchronous RAM Read, RDB Controlled


$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $\mathrm{t}_{\mathbf{x x x}}$ | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :--- |
| ORDA | New RDATA access from RB $\downarrow$ | 7.5 |  | ns |  |
| ORDH | Old RDATA valid from RB $\downarrow$ |  | 3.0 | ns |  |
| RDCYC | Read cycle time | 7.5 |  | ns |  |
| RDMH | RB high phase | 3.0 |  | ns | Inactive setup to new cycle |
| RDML | RB low phase | 3.0 |  | ns | Active |
| RPRDA | New RPE access from RB $\downarrow$ | 9.5 |  | ns |  |
| RPRDH | Old RPE valid from RB $\downarrow$ |  | 3.0 | ns |  |

## Synchronous RAM Write


$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C}$; $\mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $\mathbf{t x x x}$ | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :--- |
| CCYC | Cycle time | 7.5 |  | ns |  |
| CMH | Clock high phase | 3.0 |  | ns |  |
| CML | Clock low phase | 3.0 |  | ns |  |
| DCH | WDATA hold from WCLK $\uparrow$ | 0.5 |  | ns |  |
| DCS | WDATA setup to WCLK $\uparrow$ | 1.0 |  | ns |  |
| WACH | WADDR hold from WCLK $\uparrow$ | 0.5 |  | ns |  |
| WACS | WADDR setup to WCLK $\uparrow$ | 1.0 |  | ns |  |
| WPCA | New WPE access from WCLK $\uparrow$ | 3.0 |  | ns | WPE is invalid while |
| WPCH | Old WPE valid from WCLK $\uparrow$ | 0.5 |  | ns | PARGEN is active |
| WRCH, <br> WBCH | WRB \& WBLKB hold from WCLK $\uparrow$ | 0.5 | ns |  |  |
| WRCS, <br> WBCS | WRB \& WBLKB setup to WCLK $\uparrow$ | 1.0 |  |  |  |

Note: $\quad$ On simultaneous read and write accesses to the same location WDATA is output to RDATA.

## Synchronous Write \& Read to the Same Location



* New data is read if WCLK $\uparrow$ occurs before setup time. The data stored is read if WCLK $\uparrow$ occurs after hold time.
$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $\mathbf{t}_{\mathbf{x x}}$ | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :--- |
| CCYC | Cycle time | 7.5 |  | ns |  |
| CMH | Clock high phase | 3.0 |  | ns |  |
| CML | Clock low phase | 3.0 |  | ns |  |
| WCLKRCLKS | WCLK $\uparrow$ to RCLK $\uparrow$ setup time | -0.1 |  | ns |  |
| WCLKRCLKH | WCLK $\uparrow$ to RCLK $\uparrow$ hold time |  | 7.0 | ns |  |
| OCH | Old RDATA valid from RCLK $\uparrow$ |  | 3.0 | ns | OCA/OCH displayed for |
| OCA | New RDATA valid from RCLK $\uparrow$ | 7.5 |  | ns | Access Timed Output |

Notes:

1. This behavior is valid for Access Timed Output and Pipelined Mode Output. Shown are the timings of an access timed output.
2. During synchronous write and synchronous read access to the same location, the new write data will be read out if the active write clock edge occurs before or at the same time as the active read clock edge. The negative setup time insures this behavior for WCLK and RCLK driven by the same design signal.
3. If WCLK changes after the hold time, the data will be read.
4. A setup or hold time violation will result in unknown output data.

## Asynchronous Write \& Synchronous Read to the Same Location



* New data is read if WB $\downarrow$ occurs before setup time.

The stored data is read if WB $\downarrow$ occurs after hold time.
$\mathrm{T}_{\mathbf{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $\mathbf{t}_{\mathbf{x x x}}$ | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :--- |
| CCYC | Cycle time | 7.5 |  | ns |  |
| CMH | Clock high phase | 3.0 |  | ns |  |
| CML | Clock low phase | 3.0 |  | ns |  |
| WBRCLKS | WB $\downarrow$ to RCLK $\uparrow$ setup time | -0.1 |  | ns |  |
| WBRCLKH | WB $\downarrow$ to RCLK $\uparrow$ hold time |  | 7.0 | ns |  |
| OCH | Old RDATA valid from RCLK $\uparrow$ |  | 3.0 | ns | OCA/OCH displayed for |
| OCA | New RDATA valid from RCLK $\uparrow$ | 7.5 |  | ns | Access Timed Output |
| DWRRCLKS | WDATA to RCLK $\uparrow$ setup time | 0 |  | ns |  |
| DWRH | WDATA to WB $\uparrow$ hold time |  | 1.5 | ns |  |

## Notes:

1. This behavior is valid for Access Timed Output and Pipelined Mode Output. Shown are the timings of an access timed output.
2. In asynchronous write and synchronous read access to the same location, the new write data will be read out if the active write signal edge occurs before or at the same time as the active read clock edge. If WB changes to low after hold time, the data will be read.
3. A setup or hold time violation will result in unknown output data.

## Asynchronous Write \& Read to the Same Location


$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $\mathbf{t}_{\mathbf{x x x}}$ | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :--- |
| ORDA | New RDATA access from RB $\downarrow$ | 7.5 |  | ns |  |
| ORDH | Old RDATA valid from RB $\downarrow$ |  | 3.0 | ns |  |
| OWRA | New RDATA access from WB $\uparrow$ | 3.0 |  | ns |  |
| OWRH | Old RDATA valid from WB $\uparrow$ |  | 0.5 | ns |  |
| RAWRS | RB $\downarrow$ or RADDR from WB $\downarrow$ | 5.0 |  | ns |  |
| RAWRH | RB $\uparrow$ or RADDR from WB $\uparrow$ | 5.0 |  | ns |  |

## Notes:

1. During an asynchronous read cycle, each write operation (sync. or async.) to the same location will automatically trigger a read operation which updates the read data.
2. Violation or RAWRS will disturb access to the OLD data.
3. Violation of RAWRH will disturb access to the NEWER data.

## Synchronous Write \& Asynchronous Read to the Same Location


$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $\mathbf{t}_{\mathbf{x x x}}$ | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :--- |
| ORDA | New RDATA access from RB $\downarrow$ | 7.5 |  | ns |  |
| ORDH | Old RDATA valid from RB $\downarrow$ |  | 3.0 | ns |  |
| OWRA | New RDATA access from WCLK $\downarrow$ | 3.0 |  | ns |  |
| OWRH | Old RDATA valid from WCLK $\downarrow$ |  | 0.5 | ns |  |
| RAWCLKS | RB $\downarrow$ or RADDR from WCLK $\uparrow$ | 5.0 |  | ns |  |
| RAWCLKH | RB $\uparrow$ or RADDR from WCLK $\downarrow$ | 5.0 |  | ns |  |

Notes:

1. During an asynchronous read cycle, each write operation (sync. or async.) to the same location will automatically trigger a read operation which updates the read data.
2. Violation of RAWCLKS will disturb access to OLD data.
3. Violation of RAWCLKH will disturb access to NEWER data.

## Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty, respectively. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written during the transition out of full to not full or read during the transition out of empty to not empty. The exact time at which the write (read) operation changes from inhibited to accepted after the read (write) signal which causes the transition from full (empty) to not full (empty) is indeterminate. This indeterminate period starts 1 ns after the RB (WB) transition which deactivates full (not empty) and ends 3 ns after the RB (WB) transition, for slow cycles. For fast cycles, the indeterminate period ends 3 ns ( $7.5 \mathrm{~ns}-\mathrm{RDL}$ (WRL)) after the RB (WB) transition, whichever is later.

The timing diagram for write is shown in Figure 21 on page 35. The timing diagram for read is shown in Figure 22 on page 35. For basic RAM configurations, see Table 2 on page 9.

## Enclosed Timing Diagrams-FIFO Mode:

- Asynchronous FIFO Read
- Asynchronous FIFO Write
- Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)
- Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)
- Synchronous FIFO Write
- FIFO Reset

Table 11 • Memory Block FIFO Interface Signals

| FIFO Signal | Bits | In/Out | Description |
| :--- | :--- | :--- | :--- |
| WCLK | 1 | IN | Write clock used on synchronization on write side |
| RCLK | 1 | IN | Read clock used on synchronization on read side |
| LEVEL <0:7> | 8 | IN | Direct configuration implements static flag logic. |
| RBLKB | 1 | IN | Negative true read block select. |
| RDB | 1 | IN | Negative true read pulse. |
| RESET | 1 | IN | Negative true reset for FIFO pointers. |
| WBLKB | 1 | IN | Negative true write block select. |
| DI<0:8> | 1 | IN | Input data bits <0:8>, <8> will be generated if PARGEN is true. |
| WRB | 2 | OUT | FIFO flags. FULL prevents write and EMPTY prevents read. |
| FULL, EMPTY | 2 | OUT | EQTH is true when the FIFO holds (LEVEL) words. GEQTH is true when the <br> FIFO holds (LEVEL) words or more. |
| EQTH, GEQTH | 9 | OUT | Output data bits <0:8> |
| DO<0:8> | 1 | OUT | Read parity error. |
| RPE | 1 | OUT | Write parity error. |
| WPE | 3 | IN | Configures DEPTH of the FIFO to 2 (LGDEP+1) |
| LGDEP <0:2> | 1 | IN | Selects odd parity generation/detect when high, even when low. |
| PARODD |  |  |  |



Figure 21 • Write Timing Diagram


Figure 22 • Read Timing Diagram
ctel

## Asynchronous FIFO Read


$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol t ${ }_{\text {xxx }}$ | Description | Min. | Max. | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \hline \text { ERDH, } \\ & \text { FRDH, } \\ & \text { THRDH } \end{aligned}$ | Old EMPTY, FULL, EQTH, \& GETH valid hold time from RB $\uparrow$ |  | 0.5 | ns | Empty/ful//thresh are invalid from the end of hold until the new access is complete |
| ERDA | New EMPTY access from RB $\uparrow$ | $3.0{ }^{1}$ |  | ns |  |
| FRDA | FULL $\downarrow$ access from RB $\uparrow$ | $3.0{ }^{1}$ |  | ns |  |
| ORDA | New RDATA access from RB $\downarrow$ | 7.5 |  | ns |  |
| ORDH | Old RDATA valid from RB $\downarrow$ |  | 3.0 | ns |  |
| RDCYC | Read cycle time | 7.5 |  | ns |  |
| RDWRS | WB $\uparrow$, clearing EMPTY, setup to RB $\downarrow$ | $3.0^{2}$ |  | ns | Enabling the read operation |
|  |  |  | 1.0 | ns | Inhibiting the read operation |
| RDH | RB high phase | 3.0 |  | ns | Inactive |
| RDL | RB low phase | 3.0 |  | ns | Active |
| RPRDA | New RPE access from RB $\downarrow$ | 9.5 |  | ns |  |
| RPRDH | Old RPE valid from RB $\downarrow$ |  | 4.0 | ns |  |
| THRDA | EQTH or GETH access from RB $\uparrow$ | 4.5 |  | ns |  |

## Notes:

1. At fast cycles, ERDA \& FRDA $=\operatorname{MAX}(7.5 \mathrm{~ns}-\mathrm{RDL}), 3.0 \mathrm{~ns}$
2. At fast cycles, RDWRS (for enabling read) $=\operatorname{MAX}(7.5 \mathrm{~ns}-W R L), 3.0 \mathrm{~ns}$

## Asynchronous FIFO Write


$\mathrm{T}_{\mathbf{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $\mathrm{t}_{\text {xxx }}$ | Description | Min. | Max. | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DWRH | WDATA hold from WB $\uparrow$ | 1.5 |  | ns |  |
| DWRS | WDATA setup to WB $\uparrow$ | 0.5 |  | ns | PARGEN is inactive. |
| DWRS | WDATA setup to WB $\uparrow$ | 2.5 |  | ns | PARGEN is active. |
| EWRH, FWRH, THWRH | OId EMPTY, FULL, EQTH, \& GETH valid hold time after WB $\uparrow$ |  | 0.5 | ns | Empty/full/thresh are invalid from the end of hold until the new access is complete. |
| EWRA | EMPTY $\downarrow$ access from WB $\uparrow$ | $3.0^{1}$ |  | ns |  |
| FWRA | New FULL access from WB $\uparrow$ | $3.0^{1}$ |  | ns |  |
| THWRA | EQTH or GETH access from WB $\uparrow$ | 4.5 |  | ns |  |
| WPDA | WPE access from WDATA | 3.0 |  | ns | WPE is invalid while PARGEN is active. |
| WPDH | WPE hold from WDATA |  | 1.0 | ns |  |
| WRCYC | Cycle time | 7.5 |  | ns |  |
| WRRDS | RB $\uparrow$, clearing FULL, setup to WB $\downarrow$ | $3.0^{2}$ |  | ns | Enabling the write operation. |
|  |  |  | 1.0 |  | Inhibiting the write operation. |
| WRH | WB high phase | 3.0 |  | ns | Inactive |
| WRL | WB low phase | 3.0 |  | ns | Active |

[^3]
## Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)


$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\text {DDL }}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $\mathbf{t}_{\mathbf{x x x}}$ | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :--- |
| CCYC | Cycle time | 7.5 |  | ns |  |
| CMH | Clock high phase | 3.0 |  | ns |  |
| CML | Clock low phase | 3.0 |  | ns |  |
| ECBA | New EMPTY access from RCLK $\downarrow$ | $3.0^{1}$ |  | ns |  |
| FCBA | FULL $\downarrow$ access from RCLK $\downarrow$ | $3.0^{1}$ |  | ns |  |
| ECBH, <br> FCBH, <br> THCBH | Old EMPTY, FULL, EQTH, \& GETH valid <br> hold time from RCLK $\downarrow$ |  | 1.0 | ns | Empty/full/thresh are invalid <br> from the end of hold until the <br> new access is complete |
| OCA | New RDATA access from RCLK $\uparrow$ | 7.5 |  | ns |  |
| OCH | Old RDATA valid from RCLK $\uparrow$ |  | 3.0 | ns |  |
| RDCH | RDB hold from RCLK $\uparrow$ | 1.0 |  | ns |  |
| RDCS | RDB setup to RCLK $\uparrow$ | 9.5 |  | ns |  |
| RPCA | New RPE access from RCLK $\uparrow$ |  | 3.0 | ns |  |
| RPCH | Old RPE valid from RCLK $\uparrow$ | 4.5 |  | ns |  |
| THCBA | EQTH or GETH access from RCLK $\downarrow$ |  |  |  |  |

Note:

1. At fast cycles, ECBA \& FCBA $=M A X(7.5 . n s-C M H), 3.0 \mathrm{~ns}$

## Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)


$\mathrm{T}_{\mathbf{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $\mathbf{t x x x}$ | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :--- |
| CCYC | Cycle time | 7.5 |  | ns |  |
| CMH | Clock high phase | 3.0 |  | ns |  |
| CML | Clock low phase | 3.0 |  | ns |  |
| ECBA | New EMPTY access from RCLK $\downarrow$ | $3.0^{\uparrow}$ |  | ns |  |
| FCBA | FULL $\downarrow$ access from RCLK $\downarrow$ | $3.0^{\uparrow}$ |  | ns |  |
| ECBH, <br> FCBH, <br> THCBH | Old EMPTY, FULL, EQTH, \& GETH valid <br> hold time from RCLK $\downarrow$ |  | 1.0 | ns | Empty/full/thresh are invalid <br> from the end of hold until the <br> new access is complete |
| OCA | New RDATA access from RCLK $\uparrow$ | 2.0 |  | ns |  |
| OCH | Old RDATA valid from RCLK $\uparrow$ |  | 0.75 | ns |  |
| RDCH | RDB hold from RCLK $\uparrow$ | 0.5 |  | ns |  |
| RDCS | RDB setup to RCLK $\uparrow$ | 1.0 |  | ns |  |
| RPCA | New RPE access from RCLK $\uparrow$ | 4.0 |  | ns |  |
| RPCH | Old RPE valid from RCLK $\uparrow$ | 1.0 | ns |  |  |
| THCBA | EQTH or GETH access from RCLK $\downarrow$ | 4.5 |  | ns |  |

## Note:

1. At fast cycles, $E C B A \& F C B A=M A X(7.5 n s-C M S), 3.0 n s$

## Synchronous FIFO Write


$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\text {DDL }}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol t ${ }_{\text {xxx }}$ | Description | Min. | Max. | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CCYC | Cycle time | 7.5 |  | ns |  |
| CMH | Clock high phase | 3.0 |  | ns |  |
| CML | Clock low phase | 3.0 |  | ns |  |
| DCH | WDATA hold from WCLK $\uparrow$ | 0.5 |  | ns |  |
| DCS | WDATA setup to WCLK $\uparrow$ | 1.0 |  | ns |  |
| FCBA | New FULL access from WCLK $\downarrow$ | $3.0{ }^{1}$ |  | ns |  |
| ECBA | EMPTY $\downarrow$ access from WCLK $\downarrow$ | $3.0^{1}$ |  | ns |  |
| $\begin{aligned} & \text { ECBH, } \\ & \text { FCBH, } \\ & \text { THCBH } \end{aligned}$ | Old EMPTY, FULL, EQTH, \& GETH valid hold time from WCLK $\downarrow$ |  | 1.0 | ns | Empty/full/thresh are invalid from the end of hold until the new access is complete |
| THCBA | EQTH or GETH access from WCLK $\downarrow$ | 4.5 |  | ns |  |
| WPCA | New WPE access from WCLK $\uparrow$ | 3.0 |  | ns | WPE is invalid while |
| WPCH | Old WPE valid from WCLK $\uparrow$ |  | 0.5 | ns | PARGEN is active |
| WRCH, WBCH | WRB \& WBLKB hold from WCLK $\uparrow$ | 0.5 |  | ns |  |
| WRCS, WBCS | WRB \& WBLKB setup to WCLK $\uparrow$ | 1.0 |  | ns |  |

## Note:

1. At fast cycles, $E C B A \& F C B A=M A X(7.5 \mathrm{~ns}-C M H), 3.0 \mathrm{~ns}$

## FIFO Reset


*WB = WRB + WBLRB
$\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{DDL}}=2.3 \mathrm{~V}$ to 2.7 V

| Symbol $\mathbf{t}_{\mathbf{x x}}$ | Description | Min. | Max. | Units | Notes |
| :--- | :--- | :---: | :---: | :---: | :---: |
| CBRSH | WCLK or RCLK $\uparrow$ hold from RESETB $\uparrow$ | 1.5 |  | ns | Synchronous mode only |
| CBRSS | WCLK or RCLK $\downarrow$ setup to RESETB $\uparrow$ | 1.5 |  | ns | Synchronous mode only |
| ERSA | New EMPTY $\uparrow$ access from RESETB $\downarrow$ | 3.0 |  | ns |  |
| FRSA | FULL $\downarrow$ access from RESETB $\downarrow$ | 3.0 |  | ns |  |
| RSL | RESETB low phase | 7.5 |  | ns |  |
| THRSA | EQTH or GETH access from RESETB $\downarrow$ | 4.5 |  | ns |  |
| WBRSH | WB $\downarrow$ hold from RESETB $\uparrow$ | 1.5 |  | ns | Asynchronous mode only |
| WBRSS | WB $\uparrow$ setup to RESETB $\uparrow$ | 1.5 |  | ns | Asynchronous mode only |

## Pin Description

## I/O User Input/Output

The I/0 pin functions as an input, output, three-state, or bi-directional buffer. Input and output signal levels are compatible with standard LVTTL and LVCMOS specifications. Unused I/0 pins are configured as inputs with pull-up resistor.

## N/C

## No Connect

To maintain compatibility with future Actel ProASIC products it is recommended that this pin not be connected to the circuitry on the board.

## GL Global Input Pin

Low skew input pin for clock or other global signals. Input only. This pin can be configured with a pull-up resistor.

## GND

## Ground

Common ground supply voltage.
$\mathbf{V}_{\text {DDL }}$

## Logic Array Power Supply Pin

 2.5 V supply voltage.$\mathbf{V}_{\text {DDP }}$
I/O Pad Power Supply Pin
2.5 V or 3.3 V supply voltage.

## $\mathbf{V}_{\text {PP }} \quad$ Programming Supply Pin

This pin must be connected to $\mathrm{V}_{\mathrm{DDP}}$ during normal operation, or it can remain at 16.5 V in an ISP application. This pin must not float.

## $\mathbf{V}_{\text {PN }} \quad$ Programming Supply Pin

This pin must be connected to GND during normal operation, or it can remain at -12 V in an ISP application. This pin must not float.

## TMS Test Mode Select

The TMS pin controls the use of JTAG circuitry.
TCK Test Clock
Clock input pin for JTAG.

## TDI

Test Data In
Serial input for JTAG.

## TDO Test Data Out

Serial output for JTAG.

## TRST Test Reset Input

An optimal JTAG reset pin.

## RCK Running Clock

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted.

## Package Pin Assignments

208-Pin PQFP


## 208-Pin PQFP

| Pin Number | A500K050 Function | A500K130 Function | A500K180 Function | A500K270 Function | Pin Number | A500K050 Function | A500K130 Function | A500K180 Function | A500K270 Function |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | GND | GND | GND | GND | 53 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| 2 | I/O | I/O | I/O | I/O | 54 | I/O | I/O | I/O | I/O |
| 3 | 1/0 | 1/O | 1/O | 1/O | 55 | I/O | 1/O | 1/O | 1/O |
| 4 | I/O | 1/O | 1/O | 1/O | 56 | I/O | 1/0 | 1/O | 1/O |
| 5 | I/O | I/O | I/O | I/O | 57 | I/O | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O | I/O | 58 | I/O | I/O | I/O | I/O |
| 7 | I/O | I/O | 1/O | I/O | 59 | I/O | 1/0 | 1/0 | 1/0 |
| 8 | I/O | I/O | I/O | I/O | 60 | I/O | I/O | 1/O | 1/O |
| 9 | I/O | I/O | I/O | I/O | 61 | I/O | I/O | 1/0 | I/O |
| 10 | I/O | I/O | 1/O | I/O | 62 | I/O | 1/O | 1/O | 1/O |
| 11 | I/O | I/O | 1/O | I/O | 63 | I/O | I/O | 1/O | 1/O |
| 12 | 1/O | I/O | 1/O | I/O | 64 | I/O | I/O | I/O | I/O |
| 13 | I/O | 1/0 | 1/0 | I/O | 65 | GND | GND | GND | GND |
| 14 | 1/0 | 1/O | 1/O | I/O | 66 | I/O | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O | I/O | 67 | I/O | I/O | 1/O | 1/O |
| 16 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | 68 | 1/O | I/O | 1/0 | 1/O |
| 17 | GND | GND | GND | GND | 69 | I/O | 1/O | 1/O | 1/O |
| 18 | I/O | I/O | I/O | I/O | 70 | I/O | I/O | I/O | I/O |
| 19 | 1/0 | 1/O | 1/O | 1/O | 71 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| 20 | 1/O | I/O | I/O | I/O | 72 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| 21 | I/O | I/O | I/O | I/O | 73 | I/O | I/O | I/O | I/O |
| 22 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | 74 | 1/0 | 1/0 | 1/0 | I/O |
| 23 | I/O | I/O | I/O | I/O | 75 | 1/O | 1/O | 1/O | I/O |
| 24 | I/O | I/O | I/O | I/O | 76 | I/O | I/O | 1/0 | I/O |
| 25 | GL | GL | GL | GL | 77 | I/O | I/O | 1/0 | 1/O |
| 26 | GL | GL | GL | GL | 78 | I/O | 1/O | 1/O | I/O |
| 27 | I/O | I/O | I/O | I/O | 79 | I/O | 1/0 | 1/0 | 1/O |
| 28 | I/O | I/O | I/O | I/O | 80 | I/O | I/O | I/O | I/O |
| 29 | GND | GND | GND | GND | 81 | GND | GND | GND | GND |
| 30 | I/O | I/O | I/O | I/O | 82 | I/O | I/O | I/O | I/O |
| 31 | I/O | I/O | I/O | I/O | 83 | I/O | 1/O | 1/0 | 1/O |
| 32 | I/O | I/O | I/O | I/O | 84 | I/O | 1/O | 1/O | 1/O |
| 33 | I/O | I/O | I/O | I/O | 85 | I/O | I/O | 1/0 | I/O |
| 34 | 1/O | I/O | 1/O | 1/O | 86 | 1/O | 1/O | 1/O | 1/O |
| 35 | I/O | I/O | I/O | I/O | 87 | I/O | I/O | I/O | I/O |
| 36 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | 88 | $V_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| 37 | I/O | I/O | I/O | I/O | 89 | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| 38 | I/O | I/O | 1/O | 1/O | 90 | I/O | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O | I/O | 91 | 1/O | I/O | 1/O | 1/O |
| 40 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | 92 | 1/0 | 1/O | 1/O | 1/O |
| 41 | GND | GND | GND | GND | 93 | 1/0 | 1/O | 1/O | 1/O |
| 42 | I/O | I/O | I/O | I/O | 94 | I/O | I/O | 1/O | I/O |
| 43 | 1/O | 1/O | 1/O | 1/O | 95 | 1/O | 1/O | 1/O | I/O |
| 44 | I/O | I/O | I/O | 1/O | 96 | I/O | I/O | I/O | I/O |
| 45 | I/O | I/O | I/O | 1/O | 97 | GND | GND | GND | GND |
| 46 | 1/O | 1/O | 1/O | 1/O | 98 | I/O | I/O | I/O | I/O |
| 47 | I/O | I/O | 1/O | 1/O | 99 | I/O | 1/O | 1/0 | I/O |
| 48 | I/O | I/O | I/O | I/O | 100 | I/O | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O | 1/O | 101 | TCK, I/O | TCK, I/O | TCK, I/O | TCK, I/O |
| 50 | I/O | I/O | I/O | 1/O | 102 | TDI, I/O | TDI, I/O | TDI, I/O | TDI, I/O |
| 51 | I/O | I/O | I/O | I/O | 103 | TMS, I/O | TMS, I/O | TMS, I/O | TMS, I/O |
| 52 | GND | GND | GND | GND | 104 | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |

208-Pin PQFP (Continued)

| Pin Number | A500K050 Function | A500K130 Function | A500K180 Function | A500K270 Function |
| :---: | :---: | :---: | :---: | :---: |
| 105 | GND | GND | GND | GND |
| 106 | $V_{\text {PP }}$ | $V_{\text {PP }}$ | $V_{\text {PP }}$ | $V_{P P}$ |
| 107 | $V_{P N}$ | $V_{P N}$ | $V_{P N}$ | $\mathrm{V}_{\mathrm{PN}}$ |
| 108 | TDO, I/O | TDO, I/O | TDO, I/O | TDO, I/O |
| 109 | TRST, I/O | TRST, I/O | TRST, I/O | TRST, I/O |
| 110 | RCK, I/O | RCK, I/O | RCK, I/O | RCK, I/O |
| 111 | I/O | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O | I/O |
| 113 | I/O | I/O | 1/O | I/O |
| 114 | I/O | I/O | I/O | I/O |
| 115 | I/O | I/O | I/O | I/O |
| 116 | I/O | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O | 1/O |
| 118 | I/O | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O | I/O |
| 122 | GND | GND | GND | GND |
| 123 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| 124 | I/O | I/O | I/O | I/O |
| 125 | I/O | I/O | I/O | I/O |
| 126 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| 127 | I/O | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O | I/O |
| 129 | I/O | I/O | I/O | I/O |
| 130 | GND | GND | GND | GND |
| 131 | I/O | I/O | I/O | I/O |
| 132 | I/O | I/O | I/O | I/O |
| 133 | GL | GL | GL | GL |
| 134 | GL | GL | GL | GL |
| 135 | I/O | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O | I/O |
| 138 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\mathrm{DDP}}$ |
| 139 | I/O | I/O | I/O | I/O |
| 140 | I/O | I/O | I/O | I/O |
| 141 | GND | GND | GND | GND |
| 142 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| 143 | I/O | I/O | I/O | I/O |
| 144 | I/O | I/O | I/O | I/O |
| 145 | I/O | I/O | I/O | I/O |
| 146 | I/O | I/O | I/O | I/O |
| 147 | I/O | I/O | I/O | I/O |
| 148 | I/O | I/O | I/O | I/O |
| 149 | I/O | I/O | I/O | I/O |
| 150 | I/O | I/O | I/O | I/O |
| 151 | I/O | I/O | I/O | I/O |
| 152 | I/O | I/O | I/O | I/O |
| 153 | I/O | I/O | I/O | I/O |
| 154 | I/O | I/O | I/O | I/O |
| 155 | I/O | I/O | I/O | I/O |
| 156 | GND | GND | GND | GND |


| $\begin{gathered} \text { Pin } \\ \text { Number } \end{gathered}$ | A500K050 Function | A500K130 Function | A500K180 Function | A500K270 Function |
| :---: | :---: | :---: | :---: | :---: |
| 157 | $V_{\text {DDP }}$ | V ${ }_{\text {DDP }}$ | V ${ }_{\text {DDP }}$ | V ${ }_{\text {DDP }}$ |
| 158 | I/O | I/O | I/O | I/O |
| 159 | 1/O | 1/O | 1/O | 1/0 |
| 160 | 1/O | 1/O | 1/O | I/O |
| 161 | I/O | I/O | I/O | I/O |
| 162 | GND | GND | GND | GND |
| 163 | I/O | I/O | I/O | I/O |
| 164 | 1/O | 1/O | 1/O | I/O |
| 165 | 1/O | I/O | 1/O | I/O |
| 166 | I/O | 1/O | I/O | I/O |
| 167 | I/O | 1/O | I/O | I/O |
| 168 | 1/O | 1/O | 1/O | I/O |
| 169 | I/O | I/O | I/O | I/O |
| 170 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| 171 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| 172 | I/O | I/O | I/O | I/O |
| 173 | 1/O | I/O | 1/O | I/O |
| 174 | I/O | I/O | I/O | I/O |
| 175 | 1/O | 1/O | 1/0 | I/O |
| 176 | 1/O | 1/0 | 1/O | I/O |
| 177 | 1/O | I/O | 1/O | 1/O |
| 178 | GND | GND | GND | GND |
| 179 | I/O | I/O | I/O | I/O |
| 180 | 1/O | 1/O | 1/0 | I/O |
| 181 | 1/O | 1/O | 1/O | I/O |
| 182 | 1/O | 1/O | 1/O | I/O |
| 183 | 1/0 | 1/O | 1/0 | I/O |
| 184 | 1/O | 1/O | 1/O | I/O |
| 185 | I/O | I/O | I/O | I/O |
| 186 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| 187 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| 188 | I/O | I/O | I/O | I/O |
| 189 | 1/O | I/O | 1/O | 1/0 |
| 190 | I/O | 1/O | 1/O | I/O |
| 191 | I/O | I/O | I/O | I/O |
| 192 | 1/0 | I/O | 1/O | I/O |
| 193 | 1/O | 1/O | 1/O | I/O |
| 194 | I/O | I/O | I/O | I/O |
| 195 | GND | GND | GND | GND |
| 196 | I/O | I/O | I/O | I/O |
| 197 | 1/O | I/O | 1/O | I/O |
| 198 | I/O | I/O | I/O | I/O |
| 199 | I/O | 1/O | 1/0 | 1/0 |
| 200 | I/O | I/O | 1/O | I/O |
| 201 | I/O | 1/O | 1/O | I/O |
| 202 | 1/O | 1/O | I/O | 1/O |
| 203 | I/O | 1/O | I/O | I/O |
| 204 | I/O | 1/O | I/O | 1/O |
| 205 | 1/O | 1/O | 1/O | 1/O |
| 206 | I/O | 1/O | I/O | 1/O |
| 207 | I/O | I/O | I/O | I/O |
| 208 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |

## Package Pin Assignments (Continued)

 272-Pin PBGA (Bottom View)

## 272-Pin PBGA

| Pin Number | $\begin{gathered} \text { A500K050 } \\ \text { Function } \end{gathered}$ | A500K130 Function |
| :---: | :---: | :---: |
| A1 | I/O | I/O |
| A2 | I/O | I/O |
| A3 | I/O | I/O |
| A4 | I/O | I/O |
| A5 | I/O | I/O |
| A6 | I/O | I/O |
| A7 | I/O | I/O |
| A8 | I/O | I/O |
| A9 | I/O | I/O |
| A10 | I/O | I/O |
| A11 | I/O | I/O |
| A12 | I/O | I/O |
| A13 | I/O | I/O |
| A14 | I/O | I/O |
| A15 | I/O | I/O |
| A16 | I/O | I/O |
| A17 | I/O | I/O |
| A18 | I/O | I/O |
| A19 | I/O | I/O |
| A20 | I/O | I/O |
| B1 | I/O | I/O |
| B2 | I/O | I/O |
| B3 | I/O | I/O |
| B4 | I/O | I/O |
| B5 | I/O | I/O |
| B6 | I/O | I/O |
| B7 | I/O | I/O |
| B8 | I/O | I/O |
| B9 | I/O | I/O |
| B10 | I/O | I/O |
| B11 | I/O | I/O |
| B12 | I/O | I/O |
| B13 | I/O | I/O |
| B14 | I/O | I/O |
| B15 | I/O | I/O |
| B16 | I/O | I/O |
| B17 | I/O | I/O |
| B18 | I/O | I/O |
| B19 | I/O | I/O |
| B20 | I/O | I/O |
| C1 | I/O | I/O |
| C2 | I/O | I/O |
| C3 | I/O | I/O |
| C4 | I/O | I/O |
| C5 | I/O | I/O |
| C6 | I/O | I/O |


| Pin Number | A500K050 Function | A500K130 Function |
| :---: | :---: | :---: |
| C7 | I/O | I/O |
| C8 | I/O | I/O |
| C9 | I/O | I/O |
| C10 | I/O | I/O |
| C11 | I/O | I/O |
| C12 | I/O | I/O |
| C13 | I/O | I/O |
| C14 | I/O | I/O |
| C15 | I/O | I/O |
| C16 | I/O | I/O |
| C17 | I/O | I/O |
| C18 | I/O | I/O |
| C19 | I/O | I/O |
| C20 | I/O | I/O |
| D1 | I/O | I/O |
| D2 | I/O | I/O |
| D3 | I/O | I/O |
| D4 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| D5 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| D6 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| D7 | I/O | I/O |
| D8 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| D9 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| D10 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| D11 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| D12 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| D13 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| D14 | I/O | I/O |
| D15 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| D16 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| D17 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| D18 | I/O | I/O |
| D19 | I/O | I/O |
| D20 | I/O | I/O |
| E1 | I/O | I/O |
| E2 | I/O | I/O |
| E3 | I/O | I/O |
| E4 | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| E17 | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| E18 | I/O | I/O |
| E19 | I/O | I/O |
| E20 | I/O | I/O |
| F1 | I/O | I/O |
| F2 | I/O | I/O |
| F3 | I/O | I/O |
| F4 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |


| Pin <br> Number | A500K050 Function | A500K130 Function |
| :---: | :---: | :---: |
| F17 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| F18 | I/O | I/O |
| F19 | I/O | I/O |
| F20 | I/O | I/O |
| G1 | I/O | I/O |
| G2 | I/O | I/O |
| G3 | I/O | I/O |
| G4 | I/O | I/O |
| G17 | I/O | I/O |
| G18 | I/O | I/O |
| G19 | I/O | I/O |
| G20 | I/O | I/O |
| H1 | I/O | I/O |
| H2 | I/O | I/O |
| H3 | I/O | I/O |
| H4 | I/O | I/O |
| H17 | I/O | I/O |
| H18 | I/O | I/O |
| H19 | I/O | I/O |
| H20 | GL | GL |
| J1 | I/O | I/O |
| J2 | GL | GL |
| J3 | GL | GL |
| J4 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| J9 | GND | GND |
| J10 | GND | GND |
| J11 | GND | GND |
| J12 | GND | GND |
| J17 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| J18 | GL | GL |
| J19 | I/O | I/O |
| J20 | I/O | I/O |
| K1 | I/O | I/O |
| K2 | I/O | I/O |
| K3 | I/O | I/O |
| K4 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| K9 | GND | GND |
| K10 | GND | GND |
| K11 | GND | GND |
| K12 | GND | GND |
| K17 | $\mathrm{V}_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| K18 | I/O | I/O |
| K19 | I/O | I/O |
| K20 | I/O | I/O |
| L1 | I/O | I/O |
| L2 | I/O | I/O |

## 272-Pin PBGA (Continued)

| Pin Number | A500K050 Function | A500K130 Function |
| :---: | :---: | :---: |
| L3 | I/O | I/O |
| L4 | $V_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| L9 | GND | GND |
| L10 | GND | GND |
| L11 | GND | GND |
| L12 | GND | GND |
| L17 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| L18 | I/O | I/O |
| L19 | I/O | I/O |
| L20 | I/O | I/O |
| M1 | I/O | I/O |
| M2 | I/O | I/O |
| M3 | I/O | I/O |
| M4 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| M9 | GND | GND |
| M10 | GND | GND |
| M11 | GND | GND |
| M12 | GND | GND |
| M17 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| M18 | I/O | I/O |
| M19 | I/O | I/O |
| M20 | I/O | I/O |
| N1 | I/O | I/O |
| N2 | I/O | I/O |
| N3 | I/O | I/O |
| N4 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| N17 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| N18 | I/O | I/O |
| N19 | I/O | I/O |
| N20 | I/O | I/O |
| P1 | I/O | I/O |
| P2 | I/O | I/O |
| P3 | I/O | I/O |
| P4 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| P17 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| P18 | I/O | I/O |
| P19 | I/O | I/O |
| P20 | I/O | I/O |
| R1 | I/O | I/O |
| R2 | I/O | I/O |
| R3 | I/O | I/O |
| R4 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| R17 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| R18 | I/O | I/O |
| R19 | I/O | I/O |
| R20 | I/O | I/O |


| Pin Number | A500K050 Function | A500K130 Function |
| :---: | :---: | :---: |
| T1 | I/O | I/O |
| T2 | I/O | I/O |
| T3 | I/O | I/O |
| T4 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| T17 | $\mathrm{V}_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| T18 | I/O | I/O |
| T19 | I/O | I/O |
| T20 | I/O | I/O |
| U1 | I/O | I/O |
| U2 | I/O | I/O |
| U3 | I/O | I/O |
| U4 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| U5 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| U6 | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| U7 | I/O | I/O |
| U8 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| U9 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| U10 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| U11 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| U12 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| U13 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| U14 | I/O | I/O |
| U15 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| U16 | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| U17 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| U18 | RCK, I/O | RCK, I/O |
| U19 | I/O | I/O |
| U20 | I/O | I/O |
| V1 | I/O | I/O |
| V2 | I/O | I/O |
| V3 | I/O | I/O |
| V4 | I/O | I/O |
| V5 | I/O | I/O |
| V6 | I/O | I/O |
| V7 | I/O | I/O |
| V8 | I/O | I/O |
| V9 | I/O | I/O |
| V10 | I/O | I/O |
| V11 | I/O | I/O |
| V12 | I/O | I/O |
| V13 | I/O | I/O |
| V14 | 1/O | I/O |
| V15 | I/O | I/O |
| V16 | I/O | I/O |
| V17 | TMS, I/O | TMS, I/O |
| V18 | TDO, I/O | TDO, I/O |


| Pin <br> Number | A500K050 Function | A500K130 Function |
| :---: | :---: | :---: |
| V19 | I/O | I/O |
| V20 | I/O | I/O |
| W1 | I/O | I/O |
| W2 | I/O | I/O |
| W3 | I/O | I/O |
| W4 | I/O | I/O |
| W5 | I/O | I/O |
| W6 | I/O | I/O |
| W7 | I/O | I/O |
| W8 | 1/O | I/O |
| W9 | I/O | I/O |
| W10 | 1/O | I/O |
| W11 | I/O | I/O |
| W12 | I/O | I/O |
| W13 | I/O | I/O |
| W14 | I/O | I/O |
| W15 | I/O | I/O |
| W16 | I/O | I/O |
| W17 | TCK, I/O | TCK, I/O |
| W18 | $\mathrm{V}_{\mathrm{PP}}$ | $V_{P P}$ |
| W19 | TRST, I/O | TRST, I/O |
| W20 | I/O | I/O |
| Y1 | I/O | I/O |
| Y2 | I/O | I/O |
| Y3 | I/O | I/O |
| Y4 | I/O | I/O |
| Y5 | I/O | I/O |
| Y6 | I/O | I/O |
| Y7 | I/O | I/O |
| Y8 | I/O | I/O |
| Y9 | I/O | I/O |
| Y10 | I/O | I/O |
| Y11 | I/O | I/O |
| Y12 | I/O | I/O |
| Y13 | I/O | I/O |
| Y14 | I/O | I/O |
| Y15 | I/O | I/O |
| Y16 | I/O | I/O |
| Y17 | I/O | I/O |
| Y18 | TDI, I/O | TDI, I/O |
| Y19 | $\mathrm{V}_{\mathrm{PN}}$ | $\mathrm{V}_{\mathrm{PN}}$ |
| Y20 | I/O | I/O |

## Package Pin Assignments (Continued)

## 456-Pin PBGA (Bottom View)

```
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```



## 456-Pin PBGA

| Pin Number | $\begin{gathered} \hline \text { A500K130 } \\ \text { Function } \end{gathered}$ | A500K180 Function | $\begin{gathered} \hline \text { A500K270 } \\ \text { Function } \end{gathered}$ | Pin Number | $\begin{aligned} & \hline \text { A500K130 } \\ & \text { Function } \end{aligned}$ | A500K180 Function | $\begin{gathered} \hline \text { A500K270 } \\ \text { Function } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | AB11 | I/O | 1/0 | I/O |
| A2 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | AB12 | 1/O | 1/O | I/O |
| A3 | NC | I/O | I/O | AB13 | I/O | I/O | I/O |
| A4 | I/O | 1/0 | 1/O | AB14 | 1/O | 1/0 | 1/O |
| A5 | I/O | 1/O | I/O | AB15 | I/O | I/O | I/O |
| A6 | NC | 1/O | 1/O | AB16 | I/O | 1/O | 1/0 |
| A7 | I/O | 1/O | 1/O | AB17 | I/O | 1/O | I/O |
| A8 | NC | 1/O | 1/O | AB18 | 1/O | 1/0 | 1/O |
| A9 | NC | 1/0 | 1/O | AB19 | I/O | 1/O | I/O |
| A10 | 1/O | 1/O | 1/0 | AB20 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| A11 | NC | 1/O | 1/O | AB21 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| A12 | NC | I/O | 1/O | AB22 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| A13 | I/O | 1/O | 1/O | AB23 | I/O | I/O | I/O |
| A14 | NC | 1/0 | 1/0 | AB24 | I/O | I/O | 1/O |
| A15 | NC | 1/O | I/O | AB25 | I/O | 1/O | I/O |
| A16 | I/O | 1/O | I/O | AB26 | I/O | I/O | I/O |
| A17 | NC | 1/O | 1/O | AC1 | 1/O | 1/0 | 1/0 |
| A18 | NC | I/O | I/O | AC2 | I/O | I/O | I/O |
| A19 | 1/O | 1/O | 1/0 | AC3 | I/O | I/O | I/O |
| A20 | NC | 1/O | 1/0 | AC4 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| A21 | NC | 1/O | 1/O | AC5 | I/O | I/O | I/O |
| A22 | I/O | 1/0 | 1/0 | AC6 | I/O | I/O | 1/O |
| A23 | NC | I/O | I/O | AC7 | I/O | 1/O | I/O |
| A24 | NC | I/O | 1/O | AC8 | 1/O | 1/O | 1/O |
| A25 | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $V_{\text {DDP }}$ | AC9 | 1/0 | 1/O | I/O |
| A26 | $\mathrm{V}_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | AC10 | 1/0 | 1/0 | 1/0 |
| AA1 | I/O | I/O | I/O | AC11 | I/O | I/O | I/O |
| AA2 | 1/0 | I/O | 1/0 | AC12 | I/O | 1/0 | I/O |
| AA3 | 1/0 | 1/0 | 1/0 | AC13 | 1/O | 1/0 | I/O |
| AA4 | 1/O | I/O | 1/O | AC14 | 1/0 | 1/O | 1/0 |
| AA5 | $V_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $V_{\text {DDL }}$ | AC15 | 1/O | 1/0 | I/O |
| AA22 | $V_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $V_{\text {DDL }}$ | AC16 | 1/O | 1/0 | I/O |
| AA23 | I/O | I/O | I/O | AC17 | I/O | I/O | I/O |
| AA24 | 1/0 | 1/0 | 1/0 | AC18 | 1/O | 1/0 | 1/0 |
| AA25 | 1/0 | 1/0 | 1/0 | AC19 | I/O | 1/0 | I/O |
| AA26 | NC | I/O | 1/O | AC20 | I/O | I/O | I/O |
| AB1 | NC | 1/O | 1/0 | AC21 | TMS, I/O | TMS, I/O | TMS, I/O |
| AB2 | 1/0 | 1/0 | 1/0 | AC22 | TDO, I/O | TDO, I/O | TDO, I/O |
| AB3 | 1/0 | 1/0 | 1/0 | AC23 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| AB4 | I/O | I/O | I/O | AC24 | RCK, I/O | RCK, I/O | RCK, I/O |
| AB5 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | AC25 | I/O | I/O | I/O |
| AB6 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ | AC26 | NC | 1/0 | 1/0 |
| AB7 | $V_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $V_{\text {DDL }}$ | AD1 | NC | 1/0 | 1/0 |
| AB8 | I/O | I/O | 1/O | AD2 | I/O | I/O | I/O |
| AB9 | 1/0 | 1/0 | 1/0 | AD3 | $\mathrm{V}_{\text {DDP }}$ | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| AB10 | 1/O | 1/O | 1/O | AD4 | I/O | I/O | I/O |

456-Pin PBGA (Continued)

| Pin Number | A500K130 Function | A500K180 Function | A500K270 Function | Pin Number | A500K130 Function | A500K180 Function | A500K270 Function |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| AD5 | I/O | I/O | I/O | AE25 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| AD6 | I/O | I/O | I/O | AE26 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| AD7 | I/O | 1/O | I/O | AF1 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| AD8 | I/O | I/O | I/O | AF2 | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| AD9 | I/O | I/O | I/O | AF3 | NC | I/O | I/O |
| AD10 | I/O | I/O | I/O | AF4 | NC | I/O | I/O |
| AD11 | I/O | I/O | I/O | AF5 | I/O | I/O | I/O |
| AD12 | I/O | I/O | I/O | AF6 | NC | I/O | I/O |
| AD13 | I/O | I/O | I/O | AF7 | NC | I/O | I/O |
| AD14 | I/O | I/O | I/O | AF8 | I/O | I/O | I/O |
| AD15 | I/O | I/O | I/O | AF9 | NC | I/O | I/O |
| AD16 | I/O | 1/O | I/O | AF10 | NC | I/O | 1/O |
| AD17 | I/O | I/O | I/O | AF11 | I/O | I/O | 1/O |
| AD18 | I/O | I/O | I/O | AF12 | NC | I/O | I/O |
| AD19 | I/O | I/O | I/O | AF13 | NC | I/O | I/O |
| AD20 | I/O | I/O | I/O | AF14 | I/O | I/O | I/O |
| AD21 | TCK, I/O | TCK, I/O | TCK, I/O | AF15 | NC | I/O | I/O |
| AD22 | $\mathrm{V}_{\mathrm{PP}}$ | $\mathrm{V}_{\mathrm{PP}}$ | $\mathrm{V}_{\mathrm{PP}}$ | AF16 | NC | I/O | I/O |
| AD23 | I/O | I/O | I/O | AF17 | I/O | 1/O | 1/O |
| AD24 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | AF18 | NC | I/O | 1/O |
| AD25 | I/O | I/O | I/O | AF19 | NC | I/O | I/O |
| AD26 | NC | I/O | I/O | AF20 | I/O | I/O | I/O |
| AE1 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | AF21 | NC | I/O | 1/O |
| AE2 | $\mathrm{V}_{\text {DDP }}$ | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | AF22 | I/O | I/O | I/O |
| AE3 | I/O | I/O | I/O | AF23 | TDI, I/O | TDI, I/O | TDI, I/O |
| AE4 | I/O | I/O | I/O | AF24 | NC | I/O | I/O |
| AE5 | I/O | I/O | I/O | AF25 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| AE6 | I/O | 1/O | I/O | AF26 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| AE7 | I/O | I/O | I/O | B1 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ |
| AE8 | I/O | I/O | I/O | B2 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| AE9 | I/O | I/O | I/O | B3 | I/O | I/O | I/O |
| AE10 | I/O | I/O | I/O | B4 | I/O | I/O | I/O |
| AE11 | I/O | I/O | I/O | B5 | I/O | I/O | I/O |
| AE12 | I/O | I/O | I/O | B6 | I/O | I/O | I/O |
| AE13 | I/O | I/O | I/O | B7 | I/O | I/O | I/O |
| AE14 | I/O | I/O | I/O | B8 | I/O | I/O | I/O |
| AE15 | I/O | I/O | I/O | B9 | I/O | I/O | I/O |
| AE16 | I/O | I/O | I/O | B10 | I/O | I/O | I/O |
| AE17 | I/O | 1/O | I/O | B11 | 1/O | I/O | 1/O |
| AE18 | I/O | I/O | I/O | B12 | I/O | I/O | I/O |
| AE19 | I/O | I/O | I/O | B13 | I/O | I/O | I/O |
| AE20 | I/O | I/O | I/O | B14 | I/O | I/O | I/O |
| AE21 | I/O | 1/O | I/O | B15 | I/O | I/O | I/O |
| AE22 | I/O | I/O | I/O | B16 | I/O | I/O | I/O |
| AE23 | $\mathrm{V}_{\mathrm{PN}}$ | $\mathrm{V}_{\mathrm{PN}}$ | $V_{P N}$ | B17 | I/O | I/O | 1/O |
| AE24 | TRST, I/O | TRST, I/O | TRST, I/O | B18 | 1/O | 1/O | 1/O |

## 456-Pin PBGA (Continued)

| Pin Number | $\begin{gathered} \hline \text { A500K130 } \\ \text { Function } \end{gathered}$ | A500K180 Function | $\begin{aligned} & \hline \text { A500K270 } \\ & \text { Function } \end{aligned}$ | Pin Number | $\begin{gathered} \hline \text { A500K130 } \\ \text { Function } \end{gathered}$ | A500K180 Function | $\begin{gathered} \hline \text { A500K270 } \\ \text { Function } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| B19 | I/O | I/O | I/O | D13 | I/O | I/O | I/O |
| B20 | 1/O | 1/O | 1/O | D14 | I/O | 1/0 | I/O |
| B21 | I/O | 1/O | I/O | D15 | I/O | 1/0 | I/O |
| B22 | 1/O | 1/O | 1/0 | D16 | 1/O | 1/0 | 1/O |
| B23 | 1/0 | 1/O | 1/0 | D17 | 1/O | 1/O | I/O |
| B24 | I/O | I/O | I/O | D18 | I/O | I/O | I/O |
| B25 | $V_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $V_{\text {DDP }}$ | D19 | 1/0 | 1/0 | 1/0 |
| B26 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | D20 | I/O | I/O | I/O |
| C1 | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | $V_{\text {DDP }}$ | D21 | I/O | I/O | I/O |
| C2 | I/O | I/O | I/O | D22 | I/O | I/O | I/O |
| C3 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | D23 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ |
| C4 | I/O | I/O | I/O | D24 | I/O | I/O | I/O |
| C5 | 1/O | 1/0 | 1/O | D25 | I/O | I/O | I/O |
| C6 | I/O | 1/O | 1/O | D26 | I/O | I/O | 1/O |
| C7 | 1/O | 1/O | 1/O | E1 | NC | 1/O | I/O |
| C8 | 1/0 | 1/O | 1/O | E2 | I/O | 1/O | I/O |
| C9 | I/O | I/O | 1/O | E3 | I/O | 1/0 | 1/O |
| C10 | 1/0 | I/O | 1/0 | E4 | I/O | I/O | I/O |
| C11 | 1/O | I/O | 1/O | E5 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| C12 | 1/0 | I/O | I/O | E6 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| C13 | 1/0 | I/O | I/O | E7 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| C14 | I/O | I/O | I/O | E8 | $V_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| C15 | 1/0 | 1/O | 1/O | E9 | I/O | I/O | I/O |
| C16 | 1/O | 1/O | 1/O | E10 | I/O | I/O | I/O |
| C17 | I/O | I/O | I/O | E11 | I/O | 1/O | I/O |
| C18 | I/O | I/O | I/O | E12 | I/O | I/O | I/O |
| C19 | 1/0 | 1/O | 1/O | E13 | I/O | 1/O | 1/O |
| C20 | 1/0 | 1/O | 1/O | E14 | I/O | I/O | I/O |
| C21 | 1/0 | I/O | 1/O | E15 | I/O | I/O | I/O |
| C22 | 1/O | I/O | I/O | E16 | I/O | 1/O | I/O |
| C23 | I/O | I/O | I/O | E17 | I/O | I/O | I/O |
| C24 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | E18 | 1/0 | 1/O | 1/0 |
| C25 | I/O | I/O | I/O | E19 | I/O | 1/O | I/O |
| C26 | NC | I/O | 1/0 | E20 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| D1 | NC | I/O | 1/O | E21 | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| D2 | 1/O | 1/O | 1/O | E22 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| D3 | I/O | I/O | I/O | E23 | I/O | 1/O | 1/O |
| D4 | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | $\mathrm{V}_{\text {DDP }}$ | E24 | 1/0 | I/O | I/O |
| D5 | I/O | I/O | 1/O | E25 | 1/O | I/O | I/O |
| D6 | 1/0 | 1/0 | I/O | E26 | I/O | 1/0 | 1/O |
| D7 | 1/O | I/O | 1/O | F1 | 1/0 | 1/O | 1/0 |
| D8 | 1/O | 1/O | 1/0 | F2 | 1/O | 1/0 | 1/O |
| D9 | 1/0 | 1/O | 1/O | F3 | I/O | 1/O | 1/O |
| D10 | 1/O | 1/O | I/O | F4 | I/O | I/O | I/O |
| D11 | 1/0 | 1/0 | 1/0 | F5 | $V_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $V_{\text {DDL }}$ |
| D12 | 1/O | 1/O | 1/O | F22 | $V_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $V_{\text {DDL }}$ |

456-Pin PBGA (Continued)

| Pin Number | $\begin{aligned} & \text { A500K130 } \\ & \text { Function } \end{aligned}$ | $\begin{gathered} \hline \text { A500K180 } \\ \text { Function } \end{gathered}$ | $\begin{gathered} \hline \text { A500K270 } \\ \text { Function } \end{gathered}$ |
| :---: | :---: | :---: | :---: |
| F23 | I/O | I/O | I/O |
| F24 | 1/O | 1/O | 1/O |
| F25 | I/O | 1/O | 1/O |
| F26 | NC | I/O | I/O |
| G1 | NC | 1/O | 1/O |
| G2 | I/O | I/O | 1/O |
| G3 | I/O | I/O | 1/O |
| G4 | I/O | I/O | I/O |
| G5 | $\mathrm{V}_{\text {DDL }}$ | $V_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| G22 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| G23 | I/O | I/O | I/O |
| G24 | 1/O | 1/0 | 1/O |
| G25 | I/O | I/O | I/O |
| G26 | I/O | I/O | I/O |
| H1 | NC | 1/O | 1/O |
| H2 | I/O | I/O | I/O |
| H3 | I/O | 1/0 | 1/O |
| H4 | I/O | I/O | I/O |
| H5 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| H22 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| H23 | I/O | I/O | I/O |
| H24 | I/O | I/O | I/O |
| H25 | I/O | I/O | 1/O |
| H26 | NC | I/O | I/O |
| J1 | I/O | 1/O | 1/O |
| J2 | 1/O | I/O | I/O |
| J3 | I/O | 1/0 | 1/0 |
| J4 | 1/O | I/O | 1/O |
| J5 | 1/O | 1/O | 1/0 |
| J22 | 1/O | 1/O | 1/O |
| J23 | I/O | 1/O | 1/O |
| J24 | I/O | 1/0 | I/O |
| J25 | I/O | 1/O | 1/O |
| J26 | NC | 1/O | 1/O |
| K1 | NC | 1/0 | I/O |
| K2 | I/O | I/O | I/O |
| K3 | I/O | 1/0 | I/O |
| K4 | 1/O | 1/O | 1/O |
| K5 | I/O | 1/O | I/O |
| K22 | I/O | I/O | I/O |
| K23 | I/O | I/O | I/O |
| K24 | I/O | I/O | I/O |
| K25 | 1/O | 1/O | 1/0 |
| K26 | I/O | I/O | 1/O |
| L1 | NC | 1/0 | I/O |
| L2 | I/O | 1/0 | I/O |


| Pin Number | A500K130 Function | A500K180 Function | A500K270 Function |
| :---: | :---: | :---: | :---: |
| L3 | I/O | I/O | I/O |
| L4 | 1/O | 1/O | 1/O |
| L5 | I/O | I/O | I/O |
| L11 | GND | GND | GND |
| L12 | GND | GND | GND |
| L13 | GND | GND | GND |
| L14 | GND | GND | GND |
| L15 | GND | GND | GND |
| L16 | GND | GND | GND |
| L22 | I/O | I/O | I/O |
| L23 | 1/O | I/O | 1/O |
| L24 | I/O | I/O | I/O |
| L25 | I/O | I/O | 1/O |
| L26 | NC | I/O | I/O |
| M1 | GL | GL | GL |
| M2 | GL | GL | GL |
| M3 | I/O | I/O | I/O |
| M4 | I/O | I/O | 1/O |
| M5 | I/O | I/O | I/O |
| M11 | GND | GND | GND |
| M12 | GND | GND | GND |
| M13 | GND | GND | GND |
| M14 | GND | GND | GND |
| M15 | GND | GND | GND |
| M16 | GND | GND | GND |
| M22 | GL | GL | GL |
| M23 | I/O | I/O | I/O |
| M24 | I/O | 1/O | I/O |
| M25 | I/O | I/O | I/O |
| M26 | NC | 1/O | I/O |
| N1 | NC | I/O | 1/O |
| N2 | I/O | I/O | I/O |
| N3 | I/O | I/O | 1/O |
| N4 | I/O | 1/O | 1/O |
| N5 | I/O | I/O | I/O |
| N11 | GND | GND | GND |
| N12 | GND | GND | GND |
| N13 | GND | GND | GND |
| N14 | GND | GND | GND |
| N15 | GND | GND | GND |
| N16 | GND | GND | GND |
| N22 | I/O | I/O | I/O |
| N23 | GL | GL | GL |
| N24 | I/O | I/O | I/O |
| N25 | I/O | 1/O | I/O |
| N26 | I/O | I/O | I/O |

## 456-Pin PBGA (Continued)

| Pin Number | $\begin{aligned} & \hline \text { A500K130 } \\ & \text { Function } \end{aligned}$ | $\begin{gathered} \hline \text { A500K180 } \\ \text { Function } \end{gathered}$ | $\begin{aligned} & \hline \text { A500K270 } \\ & \text { Function } \end{aligned}$ | Pin Number | $\begin{gathered} \hline \text { A500K130 } \\ \text { Function } \end{gathered}$ | A500K180 Function | $\begin{gathered} \hline \text { A500K270 } \\ \text { Function } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P1 | NC | I/O | I/O | T23 | I/O | I/O | I/O |
| P2 | I/O | 1/O | 1/O | T24 | 1/O | 1/O | 1/O |
| P3 | 1/O | 1/O | 1/O | T25 | 1/O | 1/O | 1/O |
| P4 | I/O | I/O | 1/O | T26 | I/O | 1/O | 1/O |
| P5 | I/O | I/O | I/O | U1 | NC | I/O | I/O |
| P11 | GND | GND | GND | U2 | I/O | 1/0 | 1/O |
| P12 | GND | GND | GND | U3 | I/O | I/O | I/O |
| P13 | GND | GND | GND | U4 | 1/O | 1/O | 1/O |
| P14 | GND | GND | GND | U5 | 1/O | 1/O | 1/O |
| P15 | GND | GND | GND | U22 | I/O | 1/O | 1/O |
| P16 | GND | GND | GND | U23 | 1/O | I/O | 1/O |
| P22 | I/O | I/O | I/O | U24 | 1/O | 1/O | 1/O |
| P23 | I/O | I/O | 1/O | U25 | I/O | I/O | 1/O |
| P24 | I/O | I/O | I/O | U26 | NC | I/O | I/O |
| P25 | I/O | 1/O | 1/O | V1 | I/O | 1/O | 1/O |
| P26 | NC | I/O | I/O | V2 | I/O | I/O | 1/O |
| R1 | I/O | 1/O | 1/O | V3 | 1/O | 1/O | 1/O |
| R2 | I/O | I/O | I/O | V4 | I/O | I/O | I/O |
| R3 | I/O | I/O | I/O | V5 | I/O | I/O | I/O |
| R4 | I/O | I/O | I/O | V22 | 1/O | 1/O | 1/O |
| R5 | I/O | I/O | I/O | V23 | 1/O | 1/O | 1/O |
| R11 | GND | GND | GND | V24 | 1/O | 1/O | 1/O |
| R12 | GND | GND | GND | V25 | I/O | 1/O | 1/O |
| R13 | GND | GND | GND | V26 | NC | I/O | I/O |
| R14 | GND | GND | GND | W1 | NC | I/O | I/O |
| R15 | GND | GND | GND | W2 | I/O | 1/O | 1/O |
| R16 | GND | GND | GND | W3 | I/O | 1/O | 1/O |
| R22 | I/O | I/O | I/O | W4 | I/O | I/O | I/O |
| R23 | 1/0 | 1/0 | 1/0 | W5 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| R24 | 1/0 | 1/O | 1/0 | W22 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| R25 | I/O | I/O | I/O | W23 | I/O | I/O | I/O |
| R26 | NC | I/O | 1/O | W24 | I/O | 1/O | 1/O |
| T1 | NC | I/O | I/O | W25 | I/O | I/O | I/O |
| T2 | I/O | I/O | I/O | W26 | I/O | I/O | 1/O |
| T3 | I/O | I/O | I/O | Y1 | NC | I/O | 1/O |
| T4 | 1/O | I/O | 1/O | Y2 | I/O | I/O | 1/O |
| T5 | I/O | I/O | I/O | Y3 | I/O | I/O | I/O |
| T11 | GND | GND | GND | Y4 | I/O | I/O | I/O |
| T12 | GND | GND | GND | Y5 | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| T13 | GND | GND | GND | Y22 | $V_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ | $\mathrm{V}_{\text {DDL }}$ |
| T14 | GND | GND | GND | Y23 | I/O | I/O | I/O |
| T15 | GND | GND | GND | Y24 | 1/O | 1/O | 1/O |
| T16 | GND | GND | GND | Y25 | I/O | 1/O | 1/O |
| T22 | I/O | I/O | I/O | Y26 | NC | I/O | I/O |

## Package Mechanical Drawings

208-Pin PQFP


Side View


Detail A


Plastic Quad Flat Pack

| Jedec Equiv | PQFP 208 |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Dimension | Min. | Nom. | Max. |  |
| A |  | 3.70 | 4.10 |  |
| A1 | 0.25 | 0.38 |  |  |
| A2 | 3.20 | 3.40 | 3.60 |  |
| b | 0.17 |  | 0.27 |  |
| C | 0.09 |  | 0.20 |  |
| ccc |  |  | 0.10 |  |
| D/E | 30.25 | 30.60 | 30.85 |  |
| D1/E1 | 27.90 | 28.00 | 28.10 |  |
| e | 0.50 BSC |  |  |  |
| L | 0.50 | 0.60 | 0.75 |  |
| Theta | 0 |  |  |  |
|  |  |  |  |  |

Notes:

1. All dimensions are in millimeters.
2. BSC-Basic Spacing between Centers.

## Package Mechanical Drawings (Continued)

## 272-Pin PBGA



Bottom View


Detail A


## Package Mechanical Drawings (Continued)

## 456-Pin PBGA



Plastic Ball Grid Array

| JEDEC Equivalent | PBGA 272 |  |  | PBGA 456 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Dimension | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | 2.18 | 2.33 | 2.50 | 2.13 | 2.33 | 2.50 |
| A1 | 0.50 | 0.60 | 0.70 | 0.50 | 0.60 | 0.70 |
| A2 | 1.15 | 1.17 | 1.19 | 1.12 | 1.17 | 1.19 |
| aaa |  |  | 0.15 |  |  | 0.15 |
| b | 0.60 | 0.75 | 0.90 | 0.60 | 0.75 | 0.90 |
| bbb |  |  | 0.20 |  |  | 0.20 |
| c | 0.53 | 0.56 | 0.61 | 0.51 | 0.56 | 0.61 |
| ccc |  |  | 0.25 |  |  | 0.25 |
| D | 26.80 | 27.00 | 27.20 | 34.80 | 35.00 | 35.20 |
| D1 |  | 4.13 BS |  |  | 1.75 BS |  |
| D2 | 23.90 | 24.00 | 24.10 | 29.80 | 30.00 | 30.20 |
| E | 26.80 | 27.00 | 27.20 | 34.80 | 35.00 | 35.20 |
| E1 | 24.13 BSC |  |  | 31.75 BSC |  |  |
| E2 | 23.90 | 24.00 | 24.10 | 29.80 | 30.00 | 30.20 |
| e | 1.27 typ. |  |  | 1.27 typ. |  |  |
| Theta | $30^{\circ}$ typ. |  |  | $30^{\circ}$ typ. |  |  |

## Notes:

1. All dimensions are in millimeters
2. BSC-Basic Spacing between Centers

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[^0]:    1. If $V_{D D P}=2.5 \mathrm{~V}$, pads are compliant to 2.5V level signals as defined by JEDEC JESD 8-5.
[^1]:    2. Available after completion of full qualification/characterization 2H, 2000
[^2]:    Notes: Not all signals shown are used in all modes.

[^3]:    Notes:

    1. At fast cycles, $E W R A, F W R A=M A X(7.5 \mathrm{~ns}-W R L), 3.0 \mathrm{~ns}$
    2. At fast cycles, WRRDS (for enabling write) $=$ MAX $(7.5 \mathrm{~ns}-$ RDL $), 3.0 \mathrm{~ns}$
