TRANSMAGNETICS
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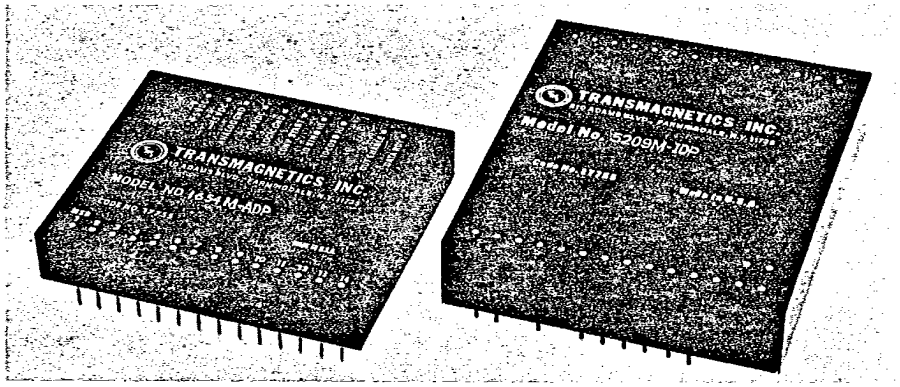
SERIES 5209

Revised April 1988

14 BIT, MUX SYNCHRO/RESOLVER TO DIGITAL CONVERTER SYSTEM

(4, 6, 8 OR MORE CHANNELS)



FEATURES

- 14 bit resolution
- 6 arc minutes accuracy
- Noise immune, not a peak sampler
- Insensitive to carrier amplitude variations
- Tristate outputs simplify computer interconnect
- Fully interchangeable modules
- Hermetically sealed units available
- Meets MIL-STD-202D: Methods, 101C, 105B, 106C, 107C, 202D, 204B and 205D
- Hi-Reliability 883B or MIL-M-38510 units on request
- Expandable by adding additional Demodulator Modules
- No special precautions required against static electricity

CONCEPT

Multiplexing is a method or system for processing several data inputs, either randomly or sequentially, through a switching matrix, and time sharing a common output to view each input in a time slot determined by the multiplexer address.

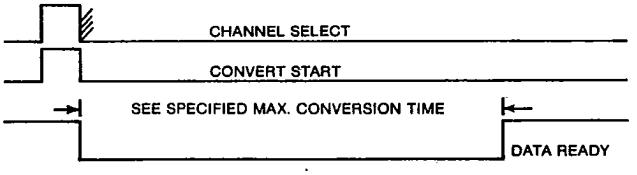
DESCRIPTION

This model describes a time proven multiplexed system using a continuous demodulation rather than a peak sampling approach. This technique assures accuracy, even though system noise is present, because peak samplers respond to perturbations on the sampled waveform with resulting deterioration of output accuracy.

This system consists of two potted, but factory repairable, modules that are designed for PC board mounting. The Demodulator module 5209 converts the four input channels into DC sine/cosine format. A switching matrix, contained within the Demodulator module, selects the particular input channel that will be converted into digital form. Each channel incorporates transformer isolated signal and reference inputs and can operate from different reference supplies. Any reference and input voltage level and frequency can be supplied. The successive approximation converter module 1654 accepts the selected DC sine/cosine input signal and upon receipt of a Convert Command digitizes the input into a binary coded word. A handshake Data Ready indicates that conversion was completed. No matching of modules is required. Any demodulator module will work with any Digitizer module, thus simplifying spare parts requirements. No calibrations, adjustments or warm-up are required. The number of input channels may be increased by adding additional Demodulator modules.
For a 12 bit version see Series 5210.
For a 10 bit version see Series 5309.

MULTIPLEXING SEQUENCE

1. Select channel by setting appropriate address logic.
2. Institute Convert Command.
3. Within the specified max. conversion time, the Data Ready Line will go High
4. Ground Tristate Enable to connect outputs to Data Lines.
5. Repeat.



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SPECIFICATIONS

Resolution:	14 bits
Accuracy:	±6 arc minutes
Reference:	See Input/Reference Code
Input:	See Input/Reference Code
Input Z:	40K min.
Logic:	Parallel, positive, TTL or CMOS compatible binary coded angle
Output Mode:	Tristate. Fan Out: 2 LPTTL Loads. Ground Tristate "Enable" to activate outputs.
Conversion Time:	*150 μs per channel. (See part number designation).
Dynamic Lag:	40 arc seconds/rpm (400 Hz units)
Convert Command:	Positive TTL level pulse of 5.0 μs min width. Triggers at trailing edge. Fan In: 1 LPTTL.
Data Ready:	A transition from "0" to "1" indicates that conversion is complete and that data is ready. Output stays high and data remains valid until next Convert Start. Fan Out: 2 LPTTL Loads.
Channel Address:	500 ns typical
Channel Access:	Random or sequential
Channel Address Logic:	2 Lines
Fan In:	1 LPTTL Load
Isolation:	Reference and inputs are transformer isolated.
Power Requirement:	±15 VDC ±5% at 60 mA. ±12 VDC option is available. +5 VDC ±5% at 20 mA
Operating Temperature:	-55°C to +85°C
Storage Temperature:	-55°C to +105°C
Grounds:	Separate analog and logic grounds are supplied to minimize potential ground loop problems.
Potting:	Potting is available for high shock or vibration environments. See part number designation.
Size:	2 Channel Demodulator: 3.125 x 3.625 x .42 4 Channel Demodulator: 3.125 x 3.625 x .82 4 Channel 50/60 Hz Demodulator: 3.625 x 4.750 x .82 Digitizer: 3.125 x 3.625 x .42

*Conversion time can be supplied as low as 150μs/channel. However, good engineering practice dictates the use of the maximum conversion time allowed by the system because a longer conversion time enables additional filtering to be added to the converter.

ORDERING INFORMATION:

DEMODULATOR

(One required for 4 channels, two for 8 channels, etc.)

5209 *-*****

- Add 883 for Hi-Rel
- Add P for Potting
- Add H for Hermetically Sealed
- Add D for separate logic ground
- See table for Input/Ref code
- Temperature Range (C or M)
- Add A to specify a two channel demodulator

DIGITIZER

B1654 *-******-*

- Conversion time (see chart)
- Add 883 for Hi-Rel
- Add P for Potting
- Add H for Hermetically Sealed
- Add D for separate logic ground
- Resolution (A = 14 bits)
- Temperature Range (C or M)

CONVERSION TIME CHART

DASH #	CONVERT TIME
None	150μs
-1	1ms
-2	1ms
-3	250μs

INPUT/REFERENCE CODE

	Channel 1				Channel 2				Channel 3				Channel 4			
Code	Type	Input (VL-L)	Ref Vrms)	Freq.	Type	Input (VL-L)	Ref (Vrms)	Freq.	Type	Input (VL-L)	Ref (Vrms)	Freq.	Type	Input (VL-L)	Ref (Vrms)	Freq.
-1	Syn	90	115	400	Syn	90	115	400	Syn	90	115	400	Syn	90	115	400
-2	Syn	11.8	26	400	Syn	11.8	26	400	Syn	11.8	26	400	Syn	11.8	26	400
-3	Syn	11.8	115	400	Syn	11.8	115	400	Syn	11.8	115	400	Syn	11.8	115	400
-5*	Syn	90	115	50/400	Syn	90	115	50/60	Syn	90	115	50/60	Syn	90	115	50/60
-6	Rsvr	11.8	26	400	Rsvr	11.8	26	400	Syn	11.8	26	400	Syn	11.8	26	400
-7	Syn	11.8	26	1200	Syn	11.8	26	1200	Syn	11.8	26	1200	Syn	11.8	26	1200

*Size increased to 3.125 x 4.750 x .82" Reference Voltage Tolerance: ±10% Frequency Tolerance: ±10%

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