PRELIMINARY

Am486® DXL

High-Performance, 32-Bit Microprocessor with Integrated Power Management

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Operating voltage range 5.0 V ± 5%**
  - — 40-MHz operating frequencies
  - — Wide range of chipsets and support available through the AMD® FusionPC℠ Program
- **High Integration On-Chip**
  - — 8-Kbyte code and data cache
  - — Floating-point unit
  - — Paged, virtual memory management
- **High-performance Design**
  - — Frequent instructions execute in one clock
  - — 128-Million bytes/second burst bus at 40 MHz
  - — 0.7-micron CMOS process technology
  - — Dynamic bus sizing for 8-, 16-, and 32-bit buses
- **Complete 32-bit Architecture**
  - — Address and data buses
  - — All registers
  - — 8-, 16-, and 32-bit data types
- **Standard 168-Pin PGA Package**
- **Multiprocessor Support**
  - — Multiprocessor instructions
  - — Cache consistency protocols
  - — Support for second-level cache
- **System Management Mode (SMM) for system and power management**
  - — System Management Interrupt ($\overline{SMI}$) for power management independent of processor operating mode and operating system
  - — $\overline{SMI}$ is a non-maskable interrupt that has higher priority than NMI.
  - — Automatic save and restore of microprocessor state
  - — Wide range of chipsets supporting SMM available to allow product differentiation
- **Environmental Protection Agency's 'Energy Star' program compliant**
  - — Energy management capability provides excellent base for energy-efficient design
  - — Works with a variety of energy-efficient power management devices

GENERAL DESCRIPTION

The Am486DXL microprocessor is an implementation of the 486DX with integrated SMM power management. The operating voltage range is 5.0 V ± 5%. The price/performance of the full 32-bit processor and floating-point unit provides the best value for designing high-volume, mainstream 486 low-powered desktop PCs.

The Am486DXL CPU operates with a 1X clock input. This 1X clock simplifies system design by cutting in half the clock frequency required by external devices. The 1X clock also reduces RF emission and simplifies clock generation.

The phases of the core clock are provided by an internal Phase Lock Loop (PLL) circuit.

SMM is provided as a mechanism to interrupt the microprocessor operation and resume the interrupted operation transparent to the operating system or application running on the system. The Am486DXL microprocessor supports the Microsoft® Advanced Power Management specification for new "power managed" applications.

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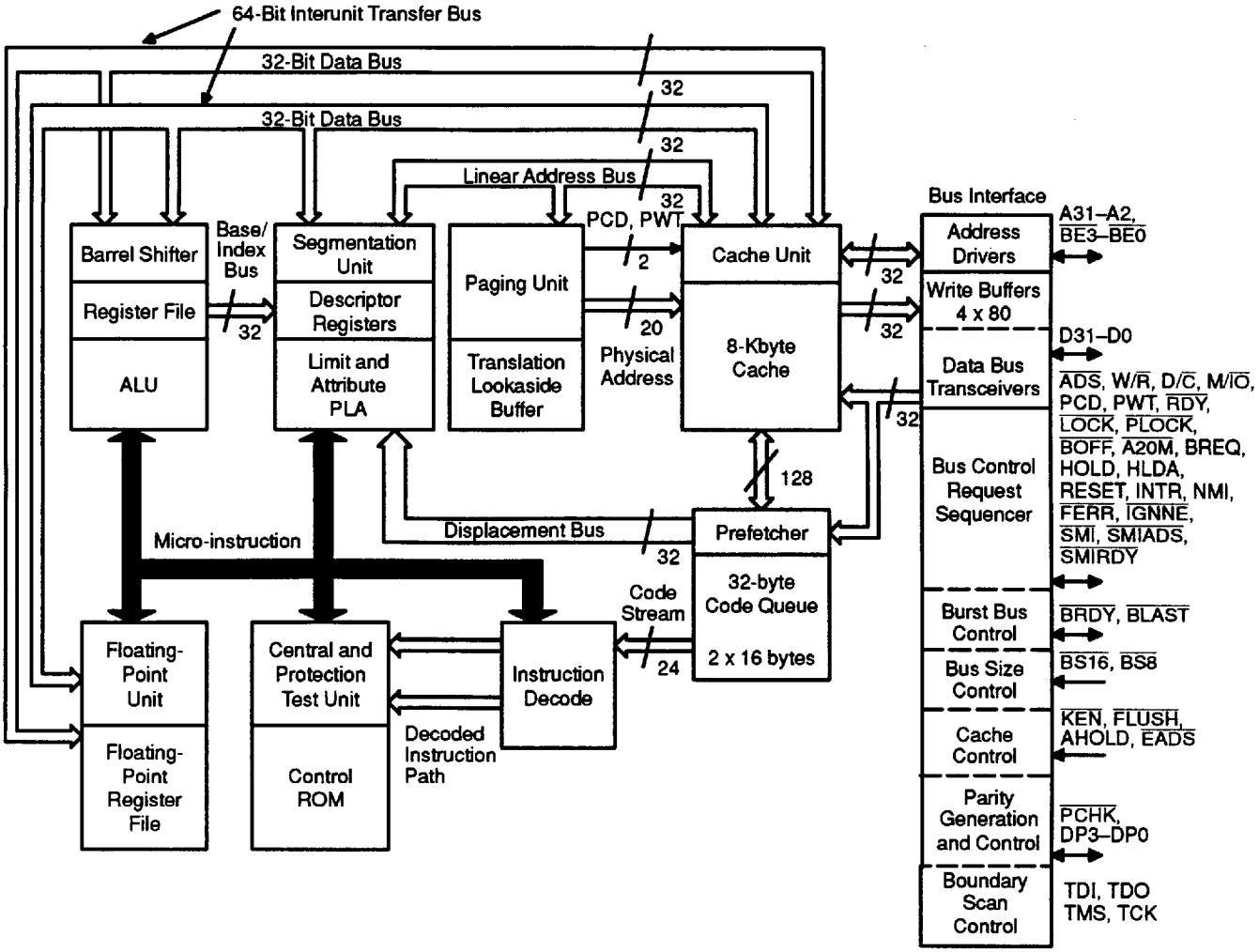
Issue Date: April 1994

BLOCK DIAGRAM

Am486DXL Microprocessor Pipelined 32-bit Microarchitecture



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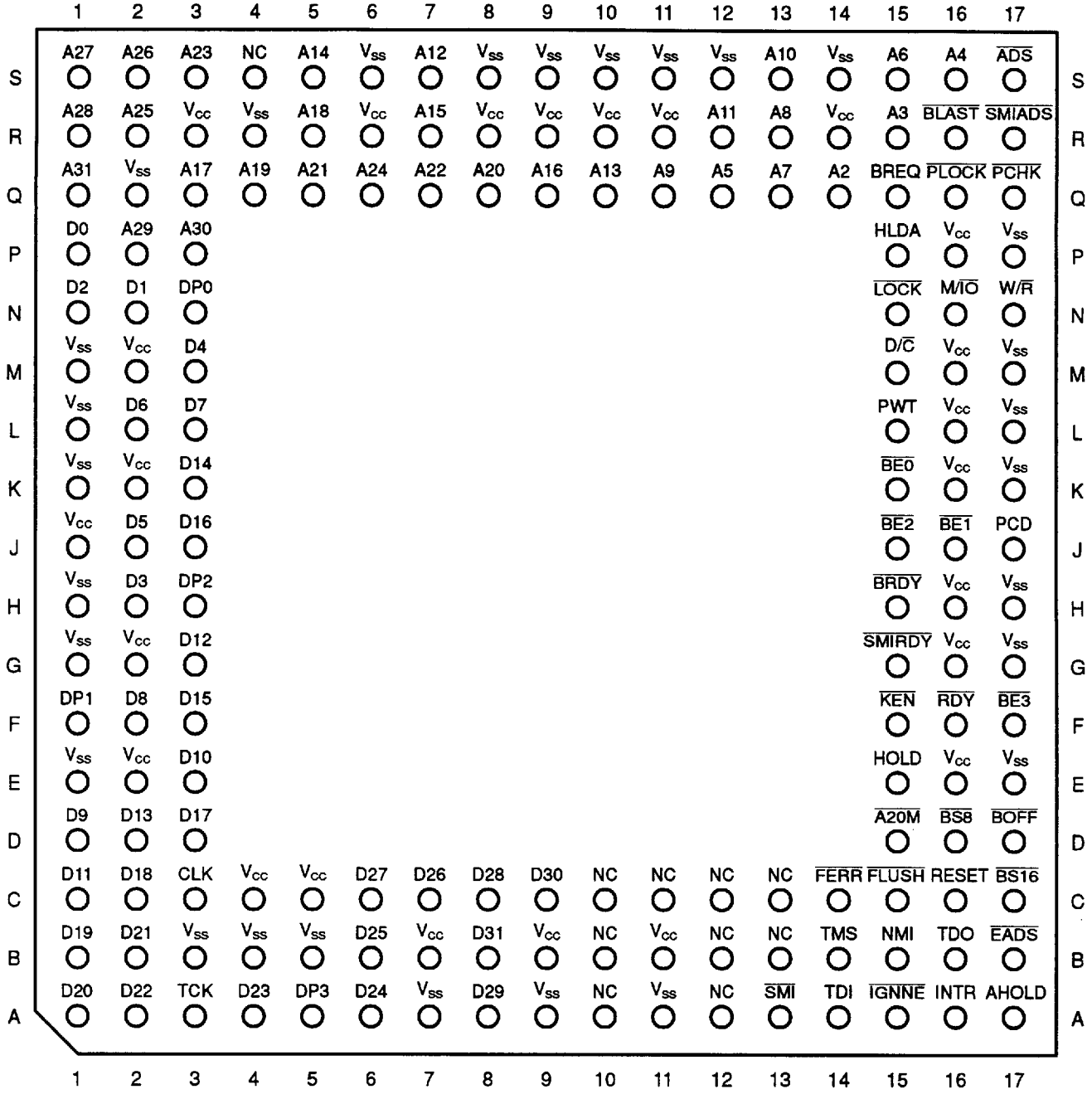
CONNECTION DIAGRAMS
Am486DXL CPU
Pin Side View

168-Pin PGA (Pin Grid Array) Package



Note:
NC = Not connected. To guarantee functionality with future revisions, these pins must not be connected.

17852A–002

CONNECTION DIAGRAMS
Am486DXL CPU
Top Side View

168-Pin PGA (Pin Grid Array) Package

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
S	$\overline{ADS}$	A4	A6	V_{SS}	A10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A12	V_{SS}	A14	NC	A23	A26	A27	S
R	$\overline{SMIADS}$	$\overline{BLAST}$	A3	V_{CC}	A8	A11	V_{CC}	V_{CC}	V_{CC}	V_{CC}	A15	V_{CC}	A18	V_{SS}	V_{CC}	A25	A28	R
Q	$\overline{PCHK}$	$\overline{PLOCK}$	BREQ	A2	A7	A5	A9	A13	A16	A20	A22	A24	A21	A19	A17	V_{SS}	A31	Q
P	V_{SS}	V_{CC}	HLDA												A30	A29	D0	P
N	W/$\overline{R}$	M/$\overline{IO}$	$\overline{LOCK}$												DP0	D1	D2	N
M	V_{SS}	V_{CC}	D/$\overline{C}$												D4	V_{CC}	V_{SS}	M
L	V_{SS}	V_{CC}	PWT												D7	D6	V_{SS}	L
K	V_{SS}	V_{CC}	$\overline{BE0}$												D14	V_{CC}	V_{SS}	K
J	PCD	$\overline{BE1}$	$\overline{BE2}$												D16	D5	V_{CC}	J
H	V_{SS}	V_{CC}	$\overline{BRDY}$												DP2	D3	V_{SS}	H
G	V_{SS}	V_{CC}	$\overline{SMIRDY}$												D12	V_{CC}	V_{SS}	G
F	$\overline{BE3}$	$\overline{RDY}$	$\overline{KEN}$												D15	D8	DP1	F
E	V_{SS}	V_{CC}	HOLD												D10	V_{CC}	V_{SS}	E
D	$\overline{BOFF}$	$\overline{BS8}$	$\overline{A20M}$												D17	D13	D9	D
C	$\overline{BS16}$	RESET	$\overline{FLUSH}$	$\overline{FERR}$	NC	NC	NC	NC	D30	D28	D26	D27	V_{CC}	V_{CC}	CLK	D18	D11	C
B	$\overline{EADS}$	TDO	NMI	TMS	NC	NC	V_{CC}	NC	V_{CC}	D31	V_{CC}	D25	V_{SS}	V_{SS}	V_{SS}	D21	D19	B
A	AHOLD	INTR	$\overline{IGNNE}$	TDI	$\overline{SMI}$	NC	V_{SS}	NC	V_{SS}	D29	V_{SS}	D24	DP3	D23	TCK	D22	D20	A
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Note:
NC = Not connected. To guarantee functionality with future revisions, these pins must not be connected.

17852A–003

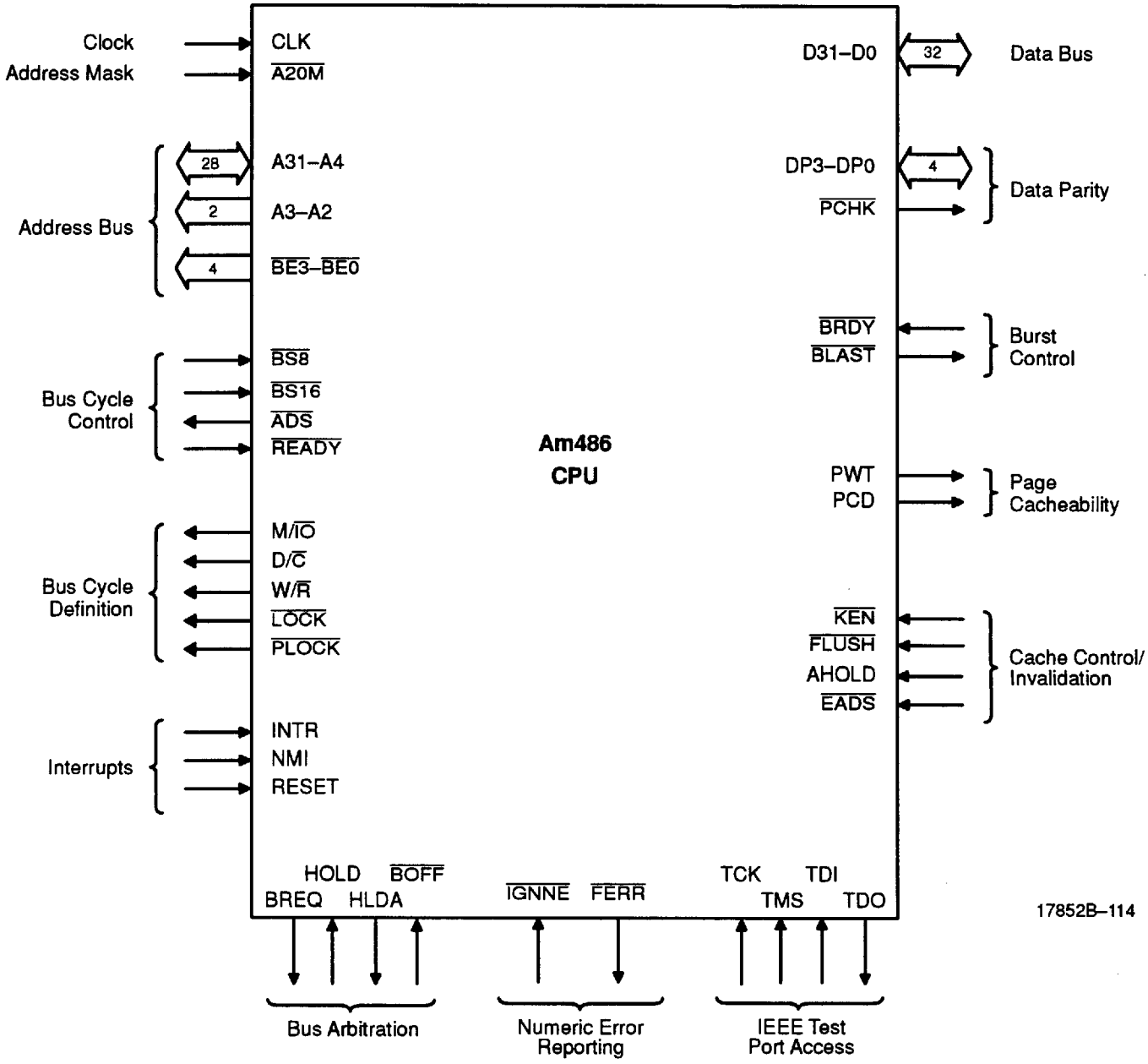
PIN DESIGNATIONS (Functional Grouping)

Address		Data		Control		Test		NC	5-V V_{cc}	V_{ss}
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.
A2	Q-14	D0	P-1	$\overline{A20M}$	D-15	TCK	A-3	A-10	B-7	A-7
A3	R-15	D1	N-2	$\overline{ADS}$	S-17	TDI	A-14	A-12	B-9	A-9
A4	S-16	D2	N-1	AHOLD	A-17	TDO	B-16	B-10	B-11	A-11
A5	Q-12	D3	H-2	$\overline{BE0}$	K-15	TMS	B-14	B-12	C-4	B-3
A6	S-15	D4	M-3	$\overline{BE1}$	J-16			B-13	C-5	B-4
A7	Q-13	D5	J-2	$\overline{BE2}$	J-15			C-10	E-2	B-5
A8	R-13	D6	L-2	$\overline{BE3}$	F-17			C-11	E-16	E-1
A9	Q-11	D7	L-3	$\overline{BLAST}$	R-16			C-12	G-2	E-17
A10	S-13	D8	F-2	$\overline{BOFF}$	D-17			C-13	G-16	G-1
A11	R-12	D9	D-1	$\overline{BRDY}$	H-15			S-4	H-16	G-17
A12	S-7	D10	E-3	BREQ	Q-15				J-1	H-1
A13	Q-10	D11	C-1	$\overline{BS8}$	D-16				K-2	H-17
A14	S-5	D12	G-3	$\overline{BS16}$	C-17				K-16	K-1
A15	R-7	D13	D-2	CLK	C-3				L-16	K-17
A16	Q-9	D14	K-3	D/$\overline{C}$	M-15				M-2	L-1
A17	Q-3	D15	F-3	DP0	N-3				M-16	L-17
A18	R-5	D16	J-3	DP1	F-1				P-16	M-1
A19	Q-4	D17	D-3	DP2	H-3				R-3	M-17
A20	Q-8	D18	C-2	DP3	A-5				R-6	P-17
A21	Q-5	D19	B-1	$\overline{EADS}$	B-17				R-8	Q-2
A22	Q-7	D20	A-1	$\overline{FERR}$	C-14				R-9	R-4
A23	S-3	D21	B-2	$\overline{FLUSH}$	C-15				R-10	S-6
A24	Q-6	D22	A-2	HLDA	P-15				R-11	S-8
A25	R-2	D23	A-4	HOLD	E-15				R-14	S-9
A26	S-2	D24	A-6	$\overline{IGNNE}$	A-15					S-10
A27	S-1	D25	B-6	INTR	A-16					S-11
A28	R-1	D26	C-7	$\overline{KEN}$	F-15					S-12
A29	P-2	D27	C-6	$\overline{LOCK}$	N-15					S-14
A30	P-3	D28	C-8	M/$\overline{IO}$	N-16					
A31	Q-1	D29	A-8	NMI	B-15					
		D30	C-9	PCD	J-17					
		D31	B-8	$\overline{PCHK}$	Q-17					
				PWT	L-15					
				$\overline{PLOCK}$	Q-16					
				$\overline{RDY}$	F-16					
				RESET	C-16					
				W/$\overline{R}$	N-17					

Superset Pins

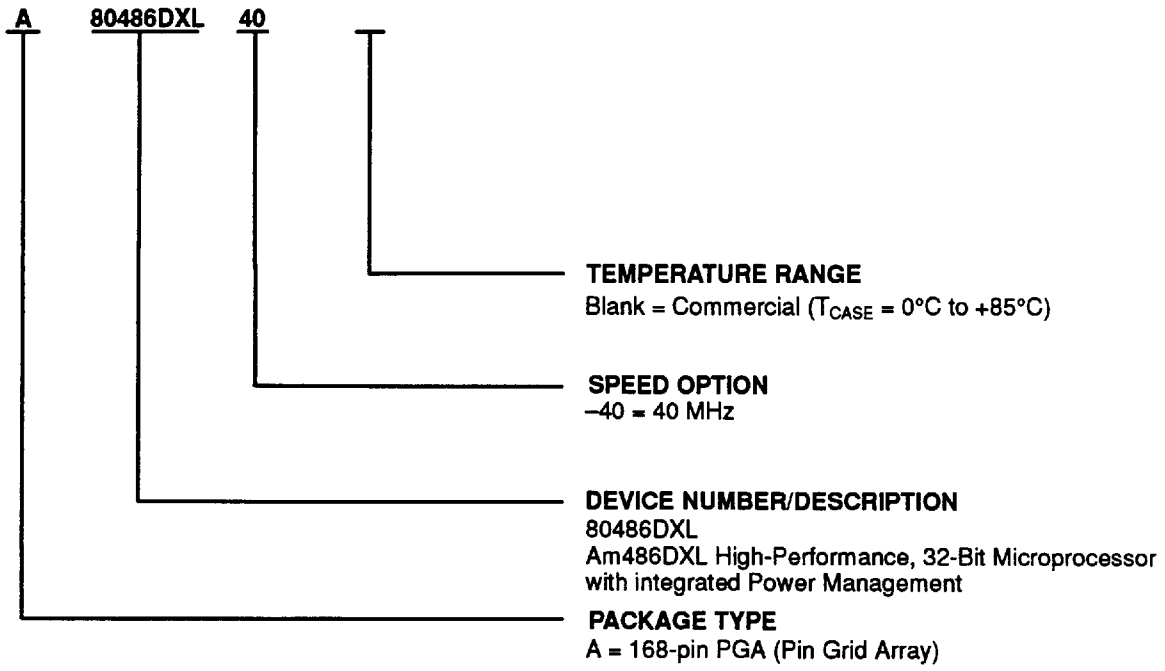
Pin Name	Pin No.
$\overline{SMI}$	A-13
$\overline{SMIADS}$	R-17
$\overline{SMIRDY}$	G-15

LOGIC SYMBOL



ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
A	80486DXL	–40

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTIONS

A31–A4/A3–A2

Address Lines (Inputs/Outputs)/(Outputs)

A31–A2, together with the byte enables $\overline{BE3}$–$\overline{BE0}$, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the microprocessor to perform cache line invalidations. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.

$\overline{A20M}$

Address Bit 20 Mask (Active Low; Input)

When asserted, the Am486DXL microprocessor masks physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. $\overline{A20M}$ emulates the address wraparound at 1 Mbyte, which occurs on the 8086. $\overline{A20M}$ is active Low and should be asserted only when the processor is in Real Mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, $\overline{A20M}$ should be sampled High at the falling edge of RESET.

All SMM address space cycles made by the Am486DXL microprocessor are 32-bit accesses. The Am486DXL CPU effectively ignores the state of $\overline{A20M}$ while performing transfers to and from SMM memory space, but recognizes $\overline{A20M}$ during UMOV instruction accesses between SMM and the normal address space.

$\overline{ADS}$

Address Status (Active Low; Output)

$\overline{ADS}$ indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. $\overline{ADS}$ is driven active in the same clock as the addresses are driven. $\overline{ADS}$ is active Low and is not driven during bus hold.

AHOLD

Address Hold (Input)

This request allows another bus master access to the Am486DXL microprocessor's address bus for a cache invalidation cycle. The Am486DXL microprocessor stops driving its address bus in the clock following AHOLD going active. Only the address bus is floated during address hold; the remainder of the bus remains active. AHOLD is active High and is provided with a small internal pull-down resistor. For proper operation, AHOLD must meet setup and hold times t_{18} and t_{19}.

$\overline{BE3}$–$\overline{BE0}$

Byte Enables (Active Low; Outputs)

These pins indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. $\overline{BE3}$ applies to D31–D24, $\overline{BE2}$ applies to D23–D16, $\overline{BE1}$ applies to D15–D8, and $\overline{BE0}$ applies to D7–D0. $\overline{BE3}$–$\overline{BE0}$ are active Low and are not driven during bus hold.

$\overline{BS8}$/$\overline{BS16}$

Bus Size 8 (Active Low; Input)/
Bus Size 16 (Active Low; Input)

These pins cause the Am486DXL microprocessor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The state of these pins in the clock before $\overline{RDY}$ is used by the Am486DXL microprocessor to determine the bus size. These signals are active Low and are provided with internal pull-up resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.

All SMM address space cycles made by the Am486DXL microprocessor are 32-bit accesses. The Am486DXL CPU ignores $\overline{BS16}$ and $\overline{BS8}$ during cycles directed to the SMM address space, but recognizes $\overline{BS16}$ during UMOV instruction accesses between SMM and the normal address space.

$\overline{BLAST}$

Burst Last (Active Low; Output)

$\overline{BLAST}$ indicates that the next time $\overline{BRDY}$ is returned, then the burst bus cycle is complete. $\overline{BLAST}$ is active for both burst and non-burst bus cycles. $\overline{BLAST}$ is active Low and is not driven during bus hold.

$\overline{BOFF}$

Backoff (Active Low; Input)

This input pin forces the Am486DXL microprocessor to float its bus in the next clock. The microprocessor floats all pins normally floated during bus hold, but HLDA is not asserted in response to $\overline{BOFF}$. $\overline{BOFF}$ has higher priority than $\overline{RDY}$ or $\overline{BRDY}$; if both are returned in the same clock, $\overline{BOFF}$ takes effect. The microprocessor remains in bus hold until $\overline{BOFF}$ is negated. If a bus cycle was in progress when $\overline{BOFF}$ was asserted, the cycle is restarted. $\overline{BOFF}$ is active Low and must meet setup and hold times t_{18} and t_{19} for proper operation.

$\overline{BRDY}$

Burst Ready Input (Active Low; Input)

This input pin performs the same cycle during a burst cycle that $\overline{RDY}$ performs during a non-burst cycle. $\overline{BRDY}$ indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to write. $\overline{BRDY}$ is ignored when the bus is idle and at the end of the first clock in a bus cycle.

$\overline{BRDY}$ is sampled in the second and subsequent clocks of a burst cycle. The data presented on the data bus is strobed into the microprocessor when $\overline{BRDY}$ is sampled active. If $\overline{RDY}$ is returned simultaneously with $\overline{BRDY}$, $\overline{BRDY}$ is ignored and the burst cycle is prematurely aborted.

$\overline{BRDY}$ is active Low and is provided with a small pull-up resistor. $\overline{BRDY}$ must satisfy the setup and hold times t_{16} and t_{17}.

BREQ

Internal Cycle Pending (Output)

BREQ indicates that the Am486DXL microprocessor has internally generated a bus request. BREQ is generated whether or not the Am486DXL microprocessor is driving the bus. BREQ is active High and is never floated, except during three-state test mode (see $\overline{FLUSH}$).

CLK

Clock (Input)

CLK is a 1X clock providing the fundamental timing and the internal operating frequency for the Am486DXL microprocessor. All external timing parameters are specified with respect to the rising edge of CLK.

D31–D0

Data Lines (Inputs/Outputs)

Lines D7–D0 define the least significant byte of the bus while lines D31–D24 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.

D/$\overline{C}$

Data/Control (Output)

This bus cycle definition pin distinguishes data cycles, either memory or I/O, from control cycles. These control cycles are: interrupt acknowledge, halt, and instruction fetching.

DP3–DP0

Data Parity (Inputs/Outputs)

Data parity is generated on all write data cycles with the same timing as the data driven by the Am486DXL microprocessor. Even parity information must be driven back into the microprocessor on the data parity pins with the same timing as read information to ensure that the correct parity check status is indicated by the Am486DXL microprocessor. The signals read on these pins do not affect program execution.

Input signals must meet setup and hold times t_{22} and t_{23}. DP3–DP0 should be connected to V_{CC} through a pull-up resistor in systems not using parity. DP3–DP0 are active High and are driven during the second and subsequent clocks of write cycles.

$\overline{EADS}$

Valid External Address (Active Low; Input)

This pin indicates a valid external address has been driven onto the Am486DXL microprocessor address pins. This address is used to perform an internal cache invalidation cycle. $\overline{EADS}$ is active Low and is provided with an internal pull-up resistor. $\overline{EADS}$ must satisfy setup and hold times t_{12} and t_{13} for proper operation.

$\overline{FERR}$

Floating-Point Error (Active Low; Output)

Driven active when a floating-point error occurs. $\overline{FERR}$ is similar to the $\overline{ERROR}$ pin on a 387 math coprocessor. $\overline{FERR}$ is included for compatibility with systems using DOS-type floating-point error reporting. $\overline{FERR}$ is active Low and is not floated during bus hold, except during three-state test mode (see $\overline{FLUSH}$).

$\overline{FLUSH}$

Cache Flush (Active Low; Input)

$\overline{FLUSH}$ forces the Am486DXL microprocessor to flush its entire internal cache. $\overline{FLUSH}$ is active Low and need only be asserted for one clock. $\overline{FLUSH}$ is asynchronous, but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock. $\overline{FLUSH}$ being sampled Low in the clock before the falling edge of RESET causes the Am486DXL microprocessor to enter the three-state test mode.

HLDA

Hold Acknowledge (Output)

HLDA goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the Am486DXL microprocessor has given the bus to another local bus master. HLDA is driven active in the same clock that the Am486DXL microprocessor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active High and remains driven during bus hold. HLDA is never floated, except during three-state test mode (see $\overline{FLUSH}$).

HOLD

Bus Hold Request (Input)

This input pin allows another bus master complete control of the Am486DXL microprocessor bus. In response to HOLD going active, the Am486DXL microprocessor floats most of its output and input/output pins. HLDA is asserted after completing the current bus cycle, burst cycle, or sequence of locked cycles. The Am486DXL microprocessor remains in this state until HOLD is deasserted. HOLD is active High and is not provided with

an internal pull-down resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.

$\overline{\text{IGNNE}}$

Ignore Numeric Error (Active Low; Input)

When this pin is asserted, the Am486DXL microprocessor will ignore a numeric error and continue executing non-control floating-point instructions. When $\overline{\text{IGNNE}}$ is deasserted, the Am486DXL microprocessor will freeze on a non-control floating-point instruction if a previous floating-point instruction caused an error. $\overline{\text{IGNNE}}$ has no effect when the NE bit in Control Register 0 is set. $\overline{\text{IGNNE}}$ is active Low and is provided with a small internal pull-up resistor. $\overline{\text{IGNNE}}$ is asynchronous but setup and hold times t_{20} and t_{21} must be met to ensure recognition on any specific clock.

INTR

Maskable Interrupt (Input)

INTR indicates an external interrupt has been generated. If the internal interrupt flag is set in EFLAGS, active interrupt processing is initiated. The Am486DXL microprocessor generates two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to ensure that the interrupt is recognized. INTR is active High and is not provided with an internal pull-down resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

$\overline{\text{KEN}}$

Cache Enable (Active Low; Input)

$\overline{\text{KEN}}$ is used to determine whether the current cycle is cacheable. When the Am486DXL microprocessor generates a cacheable cycle and $\overline{\text{KEN}}$ is active, the cycle becomes a cache line fill cycle. Returning $\overline{\text{KEN}}$ active one clock before $\overline{\text{RDY}}$ during the last read in the cache line fill causes the line to be placed in the on-chip cache. $\overline{\text{KEN}}$ is active Low and is provided with a small internal pull-up resistor. $\overline{\text{KEN}}$ must satisfy setup and hold times t_{14} and t_{15} for proper operation.

All SMM address space cycles made by the Am486DXL CPU are 32-bit accesses. The Am486DXL CPU effectively ignores the state of $\overline{\text{KEN}}$ *while performing transfers to and from SMM memory space, but recognizes* $\overline{\text{KEN}}$ *during UMOV instruction accesses between SMM and the normal address space.*

$\overline{\text{LOCK}}$

Bus Lock (Active Low; Output)

$\overline{\text{LOCK}}$ indicates the current bus cycle is locked. The Am486DXL microprocessor does not allow a bus hold when $\overline{\text{LOCK}}$ is asserted (but address holds are allowed). $\overline{\text{LOCK}}$ goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when $\overline{\text{RDY}}$ is returned. $\overline{\text{LOCK}}$ is active Low and is not driven during bus hold. Locked read cycles are not transformed into cache fill cycles if $\overline{\text{KEN}}$ is returned active.

M/$\overline{\text{IO}}$

Memory/Input_Output (Output)

This bus cycle definition pin distinguishes memory cycles from input/output cycles.

NMI

Non-maskable Interrupt (Input)

This request signal indicates that an external non-maskable interrupt has been generated. NMI is rising edge sensitive. NMI must be held Low for at least four CLK periods before this rising edge. NMI is not provided with an internal pull-down resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

PCD/PWT

Page Cache Disable/Page Write-Through (Outputs)

These reflect the state of the page attribute bits, PWT and PCD, in the page table entry or page directory entry. If paging is disabled or for unpaged cycles, PWT and PCD reflect the state of the PWT and PCD bits in Control Register 3. PWT and PCD have the same timing as the cycle definition pins (M/$\overline{\text{IO}}$, D/$\overline{\text{C}}$, and W/$\overline{\text{R}}$). PWT and PCD are active High and are not driven during bus hold. PCD is masked by the Cache Disable Bit (CD) in Control Register 0.

$\overline{\text{PCHK}}$

Parity Status (Active Low; Output)

Parity status is driven on the $\overline{\text{PCHK}}$ pin the clock after $\overline{\text{RDY}}$ for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by $\overline{\text{PCHK}}$ being Low. Parity status is only checked for enabled bytes as indicated by the byte enable and bus size signals. $\overline{\text{PCHK}}$ is valid only in the clock immediately after read data is returned to the microprocessor. At all other times $\overline{\text{PCHK}}$ is inactive High. $\overline{\text{PCHK}}$ is never floated except during three-state test mode (see $\overline{\text{FLUSH}}$).

$\overline{\text{PLOCK}}$

Pseudo-lock (Active Low; Output)

$\overline{\text{PLOCK}}$ indicates that the current bus transaction requires more than one bus cycle to complete. Examples of such operations are floating-point long reads and writes (64 bits), segment table descriptor reads (64 bits) and cache line fills (128 bits). The Am486DXL microprocessor drives $\overline{\text{PLOCK}}$ active until the addresses for the

last bus cycle of the transaction have been driven, regardless of whether $\overline{RDY}$ or $\overline{BRDY}$ has been returned.

Normally $\overline{PLOCK}$ and $\overline{BLAST}$ are inverse of each other. However, during the first bus cycle of a 64-bit floating-point write, both $\overline{PLOCK}$ and $\overline{BLAST}$ will be asserted. $\overline{PLOCK}$ is a function of the $\overline{BS8}$, $\overline{BS16}$, and $\overline{KEN}$ inputs. $\overline{PLOCK}$ should be sampled only if the clock $\overline{RDY}$ is returned. $\overline{PLOCK}$ is active Low and is not driven during bus hold.

RESET

Reset (Input)

This pin forces the Am486DXL microprocessor to begin execution at a known state. The microprocessor cannot begin execution of instructions until at least 1 ms after V_{CC} and CLK have reached their proper DC and AC specifications. The RESET pin should remain active during this time to ensure proper microprocessor operation. RESET is active High. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

$\overline{RDY}$

Non-burst Ready (Active Low; Input)

This input pin indicates that the current bus cycle is complete. $\overline{RDY}$ indicates that the external system has presented valid data on the data pins in response to a read, or that the external system has accepted data from the Am486DXL microprocessor in response to a write. $\overline{RDY}$ is ignored when the bus is idle and at the end of the bus cycle's first clock.

$\overline{RDY}$ is active during address hold. Data can be returned to the processor while AHOLD is active.

$\overline{RDY}$ is active Low and is not provided with an internal pull-up resistor. $\overline{RDY}$ must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.

$\overline{SMI}$

System Management Interrupt (Active Low; Synchronous Input/Output)

This pin is the highest level, non-maskable interrupt to the Am486DXL CPU. To initiate a System Management Interrupt, an external source must pull the input signal Low synchronously to CLK and hold it Low until the Am486DXL microprocessor suspends normal execution and enters SMM. When the CPU generates an active $\overline{SMIADS}$ pulse, it also takes control of $\overline{SMI}$ and drives $\overline{SMI}$ active Low. The CPU then continues to drive $\overline{SMI}$ Low until it exits SMM via a RESET or RES4 instruction (when the system asserts RESET, it must also release $\overline{SMI}$ to prevent buffer contention). When exiting SMM, the CPU drives $\overline{SMI}$ High for two clocks, and then releases $\overline{SMI}$ to a weak internal pull-up resistor. The $\overline{SMI}$ pull-up is active during RESET and whenever the CPU is not driving $\overline{SMI}$ active Low. The CPU disables the pull-up when it drives $\overline{SMI}$ active to minimize CPU power consumption. $\overline{SMI}$ is not three-stated during HLDA bus cycles.

Note: *$\overline{SMI}$ should not be used to qualify SMM accesses.*

$\overline{SMIADS}$

SMI Address Status (Active Low; Three-State; Output)

The Am486 CPU activates this pin to initiate a valid bus cycle to the separate SMM memory space. The function of $\overline{SMIADS}$ is analogous to $\overline{ADS}$. This signal validates the address and control lines for SMM memory, just as $\overline{ADS}$ validates address and control for non-SMM memory cycles. The system must terminate $\overline{SMIADS}$ initiated bus cycles with $\overline{SMIRDY}$. The Am486 CPU ignores both $\overline{RDY}$ and $\overline{BRDY}$ on $\overline{SMIADS}$ initiated cycles. This three-state output is floated during HLDA bus cycles.

$\overline{SMIRDY}$

SMI Ready (Active Low; Synchronous Input)

This input terminates the current bus cycle that $\overline{SMIADS}$ initiated in the same manner as $\overline{RDY}$ terminates $\overline{ADS}$ initiated bus cycles. The system must assert and deassert $\overline{SMIRDY}$ synchronously to CLK. The Am486 CPU ignores $\overline{SMIRDY}$ on $\overline{ADS}$ initiated cycles. $\overline{SMIRDY}$ has an internal pull-down resistor. This is different from the Am386® CPU $\overline{SMIRDY}$ which has an internal pull-up resistor. $\overline{SMIRDY}$ should not be physically connected to $\overline{RDY}$.

TCK

Test Clock (Input)

Test Clock is an input to the Am486 CPU and provides the clocking function required by the JTAG boundary scan feature. TCK is used to clock state information and data into and out of the component. State select information and data are clocked into the component on the rising edge of TCK on TMS and TDI, respectively. Data is clocked out of the component on the falling edge of TCK on TDO.

TDI

Test Data Input (Input)

TDI is the serial input used to shift JTAG instructions and data into the component. TDI is sampled on the rising edge of TCK during the SHIFT-IR and the SHIFT-DR TAP controller states. During all other tap controller states, TDI is a "don't care."

TDO

Test Data Output (Output)

TDO is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the fal-

ling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times, TDO is driven to the high impedance state.

TMS

Test Mode Select (Input)

TMS is decoded by the JTAG TAP (Tap Access Port) to select the operation of the test logic. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller, TMS is provided with an internal pull-up resistor.

W/$\overline{R}$

Write/Read (Output)Write/Read (Output)

This bus definition pin distinguishes write cycles from read cycles.

Table 1. Output Pins

Name	Active Level	Floated At
BREQ	High	
HLDA	High	
$\overline{BE3}$–$\overline{BE0}$	Low	Bus Hold
PCD/PWT	High	Bus Hold
W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$	High	Bus Hold
$\overline{LOCK}$	Low	Bus Hold
$\overline{PLOCK}$	Low	Bus Hold
$\overline{ADS}$	Low	Bus Hold
$\overline{BLAST}$	Low	Bus Hold
$\overline{PCHK}$	Low	
A3–A2	High	Bus, Address Hold
$\overline{SMIADS}$	Low	Hold Acknowledge

Table 2. Input Pins

Name	Active Level	Synchronous/ Asynchronous
CLK		
RESET	High	Asynchronous
HOLD	High	Synchronous
AHOLD	High	Synchronous
$\overline{EADS}$	Low	Synchronous
$\overline{BOFF}$	Low	Synchronous
$\overline{FLUSH}$	Low	Asynchronous
$\overline{A20M}$	Low	Asynchronous
$\overline{BS16}$, $\overline{BS8}$	Low	Synchronous
$\overline{KEN}$	Low	Synchronous
$\overline{RDY}$	Low	Synchronous
$\overline{BRDY}$	Low	Synchronous
INTR	High	Asynchronous
NMI	High	Asynchronous
$\overline{SMIRDY}$	Low	Synchronous

Table 3. Input/Output Pins

Name	Active Level	Floated At
D31–D0	High	Bus Hold
DP3–DP0	High	Bus Hold
A31–A4	High	Bus, Address Hold
$\overline{SMI}$	Low	Hold Acknowledge

Table 4. Bus Cycle Definition

M/$\overline{IO}$	D/$\overline{C}$	W/$\overline{R}$	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Halt/Special Cycle
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Code Read
1	0	1	Reserved
1	1	0	Memory Read
1	1	1	Memory Write

Table 5. Test Pins

Name	Input or Output	Sampled/Driven On
TCK	Input	N/A
TDI	Input	Rising Edge of TCK
TDO	Output	Falling Edge of TCK
TMS	Input	Rising Edge of TCK

CPU IDENTIFICATION CODES

The DX register always contains a component identification at the conclusion of RESET. The upper byte of DX (DH) will contain 04 and the lower byte of DX (DL) will contain a CPU type/stepping identifier.

Table 6. CPU ID

Component ID (DH)	Component ID (DL)
04	22

Table 7. JTAG ID Code

Version Code	Part Number Code	Manufacturer Identity
00h	0422	01

ELECTRICAL DATA

The following sections describe recommended electrical connections for the Am486DXL microprocessor and its electrical specifications.

Power and Grounding

Power Connections

The Am486DXL microprocessor is implemented in CS14 technology and has modest power requirements. However, its high clock frequency output buffers can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean, on-chip power distribution at high frequency, 24 V_{CC} and 28 V_{SS} pins feed the Am486DXL microprocessor.

Power and ground connections must be made to all external V_{CC} and GND pins of the Am486DXL microprocessor. On the circuit board, all V_{CC} pins must be connected on a V_{CC} plane. All V_{SS} pins must likewise be connected on a GND plane.

Power Decoupling Recommendations

Liberal decoupling capacitance should be placed near the Am486DXL microprocessor. The Am486DXL microprocessor, driving its 32-bit parallel address and data buses at high frequencies, can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high-frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the Am486DXL microprocessor, and decoupling capacitors as much as possible. Capacitors specifically for PGA packages are also commercially available.

Other Connection Recommendations

NC pins should always remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Active Low inputs should be connected to V_{CC} through a pull-up resistor. Pull-ups in the range of 20 KΩ are recommended. Active High inputs should be connected to GND.

ABSOLUTE MAXIMUM RATINGS

Case Temperature under Bias .... −65°C to +110°C
Storage Temperature ..... −65°C to +150°C
Voltage on any pin
with respect to ground ..... −0.5 V to V_{CC} +0.5 V
Supply voltage with
respect to V_{SS} ..... −0.5 V to +6.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

T_{CASE} ..... 0°C to +85°C
V_{CC} ..... 5.0 V ± 5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

T_{CASE} = 0°C to +85°C

Symbol	Parameter Description	Notes	PRELIMINARY		Unit
			Min	Max	
V_{IL}	Input Low Voltage		−0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = (Note 1) I_{OL} = 0.1 mA		0.45 0.2	V
V_{OH}	Output High Voltage	I_{OH} = (Note 2) I_{OH} = −0.1 mA	2.4 V_{CC} −0.2		V
I_{CC}	Power Supply Current	V_{CC} = 5.0 V (Note 3)		850	mA
I_{LI}	Input Leakage Current	(Note 4)		±15	µA
I_{IH}	Input Leakage Current	(Note 5)		200	µA
I_{IL}	Input Leakage Current	(Note 6)		−400	µA
I_{LO}	Output Leakage Current			±15	µA
C_{IN}	Input Capacitance	F_C = 1 MHz (Note 7)		13	pF
C_O	I/O or Output Capacitance	F_C = 1 MHz (Note 7)		17	pF
C_{CLK}	CLK Capacitance	F_C = 1 MHz (Note 7)		15	pF

Notes:

1. *This parameter is measured at:* *Address, Data, $\overline{BE3}$–$\overline{BE0}$* *4.0 mA*
   Definition, Control *5.0 mA*
2. *This parameter is measured at:* *Address, Data, $\overline{BE3}$–$\overline{BE0}$* *−1.0 mA*
   Definition, Control *−0.9 mA*
3. *Typical supply current: 700 mA @ 40 MHz*
4. *This parameter is for inputs without pull-ups or pull-downs and $0 \le V_{IN} \le V_{CC}$.*
5. *This parameter is for inputs with pull-downs and V_{IH} = 2.4 V.*
6. *This parameter is for inputs with pull-ups and V_{IL} = 0.45 V.*
7. *Not 100% tested.*

SWITCHING CHARACTERISTICS

The switching characteristics consist of output delays, input set-up requirements, and input hold requirements. All switching characteristics are relative to the rising edge of the CLK signal.

Switching characteristics measurement is defined by Figure 2 through Figure 8. Inputs must be driven to the voltage levels indicated by Figure 1 when switching characteristics are measured.

Am486DXL microprocessor output delays are specified with minimum and maximum limits, measured as shown. The minimum Am486DXL microprocessor delay times are hold times provided to external circuitry. Am486DXL microprocessor input setup and hold times are specified as minimums, defining the smallest acceptable sampling windows. Within the sampling windows, a synchronous input signal must be stable for correct Am486DXL microprocessor operation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Switching Characteristics at 40 MHz; T_{CASE} = 0°C to +85°C; C_L = 50 pF unless otherwise specified.

Symbol	Parameter Description	Notes	Figure	PRELIMINARY		Unit
				Min	Max	
	Operating Frequency			0	40	MHz
t_1	CLK Period		1	25		ns
t_{1a}	CLK Period Stability	Adjacent Clocks			0.1%	Δ
t_2	CLK High Time	@ 2.0 V	1	9		ns
t_3	CLK Low Time	@ 0.8 V	1	9		ns
t_4	CLK Fall Time		1		3	ns
t_5	CLK Rise Time		1		3	ns
t_6	A31–A2, PWT, PCD, M/$\overline{IO}$, $\overline{BE3}$–$\overline{BE0}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$, $\overline{FERR}$, BREQ, HLDA Valid Delay		6	3	16	ns
t_{6s}	$\overline{SMIADS}$ Valid Delay	C_L = 50 pF	6	3	16	ns
t_7	A31–A2, PWT, PCD, M/$\overline{IO}$, $\overline{BE3}$–$\overline{BE0}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$ Float Delay	(Note 1)	7	3	20	ns
t_{7s}	$\overline{SMIADS}$ Float Delay	(Note 1)	7	3	20	ns
t_8	$\overline{PCHK}$ Valid Delay		5	3	20	ns
t_{8a}	$\overline{BLAST}$, $\overline{PLOCK}$ Valid Delay		6	3	16	ns
t_9	$\overline{BLAST}$, $\overline{PLOCK}$ Float Delay	(Note 1)	7	3	20	ns
t_{10}	D31–D0, DP3–DP0 Write Data Valid Delay		6	3	18	ns
t_{11}	D31–D0, DP3–DP0 Write Data Float Delay	(Note 1)	7	3	20	ns
t_{12}	$\overline{EADS}$ Setup Time		3	5		ns
t_{13}	$\overline{EADS}$ Hold Time		3	3		ns
t_{14}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Setup Time		3	5		ns
t_{15}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Hold Time		3	3		ns
t_{16}	$\overline{RDY}$, $\overline{BRDY}$ Setup Time		4	5		ns
t_{16s}	$\overline{SMIRDY}$ Setup Time		4	5		ns
t_{17}	$\overline{RDY}$, $\overline{BRDY}$ Hold Time		4	3		ns
t_{17s}	$\overline{SMIRDY}$ Hold Time		4	3		ns
t_{18}	HOLD, AHOLD Setup Time		3	6		ns
t_{18a}	$\overline{BOFF}$ Setup Time		3	8		ns
t_{19}	HOLD, AHOLD, $\overline{BOFF}$ Hold Time		3	3		ns
t_{20}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR , $\overline{IGNNE}$ Setup Time		2, 3	5		ns
t_{20s}	$\overline{SMI}$ Setup Time		2, 3	5		ns
t_{21}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$ Hold Time		2, 3	3		ns
t_{21s}	$\overline{SMI}$ Hold Time		2, 3	3		ns
t_{22}	D31–D0, DP3–DP0, A31–A4 Read Setup Time		3, 4	5		ns
t_{23}	D31–D0, DP3–DP0, A31–A4 Read Hold Time		3, 4	4		ns

Note:

1. Not 100% tested. Guaranteed by design characterization.

Am486DXL Microprocessor AC Characteristics for Boundary Scan Test Signals at 25 MHz

V_{CC} = 5 V ±5%; T_{CASE} = 0°C to +85°C; C_L = 0 pF. All inputs and outputs are TTL Level.

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{24}	TCK Frequency		25	MHz		1X Clock
t_{25}	TCK Period	40		ns		Note 2
t_{26}	TCK High Time	10		ns		at 2.0 V
t_{27}	TCK Low Time	10		ns		at 0.8 V
t_{28}	TCK Rise Time		4	ns		Note 1
t_{29}	TCK Fall Time		4	ns		Note 1
t_{30}	TDI, TMS Setup Time	8		ns	8	Note 3
t_{31}	TDI, TMS Hold Time	7		ns	8	Note 3
t_{32}	TDO Valid Delay	3	25	ns	8	Note 3
t_{33}	TDO Float Delay		36	ns	8	Note 3
t_{34}	All Outputs (Non-Test) Valid Delay	3	25	ns	8	Note 3
t_{35}	All Outputs (Non-Test) Float Delay		36	ns	8	Note 3
t_{36}	All Inputs (Non-Test) Setup Time	8		ns	8	Note 3
t_{37}	All Inputs (Non-Test) Hold Time	7		ns	8	Note 3

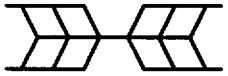
Notes:

1. Rise/Fall times are measured between 0.8 V and 2.0 V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.

2. TCK period ≥ CLK period.

3. Parameter measured from TCK.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

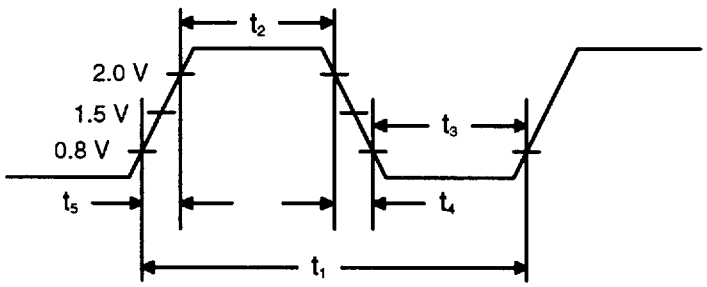


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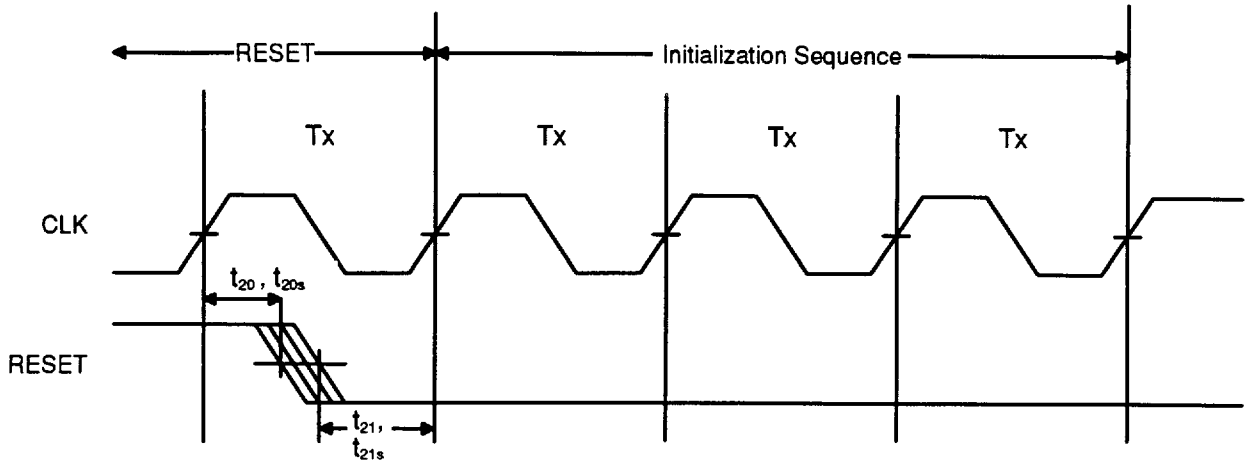
Figure 1. CLK Waveforms



17852A–098

Figure 2. RESET Setup and Hold Timing

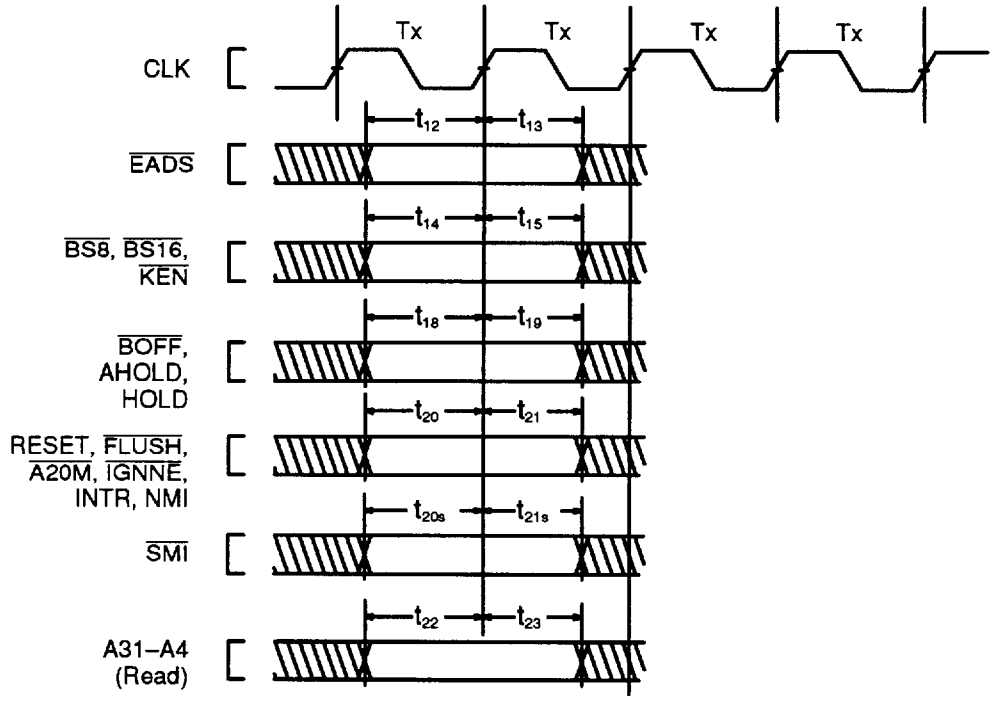


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Figure 3. Input Setup and Hold Timing

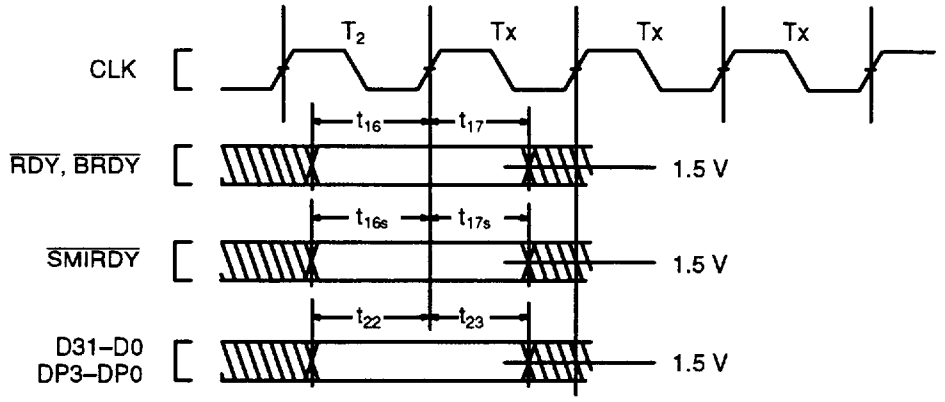

Figure 4. $\overline{\text{RDY}}$ and $\overline{\text{BRDY}}$ Input Setup and Hold Timing

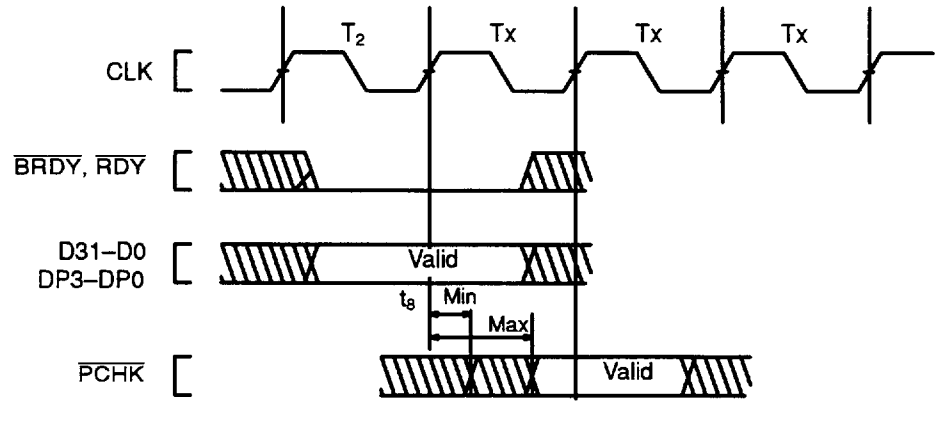

Figure 5. $\overline{\text{PCHK}}$ Valid Delay Timing

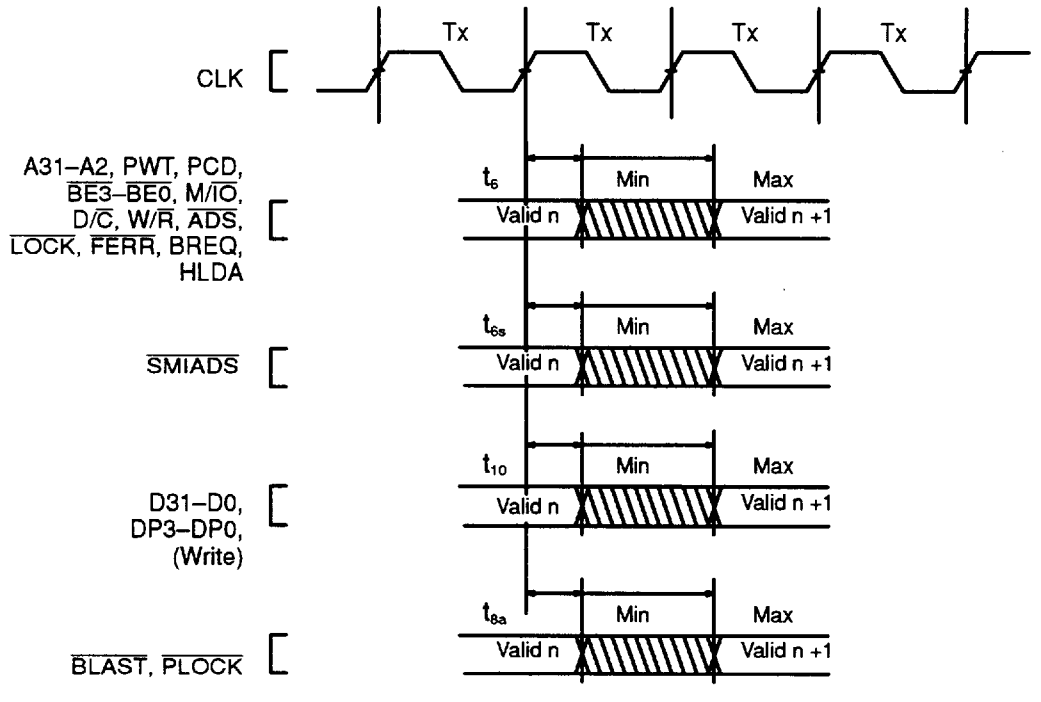

Figure 6. Output Valid Delay Timing

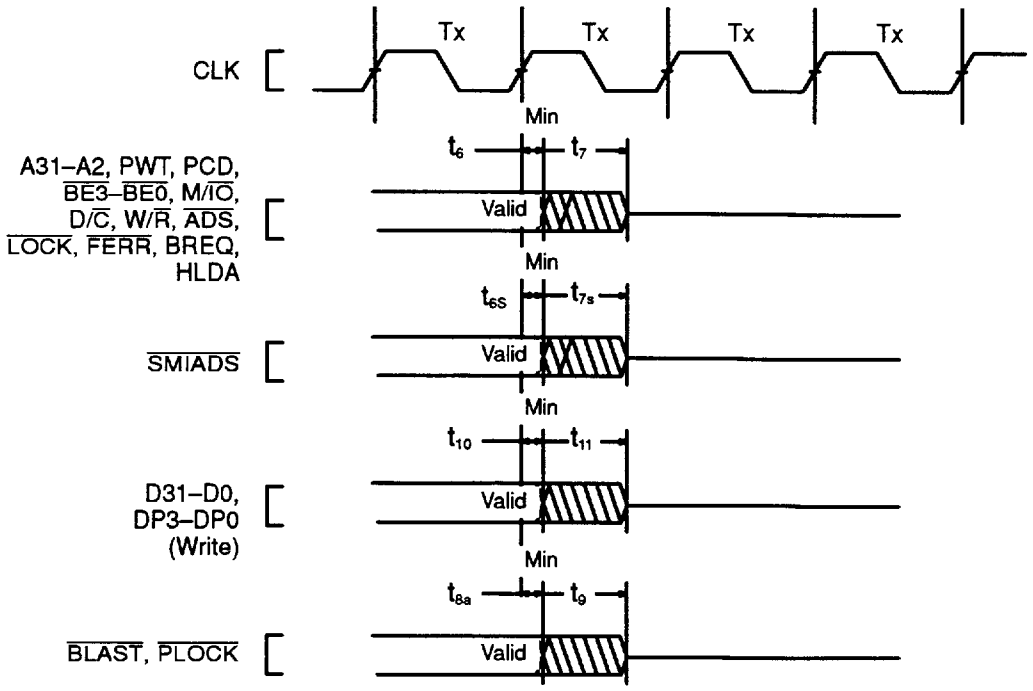

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Figure 7. Maximum Float Delay Timing

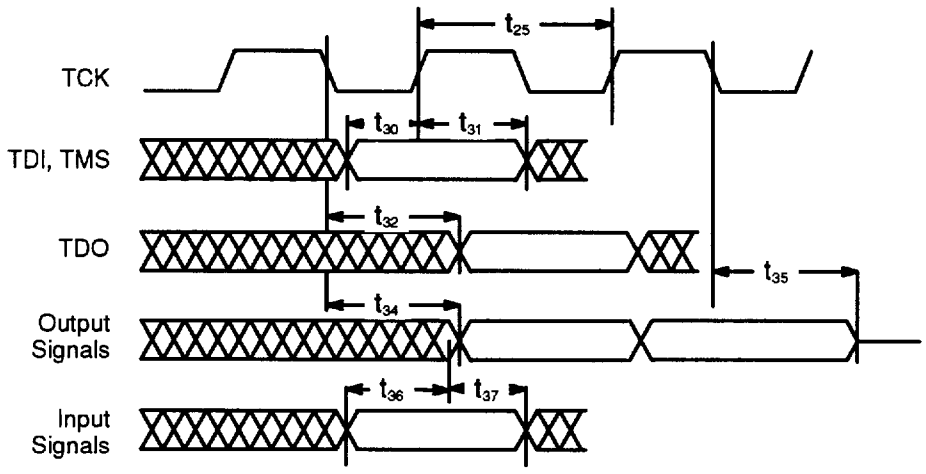

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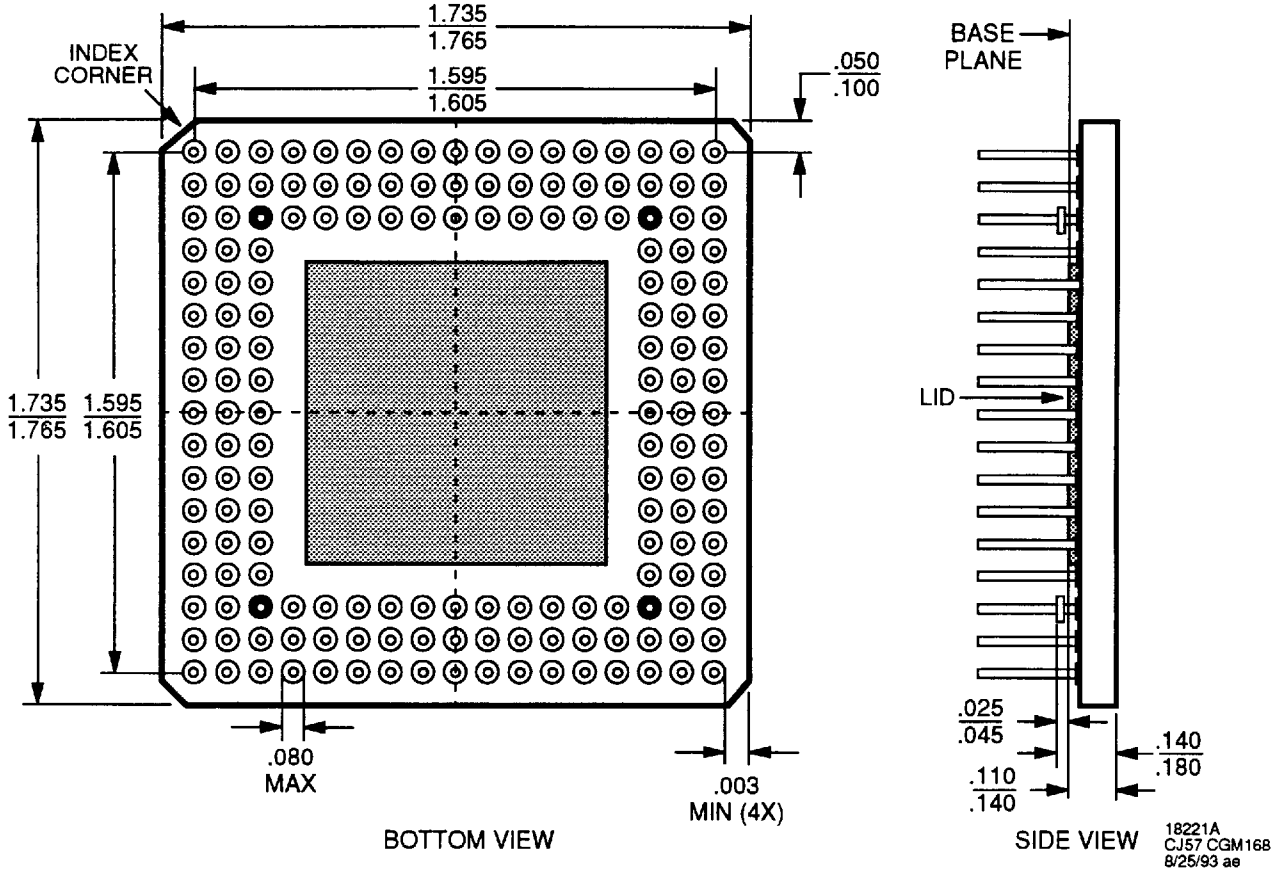
Figure 8. Test Signal Timing Diagram

PHYSICAL DIMENSIONS

CGM 168 (measured in inches)



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