PACIFIC MICROCIRCUITS LTD.

PD32HC01

DIGITAL SIGNAL PROCESSOR INTERFACE for theTMS32010 / DSP32010

Features

- Single-chip solution to TMS32010 serial interfacing
- Serial Codec port
- Serial Data communications port
- I/O and Interrupt control
- Decoding for external RAM and ROM memory
- I/O expansion interface
- 2400 Hz bit rate generator
- Low-power CMOS technology

Description

The PD32HC01 is a DIGITAL SIGNAL PROCESSOR INTERFACE circuit, intended for use in voice band signal processing circuits. It provides an optimized interface between the TMS32010 digital signal processor, and external RAM, ROM, and Codec.

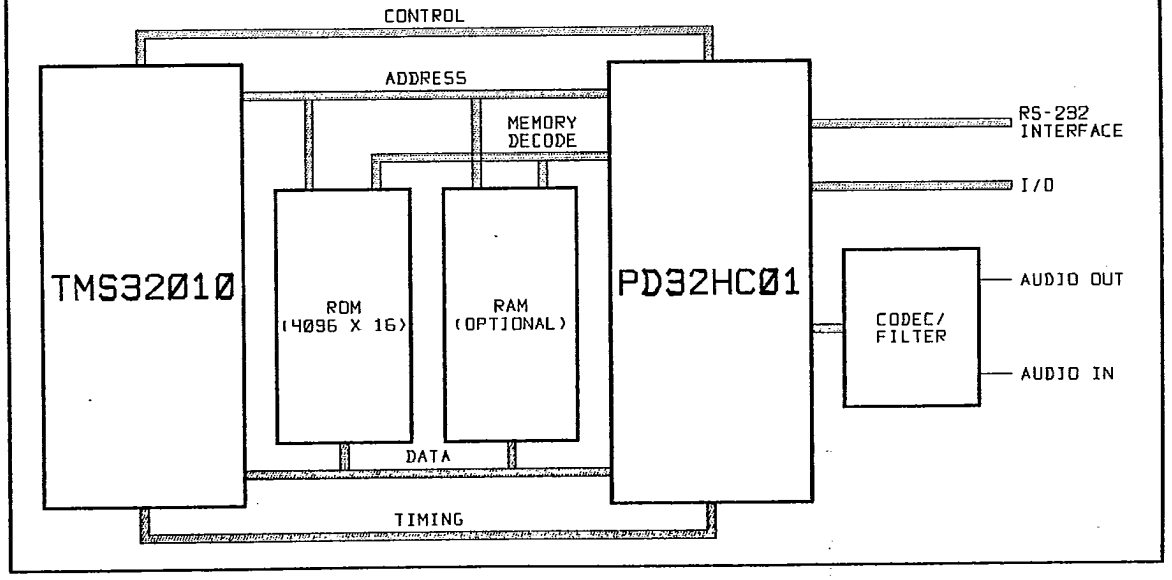
Applications

- Digital Telephony
- Data Communications
- Digital Radio
- Voice Coders/Decoders
- Speech Synthesis
- Speech Recognition

Package Availability

- 40 Lead DIL Ceramic (PD32HC01C)
- 40 Lead DIL Plastic (PD32HCO1E)
- 44 Lead Surface Mounted Plastic (PD32HC01P)

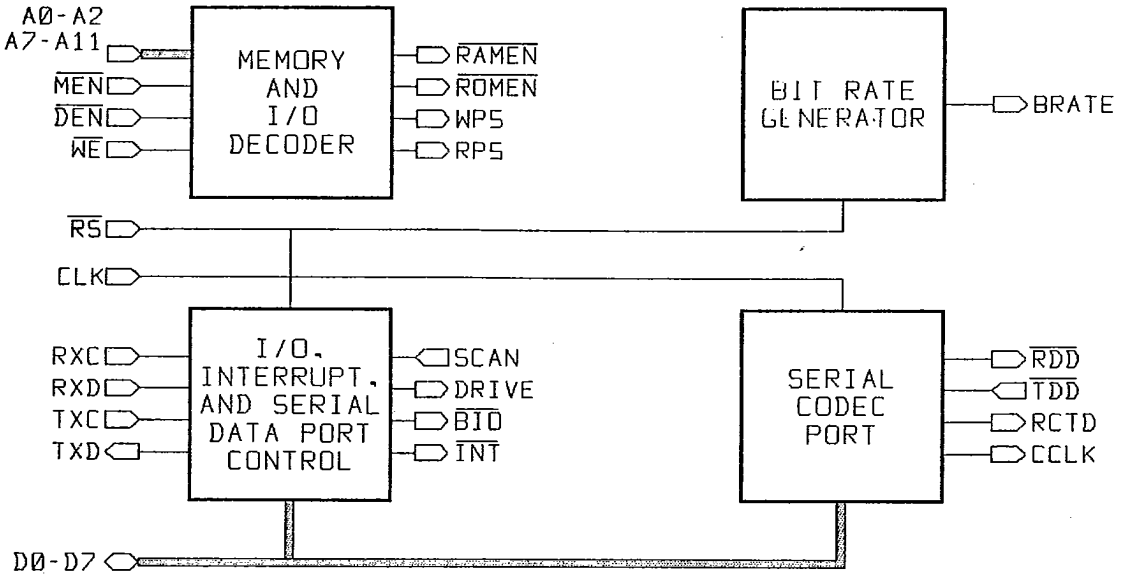
TYPICAL APPLICATION (FIG. 1)



 D/S 601-00012-AA January 1986

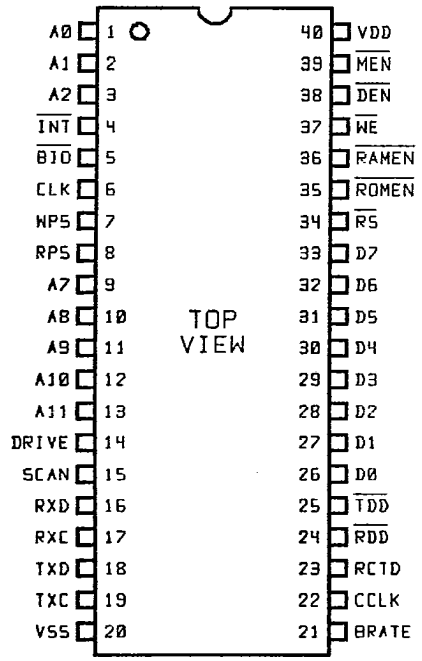
Pacific Microcircuits Ltd., 240 'H' Street, Blaine, WA 98230 1-800-663-5015
In Canada: Pacific Microcircuits Ltd., 1645 - 140th St., White Rock, BC V4A 4H1 (604) 536-1886

FUNCTIONAL BLOCK DIAGRAM (FIG. 2)



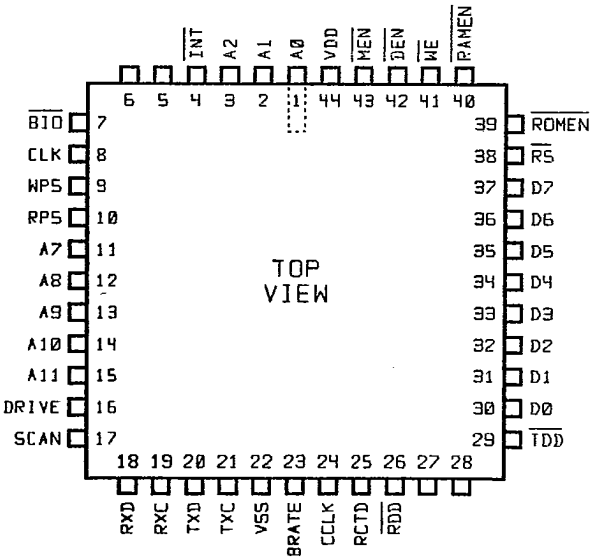
PD32HC01

PIN ASSIGNMENTS



40 PIN DUAL-IN-LINE PACKAGE

PD32HC01C (CERAMIC)
PD32HC01E (PLASTIC)



44 PIN SURFACE-MOUNT PACKAGE

PD32HC01P (PLASTIC)

PD32HC01 Pin Description

Pin	Name	I/O	Description
1-3	**A0-A2**	Inputs	**Address bus** from processor.
4	**INT-**	Output	**Interrupt request** to processor. Responds to RXC, TXC, or Codec A/D interrupts.
5	**BIO-**	Output	**Polled output port** bit to processor. Data source to be polled is specified in the Peripheral Status Register.
6	**CLK**	Input	**4.128 MHz (nominal) clock,** derived from processor clock. Drives the bit rate generator and Codec interface timing.
7,8	**WP5, RP5**	Output	**Decoded I/O port write and read pulses** for I/O expansion.
9-13	**A7-A11**	Inputs	**Address bus** from processor.
14	**DRIVE**	Output	**Output bit** controlled from the Peripheral Status Register.
15	**SCAN**	Input	**Input bit** selected from the Peripheral Status Register to appear on BIO-.
16	**RXD**	Input	**Serial data input.** Must be stable on the rising edge of RXC. Selected from the Peripheral Status Register to appear on BIO-.
17	**RXC**	Input	**Serial data receive clock.** Rising edge retimes RXD, and raises an RX clock interrupt.
18	**TXD**	Output	**Serial data output.** Programmed from the Peripheral Status Register. Edges of TXD are synchronized to the rising edge of TXC.
19	**TXC**	Input	**Serial data transmit clock.** Rising edge clocks out data onto TXD from the Peripheral Status Register, and raises a TX clock interrupt.
20	**V_{SS}**	Power	**Negative supply (ground).**
21	**BRATE**	Output	**2400 Hz square wave** (CLK / 1720-- mask programmable).
22	**CCLK**	Output	**2.064 MHz (nominal) Codec clock.**
23	**RCTD**	Output	**Codec framing pulse** for Codec synchronization. Codec A/D interrupt occurs 16 CLK cycles after RCTD goes high.
24	**RDD-**	Output	**Serial data output to Codec.** PCM data is shifted out on the rising edges of the first 8 CCLK cycles after the rising edge of RCTD.
25	**TDD-**	Input	**Serial data input from Codec.** PCM data is sampled on the first 8 CCLK falling edges after the rising edge of RCTD.
26-33	**D0-D7**	In/Out	**Data bus** to chip.
34	**RS-**	Input	**Master reset** to chip. A low on this input will reset the INT- signal, and initalize the bit rate timer. This is a Schmitt trigger input.
35	**ROMEN-**	Output	**ROM enable** output. This signal goes low during a valid read from memory locations >000 - >F7F (MEN- low).
36	**RAMEN-**	Output	**RAM enable** output. This signal goes low during a valid read or write to memory locations >F80 - >FFF (MEN- low or WE- low).
37	**WE-**	Input	**Write enable** to chip. Goes low for I/O or RAM write operations.
38	**DEN-**	Input	**Data enable** to chip. Goes low for I/O read operations.
39	**MEN-**	Input	**Memory enable** to chip. Goes low for ROM or RAM reads.
40	**V_{DD}**	Power	**Positive supply (+5 Volts).**

Detailed Description

The PD32HC01 consists of 4 functional blocks: a memory and I/O decoder; I/O, interrupt, and serial data port control; a serial Codec port; and a bit rate generator (see figures. 2 & 3).

Memory and I/O Decoder

The memory and I/O decoder segments the 4K word address space of the TMS32010 into 3 areas: a 3968 word ROM area inclusive of addresses >000 to >F7F; a 128 word RAM area inclusive of addresses >F80 to >FFF; and from addresses >XX0 to >XX7, an I/O expansion port, an I/O, interrupt, and serial data port control; and a serial Codec port.

Memory Decoding

The **ROMEN-** signal is used for selecting external program ROM. It goes low during memory read or table read cycles (**MEN-** low), and the processor address is less than >F80.

The **RAMEN-** signal is used for selecting external data RAM. It goes low during memory read, table read, or table write cycles (**MEN-** or **WE-** low), and the processor address is above >F7F.

I/O Expansion Port

The **RP5** and **WP5** signals are used for I/O port expansion. **RP5** goes high during an I/O read cycle from port 5 (**DEN-** low). **WP5** goes high during an I/O write cycle to port 5, or a table write cycle to address >XX5 (**WE-** low).

I/O, Interrupt, and Serial Data Port

The Program Status Register (PSR) at port location 6 controls the **DRIVE** and **TXD** output signals; the **INT-** output operation via the Codec A/D, TX clock, and RX clock interrupt mask bits; and selects inputs to be tested on **BIO-** (interrupt flags; the **SCAN** input; or the retimed **RXD** input). The bit encoding of the PSR is shown below:

bit 0: **RXMSK**, RX clock interrupt mask.
bit 1: **TXMSK**, TX clock interrupt mask.
bit 2: **ADMSK**, Codec interrupt mask.

Writing 1's to these bits will mask interrupts from the respective sources, and/or clear posted interrupts. Writing 0's will enable interrupts. By testing for the interrupting source on the **BIO-** line, interrupt vectoring can be managed (see bits 3,4,5 description).

bits 3,4,5: BIO Source Select. These three bits select one of five input sources (interrupt flags or pin inputs) onto the **BIO-** output.

bit 5	bit 4	bit 3	Selected Source
0	0	0	Codec A/D Int. status
0	0	1	TX Clock Int. status
0	1	0	RX Clock Int. status
0	1	1	**SCAN** bit input
1	X	X	Retimed **RXD** input

Whenever a posted interrupt is selected, **BIO-** will go low. **BIO-** will stay high if the selected interrupt is not posted. When the **SCAN-** input or the retimed **RXD** input is selected, **BIO-** follows the polarity of the respective signal.

bit 6: **TXD**, the serial data port transmit data bit. This signal is retimed by the rising edge of the **TXC** clock, and appears on the **TXD** output pin.

bit 7: **DRIVE**, a general purpose output pin.

Serial Codec Port

The Serial Codec Port consists of 8-bit Transmit and Receive data registers, designed to directly interface to Motorola 14400 series PCM Monochips, and the Intel 2914.

The Transmit Register forms incoming serial data on **TDD-** into 8-bit parallel PCM samples, while the Receive Register forms 8-bit parallel PCM data samples into serial data on **RDD-** . The operation of these registers is controlled by the Codec Timing Generator, which also generates the **CCLK**, the **RCTD**, and the internal A/D interrupt signals.

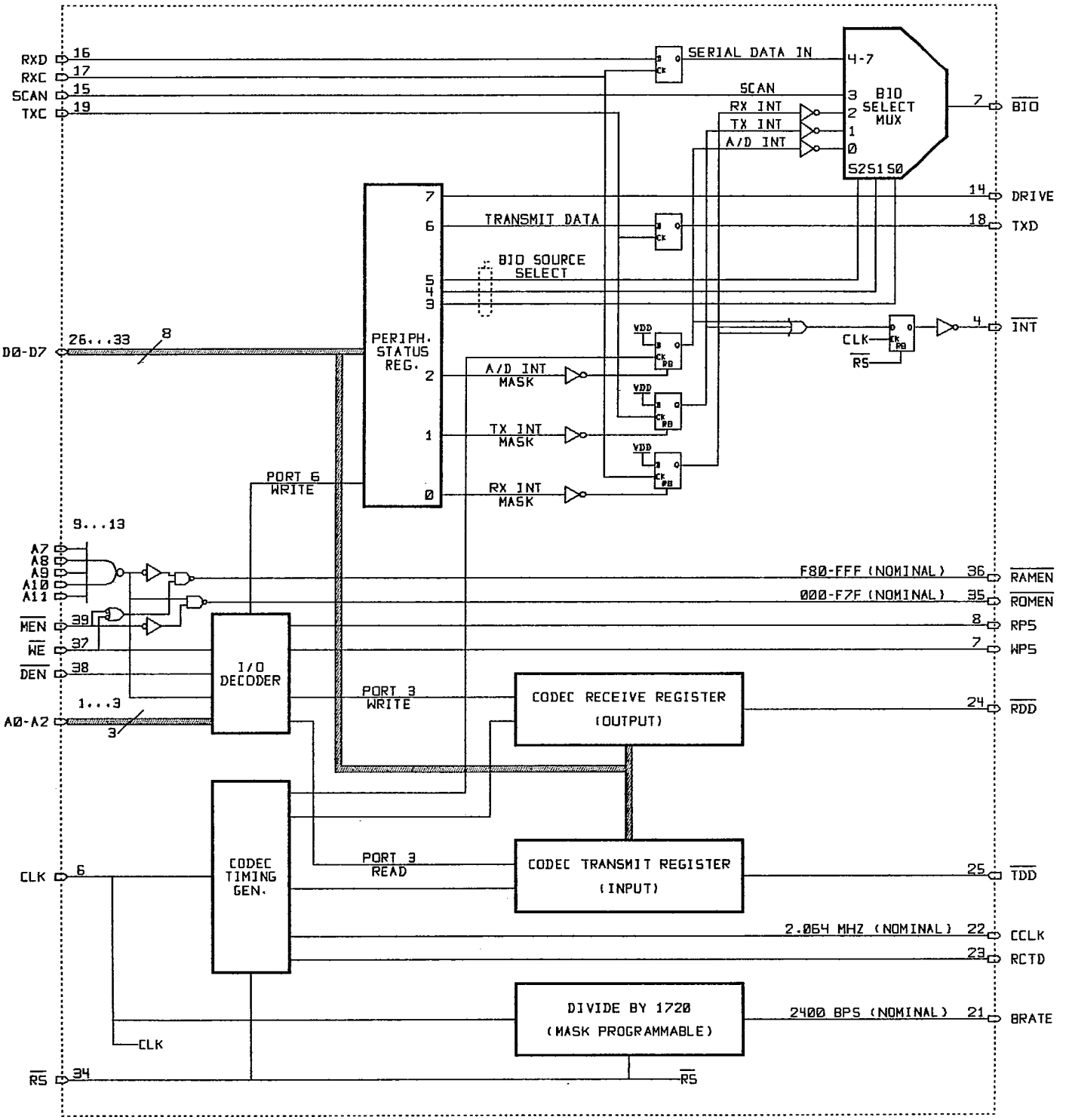
Data written to the Receive Register at I/O port location 3 is inverted, and sent MSB first on the **RDD-** Pin. Data is shifted out on the 8 rising edges of **CCLK** following the rising edge of **RCTD**. To prevent Receive Register underflow, data must be available in the Receive Register within 248 **CCLK** cycles after an A/D interrupt (nominally 120 usec).

Serial PCM data on the **TDD-** pin is inverted, and read into the Transmit Register, MSB first, at I/O port location 3. Data is shifted in on the 8 falling edges of **CCLK** following the rising edge of **RCTD**. To prevent Transmit Register overflow, data must be read within 248 **CCLK** cycles after an A/D interrupt (nominally 120 usec).

Bit Rate Generator

The **BRATE** output signal is nominally a 2400 Hz square wave, derived from the **CLK** input divided by 1720 (mask programmable). This signal may be used for bit rate generation, TXC or RXC clocking, or real-time interrupts. **BRATE** is reset whenever the **RS-** signal is low.

PD32HC01 DETAILED BLOCK DIAGRAM (FIG. 3)



NOTE: ALL PIN NUMBERS ARE FOR 40 PIN DIL PACKAGE

5

Address and Input/Output Map[1]

Address/ Ports	R/W[2]	Function
>XX3 Port 3	Read[3]	**Codec Transmit Register.** Valid for 248 CCLK cycles (nominally 120 usec) after an A/D interrupt. This 8-bit register contains the inverted version of the digitized serial PCM signal appearing on **TDD-**. This register can only be read by using a IN from port 3 instruction.
>XX3 Port 3	Write	**Codec Receive Register.** Must be valid within 248 CCLK cycles (nominally 120 usec) after an A/D interrupt. Data written to this 8-bit register will be inverted and shifted out on the **RDD-** pin. This register can be written using a OUT to port 3 instruction, or by using a TBLW to address >XX3 (address must be less than >F80).
>XX5 Port 5	Read[3]	**Input Port Expansion.** The **RP5** signal will pulse high whenever an IN from port 5 instruction is executed.
>XX5 Port 5	Write	**Output Port Expansion.** The **WP5** signal will pulse high whenever an OUT to port 5, or TBLW to >XX5 instruction is executed (address must be less than >F80).
>XX6 Port 6	Write	**Peripheral Status Register.** This register is used to: Select I/O and interrupt status bits onto the **BIO-** pin; mask and reset interrupts; control the DRIVE pin; and to send data on **TXD.** This register can be written using an OUT to port 6 instruction, or by using a TBLW to address >XX6 (address must be less than >F80).
>000- >77F	Read	Program ROM space. Notice that the I/O space and the ROM space are mapped to overlapping addresses, but are distinguished by the **MEN-** and **DEN-** signals. **MEN-** will go low for valid instruction reads, while **DEN-** will go low for I/O reads.
>780- >7FF	R/W	Data/Program RAM space. For read cycles, **MEN-** goes low; for write cycles **WE-** goes low.

Notes:
1. When using TBLW to perform Output, many aliases of the I/O port locations exist due to incomplete address decoding. To maintain compatibility with future products, it is recommended that addresses >000 to >007 be used. When using OUT instructions, the TMS32010 always addresses >000 to >007, and the aliases are irrelevant.
2. Some I/O addresses are not used. To prevent data corruption, port locations 0, 1, 2, and 4 should not be written with TBLW or OUT.
3. The I/O read locations can only be accessed with a TMS32010 IN instruction. The actual address locations are shown, however, for applications using other than the TMS32010 processor.

Recommended operating conditions @ V_{SS} = 0 Volts

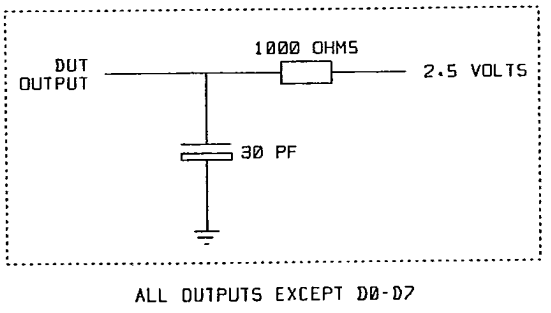
Parameter	Symbol	Min	Typ	Max	Units	Notes
Supply voltage	V_{DD}	4.75	5.0	5.25	V	
Input high voltage	V_{IH}	2		V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3		0.8	V	
Output high current	I_{OH}			3	mA	
Output low current	I_{OL}			3	mA	
Operating Temperature	T_A	0		70	°C	

Electrical characteristics over recommended operating conditions[1]

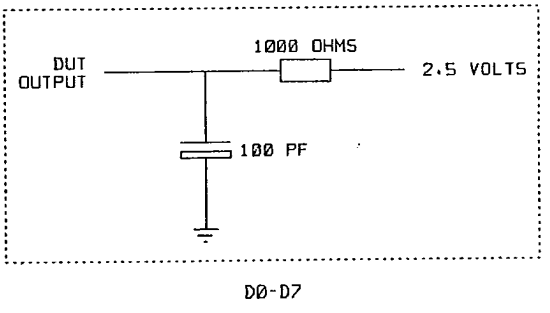
Parameter	Symbol	Min	Typ[2]	Max	Units	Test Condition
High level output voltage	V_{OH}	3.5	4.5		V	I_{OH} = 1 ma
Low level output voltage	V_{OL}		0.3	0.5	V	I_{OL} = 2 ma
RS- hysteresis voltage	V_{HYS}		200		mV	
Off-state leakage current	I_{OZ}		0.5	5	uA	
Input current	I_{IN}		0.5	5	uA	$V_{SS}<V_{IN}<V_{DD}$
Supply current [3]	I_{DD}		2		mA	
Input capacitance	C_I		10		pF	@ 1 MHz;
Output capacitance	C_O		10		pF	all other pins 0 V
CLK input frequency	F_{CLK}	0	4.128	6.25	MHz	

Note:
1. See Fig. 4 or DUT test loads.
2. Typical specifications are valid at T_A = 25 °C, V_{DD} = 5.0 Volts.
3. I_{DD} Is a function of V_{DD}, clock frequency, and output loading.

TEST LOADS (FIG. 4)



ALL OUTPUTS EXCEPT D0-D7



D0-D7

7

Timing Specifications over recommended operating conditions[1]

	Name	Description	Min	Typ[2]	Max	Units
R	(1) t_{ROMHL1}	ROMEN- select time from addr.		28		nsec
O	(2) t_{ROMLH1}	ROMEN- deselect time from addr.		30		nsec
M	(3) t_{ROMHL2}	ROMEN- select time from MEN-		25		nsec
	(4) t_{ROMLH2}	ROMEN- deselect time from MEN-		18		nsec
	(5) t_{RAMHL1}	RAMEN- select time from addr.		27		nsec
	(6) t_{RAMLH1}	RAMEN- deselect time from addr.		15		nsec
R	(7) t_{RAMHL2}	RAMEN- select time from MEN-		24		nsec
A	(8) t_{RAMLH2}	RAMEN- deselect time from MEN-		14		nsec
M	(9) t_{RAMHL3}	RAMEN- select time from addr.		27		nsec
	(10) t_{RAMLH3}	RAMEN- deselect time from addr.		15		nsec
	(11) t_{RAMHL4}	RAMEN- select time from WE-		21		nsec
	(12) t_{RAMLH4}	RAMEN- deselect time from WE-		15		nsec
	(13) t_{DR1}	Data read access time from addr.		33		nsec
R	(14) t_{DRHLD1}	Data read hold time from addr.		60		nsec
E	(15) t_{DR2}	Data read access time from DEN-		29		nsec
G	(16) t_{DRHLD2}	Data read hold time from DEN-		56		nsec
I	(17) t_{RPLH1}	RP5 select time from address		30		nsec
S	(18) t_{RPHL1}	RP5 deselect time from address		32		nsec
T	(19) t_{RPLH2}	RP5 select time from DEN-		26		nsec
E	(20) t_{RPHL2}	RP5 deselect time from DEN-		26		nsec
R	(21) t_{ASUW}	Address set-up time to WE-		4		nsec
	(22) t_{AHLDW}	Address hold time from WE-		-5		nsec
&	(23) t_{DWSU}	Data write set-up time to WE-		-25		nsec
	(24) t_{DWHLD}	Data write hold time from WE-		0		nsec
I	(25) t_{WPLH1}	WP5 select time from address		31		nsec
/	(26) t_{WPHL1}	WP5 deselect time from address		32		nsec
O	(27) t_{WPLH2}	WP5 select time from WE-		27		nsec
	(28) t_{WPHL2}	WP5 deselect time from WE-		27		nsec
S	(29) t_{RXDSU}	RXD set-up time to RXC	20	3		nsec
I	(30) t_{RXDHLD}	RXD hold time from RXC	20	2		nsec
O	(31) t_{TXD}	TXD delay time from TXC		28		nsec
C	(32) t_{RCTD}	RCTD Delay time from CCLK	15	34	100	nsec
O	(33) t_{TDDSU}	TDD- set-up time to CCLK	50	16		nsec
D	(34) t_{TDDHLD}	TDD- hold time from CCLK	20	-14		nsec
E	(35) t_{RDD}	RDD- delay time from CCLK		19	50	nsec
C	(36) t_{ADINT}	INT- delay time from RCTD			Note 3	

Note:
1. See Fig. 4 for DUT test loads.
2. Typical specifications are valid at T_A = 25 °C, V_{DD} = 5.0 Volts
3. t_{ADINT}(max) is 17 x t_{CLK} - 45 nsec (nominally 4.1 usec).

9