1.1 Scope.

This specification covers the detail requirements for a hybrid, complete, 16-channel data acquisition system. The device consists of two 8-channel input multiplexers, a programmable gain amplifier, a 12-bit sampling analog-to-digital converter, two 32-word FIFOs, a controller, and registers for status and control.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD1341TZ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: Z–100.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage ..... ±18 V
Logic Supply Voltage (V_{DD} to Digital Ground) ..... +7 V
Analog Power/Analog Signal Ground to Digital Ground ..... −0.3 V to +0.3 V
Analog Inputs to Analog Power/Analog Signal Ground
  Multiplexer ..... $+V_S$ +16 V, $-V_S$ −16 V
  PGA ..... $-V_S$ to $+V_S$
  Reference Input ..... 0 V to +11 V
Digital Inputs to Digital Ground ..... −0.3 V to V_{DD} +0.3 V or 10 mA
Output Short Circuit Duration
  Reference and Multiplexer Outputs ..... Indefinite
  Digital Outputs ..... 1 Output for 1 Second
Power Dissipation ..... 1.6 W
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Electrostatic Discharge Sensitivity ..... Class 1

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = TBD
θ_{JA} = TBD

AD1341—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit @+25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1, 2]	Units
Analog Input								
Input Impedance	R_{IN}	−1	100					MΩ typ
Voltage Range								
Common Mode	V_{INCM}	−1	±10					V min
Differential	V_{IND}	−1	10 ÷ Gain					V typ
Common-Mode Rejection Ratio	CMRR	−1	80				G = 1 or 128	dB min
Input Bias Current	I_B	−1	±2		±300		V_{CM} = 0	nA max
Voltage Noise							Referred to Input	
Gain = 1	E_{N1}	−1	75					μV rms typ
Gain = 128	E_{N2}	−1	10					μV rms typ
Reference								
Reference Voltage	V_{REF}	−1	9.90					V min
			10.10					V max
Reference Drift	V_{REFD}	−1	±30					ppm/°C max
Reference Current	I_{REF}	−1	±1					mA min
Transfer Characteristics								
Standard Throughput Rate							Note 2	
Gain = 1, 2, 4 or 8	TR_{S1}	−1	150,000					Channels/
Gain = 16	TR_{S2}	−1	75,000					Second min
Gain = 32	TR_{S3}	−1	37,500					
Gain = 64	TR_{S4}	−1	18,750					
Gain = 128	TR_{S5}	−1	9,375					
Accelerated Throughput Rate							Notes 2, 3	
Gain = 1, 2, 4 or 8	TR_{A1}	−1	150,000					Channels/
Gain = 16	TR_{A2}	−1	100,000					Second min
Gain = 32	TR_{A3}	−1	57,690					
Gain = 64	TR_{A4}	−1	29,410					
Gain = 128	TR_{A5}	−1	14,850					
Static Characteristics Programmable Gain								
Accuracy	P_{GAE}	−1	±2				Any Gain	% max
Integral Nonlinearity	INL	−1	±1		±1			LSB max
Resolution for No Missing Codes	RS_{NMC}	−1	12		12			Bits min
Unipolar Offset Error	V_{OS}	−1	±2		±6			LSB max
Bipolar Zero Error	B_{PZE}	−1	±2		±6			LSB max
Gain Error	A_E	−1	±2		±12			LSB max
Dyanmic Characteristics								
Signal-to-Noise Ratio							Note 4	
Gain = 1	SNR_1	−1	70	70		70	f_S = 150.0 kHz	dB min
Gain = 2	SNR_2	−1	72				f_S = 150.0 kHz	dB typ
Gain = 4	SNR_3	−1	72				f_S = 150.0 kHz	dB typ
Gain = 8	SNR_4	−1	71				f_S = 150.0 kHz	dB typ
Gain = 16	SNR_5	−1	68	68		68	f_S = 75.0 kHz	dB min
Gain = 32	SNR_6	−1	70				f_S = 37.5 kHz	dB typ
Gain = 64	SNR_7	−1	69				f_S = 18.8 kHz	dB typ
Gain = 128	SNR_8	−1	66				f_S = 9.4 kHz	dB typ
Total Harmonic Distortion							Note 4	
Gain = 1	THD_1	−1	−80	−80		−80	f_S = 150.0 kHz	dB max
Gain = 2	THD_2	−1	−90				f_S = 150.0 kHz	dB typ
Gain = 4	THD_3	−1	−88				f_S = 150.0 kHz	dB typ
Gain = 8	THD_4	−1	−88				f_S = 150.0 kHz	dB typ
Gain = 16	THD_5	−1	−78	−78		−78	f_S = 75.0 kHz	dB max
Gain = 32	THD_6	−1	−88				f_S = 37.5 kHz	dB typ
Gain = 64	THD_7	−1	−85				f_S = 18.8 kHz	dB typ
Gain = 128	THD_8	−1	−84				f_S = 9.4 kHz	dB typ
Channel-to-Channel Isolation	ISO_{CH}	−1	80					dB typ

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Test	Symbol	Device	Design Limit @+25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1, 2]	Units
Digital Inputs							Note 5	
Input Voltage Low	V_{IL}	−1	0.8	0.8				V max
Input Voltage High	V_{IH}	−1	2.25	2.25				V min
Input Current	I_I	−1	200	200				μA max
Input Capacitance	C_I	−1	2	2				pF typ
$\overline{\text{Reset}}$ Low Pulse Width	t_{RPW}	−1	10	10				ns min
Clock Input								
Frequency	F_{CLK}	−1	3.0	3.0				MHz max
Duty Cycle	DCL	−1	45	45				% min
			55	55				% max
Digital Outputs							Note 5	
Output Voltage Low	V_{OL}	−1	0.4	0.4			I_{OL} = 3.2 mA	V max
Output Voltage High	V_{OH}	−1	2.4	2.4			I_{OH} = −3.2 mA	V min
Output Capacitance	C_O	−1	6	6				pF typ
High Impedance Leakage, D0–D15	I_{OZ}	−1	±200	±200				μA max
Off State Leakage	I_{OZ}	−1	±10	±10				μA max
Power Supply								
+Analog Supply	$+V_S$	−1	+13.5					V min
			+16.5					V max
−Analog Supply	$-V_S$	−1	−16.5					V max
			−13.5					V min
+Analog Supply Current	$+I_S$	−1	56				Quiescent	mA max
−Analog Supply Current	$-I_S$	−1	50				Quiescent	mA max
Logic Supply Current	I_{DD}	−1	10				Quiescent	mA max
Power Consumption	P_D	−1	1.6					W max
Power Supply Rejection Ratio	PSRR	−1	±1/2				$\pm V_S$	LSB/V
Read Cycle								
Read Cycle Time	t_{RC}	−1	25				C_{OUT} = 30 pF	ns min
			35				C_{OUT} = 100 pF	ns min
Data Access Time	t_A	−1	15				C_{OUT} = 30 pF	ns max
			25				C_{OUT} = 100 pF	ns max
			35				C_{OUT} = 150 pF	ns max
Output LO-Z Time	t_{LZ}	−1	2					ns min
Output HI-Z Time	t_{HZ}	−1	15				C_{OUT} = 30 pF	ns max
			25				C_{OUT} = 100 pF	ns max
Output Hold Time	t_{OH}	−1	2					ns min
A0 Valid to $\overline{\text{RD}}$ Low	t_{ARD}	−1	3					ns min
$\overline{\text{RD}}$ High to A0 Invalid	t_{RDA}	−1	3					ns min
A0 Valid to $\overline{\text{CS}}$ Low	t_{ACS}	−1	3					ns min
$\overline{\text{CS}}$ High to A0 Invalid	t_{CSA}	−1	3					ns min
Write Cycle								
Write Cycle Time	t_{WC}	−1	15					ns min
Write Pulse Width	t_{WP}	−1	5					ns min
Input Setup Time	t_{SU}	−1	2					ns min
Input Hold Time	t_{IH}	−1	3					ns min
A0 Valid to $\overline{\text{WR}}$ Low	t_{AWR}	−1	3					ns min
$\overline{\text{WR}}$ High to A0 Invalid	t_{WRA}	−1	3					ns min
A0 Valid to $\overline{\text{CS}}$ Low	t_{ACS}	−1	3					ns min
$\overline{\text{CS}}$ High to A0 Invalid	t_{CSA}	−1	3					ns min

NOTES

[1]T_A = +25°C, V_S = ±15 V dc, 16-channel, single-ended bipolar mode, $\overline{\text{ASYNCEN}}$ = Low, F_{CLK} = 3.0 MHz, and G = 1, unless otherwise noted.

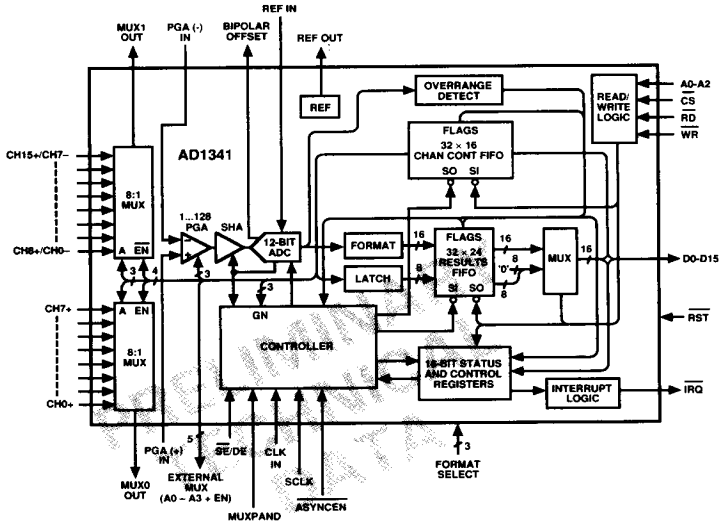
[2]All channel gains are fixed at the specified value.

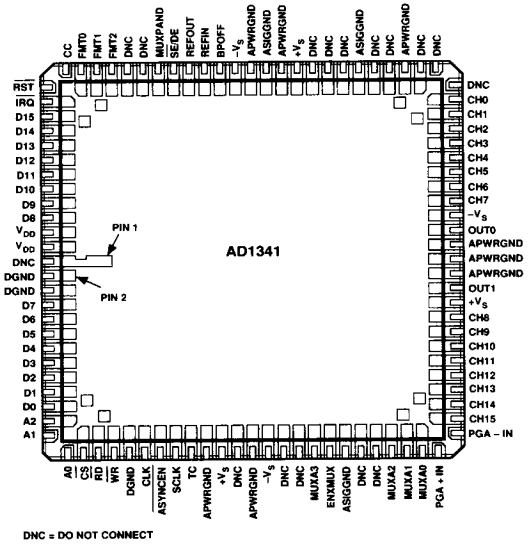
[3]Accelerated performance is achieved through using a pipeline architecture and constant SHA acquisition times.

[4]f_{IN} = 4.6 kHz for G = 1, 2, 3 kHz for G = 16 tests. SNR excludes harmonics 2–9. THD includes harmonics 2–9. Input amplitude is −0.3 dB relative to full scale at each gain.

[5]Guaranteed over operating temperature range, tested at +25°C only.

3.2.1 Functional Block Diagram and Terminal Assignments.





DNC = DO NOT CONNECT

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 method 1015 test condition (B).