

Features

- ☐ High speed access times
Com'l: 8, 10, 12, 15, 20 and 25 ns
Ind'l: 10, 12, 15, 20, and 25 ns
- ☐ Low power operation
 - PDM41298SA
Active: 400 mW (typ.)
Standby: 150 mW (typ.)
 - PDM41298LA
Active: 350 mW (typ.)
Standby: 25 mW (typ.)
- ☐ Output Enable pin available for greater system flexibility
- ☐ Single +5V ($\pm 10\%$) power supply
- ☐ TTL compatible inputs and outputs
- ☐ Packages
 - Plastic DIP (300 mil) - P
 - Cerdip (300 mil) - D
 - Plastic SOJ (300 mil) - SO
 - Plastic TSOP - T

Description

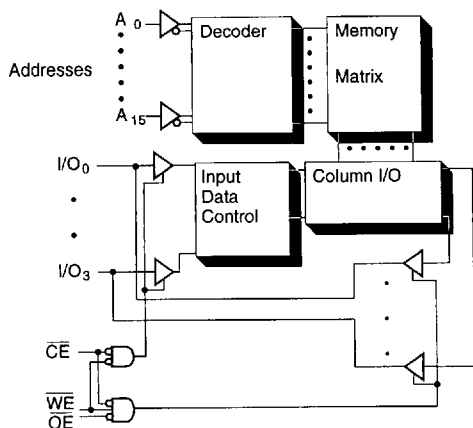
The PDM41298 is a high-performance CMOS static RAM organized as 65,536 x4 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing to this devices is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ are both LOW.

The PDM41298 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM41298 comes in two versions, the standard power version PDM41298SA and a low power version the PDM41298LA. The two versions are functionally the same and only differ in their power consumption.

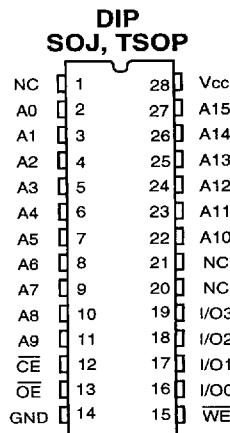
The PDM41298 is available in a 28-pin 300 mil DIP, a 28-pin 300 mil Cerdip, a 28-pin plastic TSOP, and a 28-pin 300 mil SOJ for surface mount applications.

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Functional Block Diagram



Pin Configuration



Truth Table

OE	WE	CE	I/O	MODE
X	X	H	Hi-Z	Standby
L	H	L	D _{OUT}	Read
X	L	L	D _{IN}	Write
H	H	L	Hi-Z	Output Disable

NOTE: 1. H = V_{IH} , L = V_{IL} , X = DON'T CARE

Absolute Maximum Ratings ⁽¹⁾

Symbol	Rating	Com'l.	Ind.	Unit
V _{TERM}	Terminal Voltage with Respect GND	-0.5 to +7.0	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	0	25	70	°C
Industrial	Ambient Temperature	-40	25	85	°C

DC Electrical Characteristics ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions		PDM41298SA		PDM41298LA		Unit
				Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	$V_{CC} = \text{MAX.}, V_{IN} = \text{GND to } V_{CC}$	Com'l/ Ind.	-5	5	-2	5	μA
I_{LO}	Output Leakage Current	$V_{CC} = \text{MAX.},$ $\overline{CE} = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	Com'l/ Ind.	-5	5	-2	5	μA
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage			-0.5 ⁽¹⁾	0.8	-0.5 ⁽¹⁾	0.8	V
V_{OL}	Output Low Voltage	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min.}$ $I_{OL} = 10 \text{ mA}, V_{CC} = \text{Min.}$		—	0.4 0.5	—	0.4 0.5	V V
V_{OH}	Output High Voltage	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min.}$		2.4	—	2.4	—	V

NOTE: 1. $V_{IL}(\text{min}) = -3.0\text{V}$ for pulse width less than 20 ns.

Power Supply Characteristics

Symbol	Parameter	Power	-8	-10		-12		-15		-20		-25	
			Com'l.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.
I_{CC}	Operating Current $\overline{CE} = V_{IL}$	SA	200	190	200	180	190	170	180	160	170	150	160
	$f = f_{\text{MAX}} = 1/t_{RC}$ $V_{CC} = \text{Max}$ $I_{OUT} = 0 \text{ mA}$	LA	180	170	180	160	170	150	160	140	150	130	140
I_{SB}	Standby Current $\overline{CE} = V_{IH}$	SA	80	70	70	60	60	50	50	40	40	35	35
	$f = f_{\text{MAX}} = 1/t_{RC}$ $V_{CC} = \text{Max}$	LA	80	70	70	60	60	50	50	40	40	35	35
I_{SB1}	Full Standby Current $\overline{CE} \geq V_{CC} - 0.2\text{V}$	SA	20	20	20	20	20	10	20	10	20	10	20
	$f = 0$ $V_{CC} = \text{Max}$ $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $\leq 0.2\text{V}$	LA	5	5	10	5	10	5	10	5	10	5	10

SHADED AREA = PRELIMINARY DATA.

NOTE: All values are maximum guaranteed values.

Capacitance⁽¹⁾ ($T_A = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE: 1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

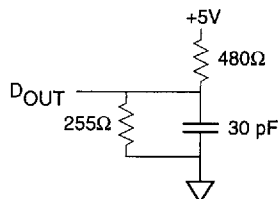


Figure 1. Output Load Equivalent

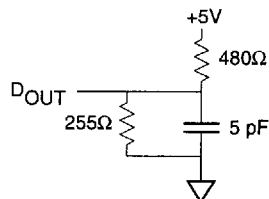
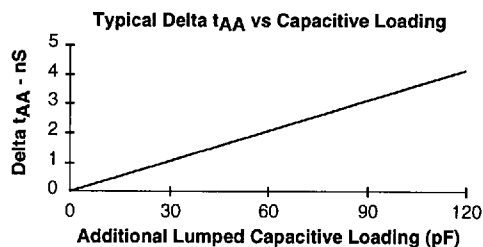
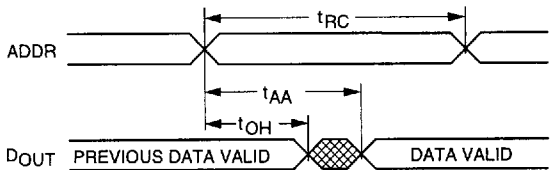


Figure 2. Output Load Equivalent
(for t_{LZCE} , t_{HZCE} , t_{LZWE} , t_{HZWE} , t_{LZOE} , t_{HZOE})

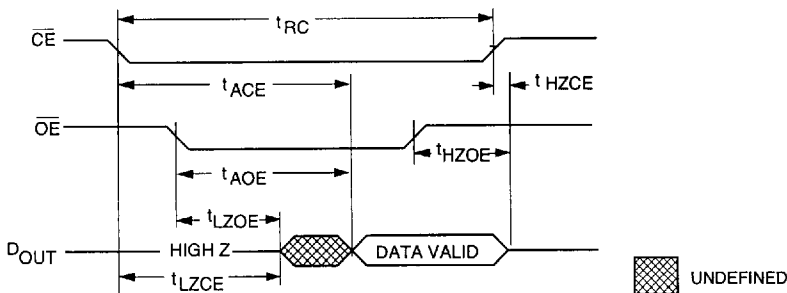


Read Cycle No. 1⁽¹⁾



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Read Cycle No. 2⁽²⁾



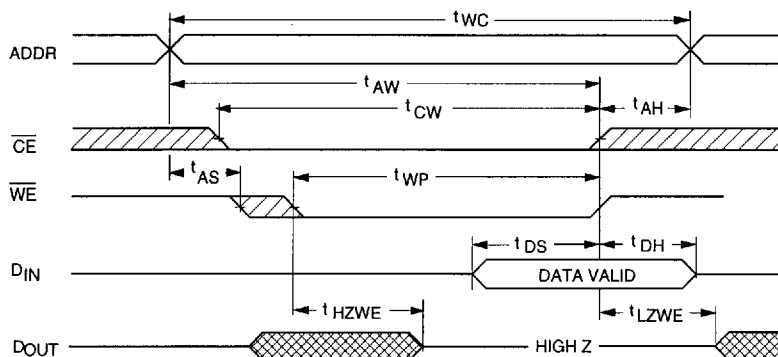
AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

Description		-8 ⁽⁶⁾		-10 ⁽⁶⁾		-12		-15		-20		-25		
READ Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
READ cycle time	t _{RC}	8		10		12		15		20		25		ns
Address access time	t _{AA}		8		10		12		15		20		25	ns
Chip enable access time	t _{ACE}		8		10		12		15		20		25	ns
Output hold from address change	t _{OH}	3		3		3		3		3		3		ns
Chip enable to output in low Z ^(3, 4, 5)	t _{LZCE}	5		5		5		5		5		5		ns
Chip disable to output in high Z ^(3, 4, 5)	t _{HCZE}		8		10		10		10		15		15	ns
Chip enable to power up time ⁽⁴⁾	t _{PU}	0		0		0		0		0		0		ns
Chip disable to power down time ⁽⁴⁾	t _{PD}		8		10		12		15		20		25	ns
Output enable access time	t _{AOE}		5		5		6		8		10		12	ns
Output enable to output in low Z ^(4, 5)	t _{LZOE}	0		0		0		0		0		0		ns
Output disable to output in high Z ^(4, 5)	t _{HZOE}		8		8		8		8		8		10	ns

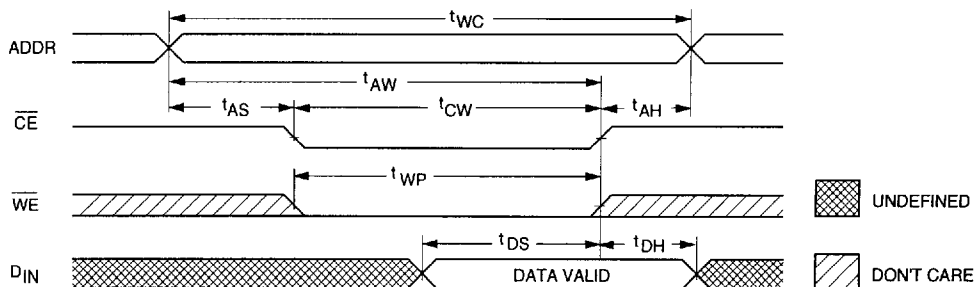
SHADED AREA = PRELIMINARY DATA.

Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)



Write Cycle No. 2 (Chip Enable Controlled)

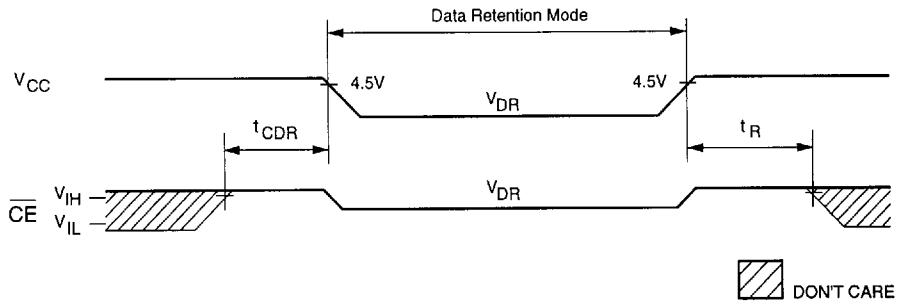


AC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)

Description	Sym	-8 ⁽⁶⁾		-10 ⁽⁶⁾		-12		-15		-20		-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE Cycle														
WRITE Cycle time	t_{WC}	8		10		12		15		20		25		ns
Chip enable to end of write	t_{CW}	8		10		10		12		13		15		ns
Address Valid to end of write	t_{AW}	8		10		10		12		13		15		ns
Address setup time	t_{AS}	0		0		0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns
Write pulse width	t_{WP}	8		10		10		11		12		15		ns
Data setup time	t_{DS}	7		7		7		8		9		10		ns
Data hold time	t_{DH}	0		0		0		0		0		0		ns
Write disable to output in low $Z^{(4, 5)}$	t_{LZWE}	0		0		0		0		0		0		ns
Write enable to output in high $Z^{(4, 5)}$	t_{HZWE}		3		3		3		3		3		5	ns

SHADED AREA = PRELIMINARY DATA.

Low V_{CC} Data Retention Waveform



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Data Retention Electrical Characteristics (LA Version Only)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data		2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$				
		$V_{CC} = 2V$	—	95	500	μA
		$V_{CC} = 3V$	—	350	750	μA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	ns
$t_R^{(4)}$	Operation Recovery Time		t_{RC}	—	—	ns

NOTES: (For 3 previous Electrical Characteristics tables)

1. The device is continuously selected. All the Chip Enables are held in their active state.
2. The address is valid prior to or coincident with the latest occurring Chip Enable.
3. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} .
4. This parameter is sampled.
5. The parameter is tested with $C_L = 5 \text{ pF}$ as shown in Figure 2. Transition is measured $\pm 200 \text{ mV}$ from steady state voltage.
6. $V_{CC} = 5V \pm 5\%$.

Ordering Information

PDM	XXXXX	A	XX	A	A	
	Device Type	Power	Speed	Package	Process / Temperature Range	
					Blank	Commercial (0° to +70°C)
					I	Industrial Temp. (-40°C to +85°C)
					P	28-pin 300 mil Plastic Dip
					D	28-pin 300 mil Cerdip
					SO	28-pin 300 mil Plastic SOJ
					T	28-pin TSOP
					8	Commercial Only
					10	
					12	
					15	
					20	
					25	
					SA	Standard Power
					LA	Low Power
					41298	256K (64K x 4) Static RAM

Chip

PDM41298

Package Type

28-pin Plastic DIP
28-pin Cerdip
28-pin Plastic SOJ
28-pin Plastic TSOP