Complete 16-Channel, 12-Bit Data Acquisition Systems

AD362/AD363/AD364

FEATURES

AD362

16-Channel Data Acquisition Input Stage with:
- Digitally Controlled Channel Selection/Mode Control
- 16 Single-Ended or 8 Differential Channels
- High Common-Mode Rejection
- 10μs Acquisition Time to 12-Bit Accuracy (0.01%)

AD363

16-Channel Data Acquisition Input Stage with:
- Digitally Controlled Channel Selection/Mode Control
- 16 Single-Ended or 8 Differential Channels
- 25kHz Throughput Rate
- Guaranteed No Missing Codes Over Temperature

AD364

16-Channel Data Acquisition Input Stage with:
- Digitally Controlled Channel Selection/Mode Control
- 16 Single-Ended or 8 Differential Channels
- 20kHz Throughput Rate
- Guaranteed No Missing Codes Over Temperature
- Three-State Buffered Digital Output

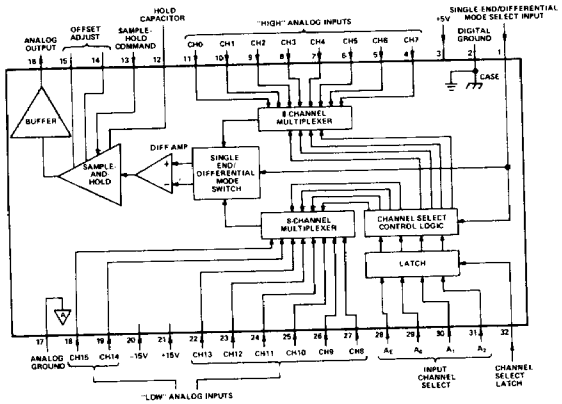
PRODUCT DESCRIPTIONS

The AD362 is a precision 16-channel data acquisition input stage which conditions, samples and holds a voltage signal for subsequent analog-to-digital conversion. The device consists of a 16-channel input multiplexer, a differential amplifier and a sample-and-hold amplifier. The product is manufactured using reliable hybrid circuit technology and is packaged in a hermetic 32-pin DIP.

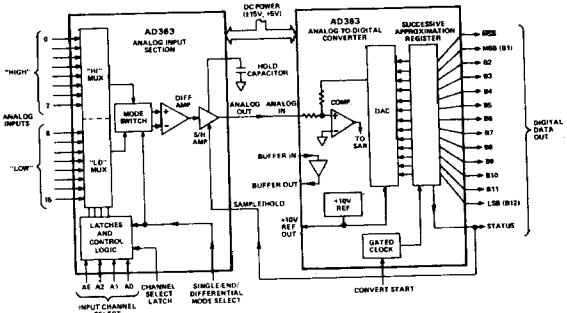
The AD363/AD364 are 16-channel data acquisition systems which condition and subsequently convert a voltage signal into a 12-bit digital word. The system consists of two devices, the analog input stage (AIS) and the analog-to-digital converter (ADC). The AIS includes a 16-channel multiplexer, a differential amplifier and a sample-and-hold amplifier. The ADC is a 12-bit successive approximation type converter with an on-board voltage reference and a three-state digital output. The AIS is manufactured using reliable hybrid circuit technology and is packaged in a 32-pin DIP. The ADC is a monolithic IC and is packaged in a 18-pin DIP.

The AD364 is a sixteen channel data acquisition system which conditions and subsequently converts a voltage signal into a 12-bit digital word. The system consists of two devices, the analog input stage (AIS) and the analog-to-digital converter (ADC). The AIS includes a 16-channel multiplexer, a differential amplifier and a sample-and-hold amplifier. The ADC is a 12-bit successive approximation type converter with an on-board voltage reference and a three-state digital output. The AIS is manufactured using reliable hybrid circuit technology and is packaged in a 32-pin DIP. The ADC is a single-chip IC and is packaged in a 28-pin DIP.

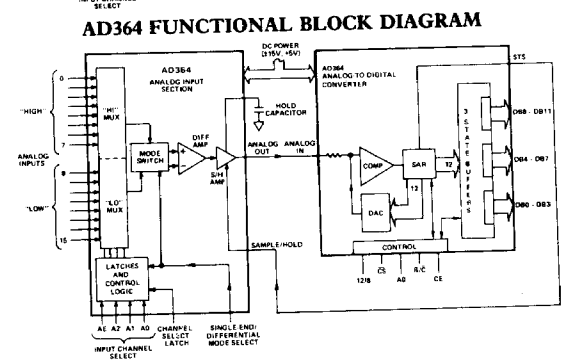
AD362 FUNCTIONAL BLOCK DIAGRAM



AD363 FUNCTIONAL BLOCK DIAGRAM



AD364 FUNCTIONAL BLOCK DIAGRAM



All products are specified for operation over both commercial (0 to +70°C) and military (−55°C to +125°C) temperature ranges. The AD362 is available fully qualified to MIL-STD-883B. The AD363 and AD364 are available with screening in accordance with the B Program of ADI Microelectronics. Please contact the factory or nearest sales office for details.

SPECIFICATIONS

(typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD362KD	AD362SD
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Range, Linear T_{min} to T_{max}	±10V min	*
Input (Bias) Current, Per Channel	±50nA	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel, Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
Offset, Channel to Channel	±2.5mV max	*
ACCURACY		
Gain Error, T_{min} to T_{max}	±0.02% FSR, max	*
Offset Error, T_{min} to T_{max}	±4mV	*
Linearity Error	±0.005% max	*
T_{min} to T_{max}	±0.01% max	*
Noise Error	1mV p-p, 0.1 to 1MHz, max	*
T_{min} to T_{max}	2mV p-p, 0.1 to 1MHz, max	*
TEMPERATURE COEFFICIENTS		
Gain, T_{min} to T_{max}	±4ppm/°C max	±2ppm/°C max
Offset, ±10V Range, T_{min} to T_{max}	±2ppm/°C max	±1.5ppm/°C max
SAMPLE AND HOLD DYNAMICS		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time, for 20V Step to ±0.01% of Final Value	18μs max (10μs typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[1]		
Input Channel Select (Pins 28-31)	4-Bit Binary, Channel Address	*
	1LS TTL Load	*
Channel Select Latch (Pin 32)	"1": Latch Transparent	*
	"0": Latched	*
	8LS TTL Loads	*
Single Ended/Differential Mode Select (Pin 1)	"0": Single-Ended Mode	*
	"1": Differential Mode (@ +4.0V min)	*
	3TTL Loads	*
Sample and Hold Command (Pin 13)	"0": Sample Mode	*
	"1": Hold Mode	*
	1TTL Load	*
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ 30mA max	*
	-15V, ±5% @ 30mA max	*
	+5V, ±5% @ 40mA max	*
Total Power Dissipation	1.1 Watts max	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[2]	-55°C to +150°C
PACKAGE OPTION[3]		
DH-32A	AD362KD	AD362SD

NOTES

[1] One TTL Load is defined as I_{IL} = -1.6mA max @ V_{IL} = 0.4V, I_{IH} = 40μA max @ V_{IH} = 2.4V.
One LS TTL Load is defined as I_{IL} = -0.36mA max @ V_{IL} = 0.4V, I_{IH} = 20μA max @ V_{IH} = 2.7V.

[2] AD362KD External Hold Capacitor is limited to +85°C; AD362 device itself may be stored at up to +150°C.

[3] See Section 13 for package outline information.

*Specifications same as AD362KD.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
(ALL MODELS)

+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
–V, Analog Supply	–16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

AD362 PIN FUNCTION DESCRIPTION

Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Ground
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Status
14	Offset Adjust
15	Offset Adjust
16	Analog Output Normally Connected to ADC "Analog In"
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, –15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch Transparent

SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD363K	AD363S
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Ranges		
Bipolar	±2.5V, ±5.0V, ±10.0V	*
Unipolar	0 to +5V, 0 to +10V	*
Input (Bias) Current, Per Channel	±50nA	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel, Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
RESOLUTION	12 BITS	*
ACCURACY		
Gain Error[1]	±0.05% FSR (Adj. to Zero)	*
Unipolar Offset Error	±10mV (Adj to Zero)	*
Bipolar Offset Error	±20mV (Adj to Zero)	*
Linearity Error	±½LSB max	*
Differential Linearity Error	±1LSB max (±½LSB typ)	*
Relative Accuracy	±0.025% FSR	*
Noise Error	1mV p-p, 0 to 1MHz	*
TEMPERATURE COEFFICIENTS		
Gain	±30ppm/°C max (±10ppm/°C typ)	±25ppm/°C max (±15ppm/°C typ)
Offset, ±10V Range	±10ppm/°C max (±5ppm/°C typ)	±8ppm/°C max (±5ppm/°C typ)
Differential Linearity	No Missing Codes Over Temperature Range	*
SIGNAL DYNAMICS		
Conversion Time[2]	25µs max (22µs typ)	*
Throughput Rate, Full Rated Accuracy	25kHz min (30kHz typ)	*
Sample and Hold		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time		
To ±0.01% of Final Value for Full Scale Step	18µs max (10µs, typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[4]		
Convert Command (to ADC Section, Pin 21)	Positive Pulse, 200ns min Width. Leading Edge ("0" to "1") Resets Register, Trailing Edge ("1" to "0") Starts Conversion.	*
	1TTL Load	*
Input Channel Select (To Analog Input Section, Pins 28-31)	4 Bit Binary, Channel Address.	*
	1LS TTL Load	*
Channel Select Latch (To Analog Input Section, Pin 32)	"1" Latch Transparent	*
	"0" Latched	*
	4LS TTL Loads	*

MODEL	AD363K	AD363S
DIGITAL INPUT SIGNALS, cont.		
Sample-Hold Command (To Analog Input Section Pin 13 Normally Connected To ADC "Status", Pin 20)	"0" Sample Mode "1" Hold Mode 2LS TTL Loads	* * *
Short Cycle (To ADC Section Pin 14)	Connect to +5V for 12 Bits Resolution. Connect to Output Bit n + 1 For n Bits Resolution. 1TTL Load	* * *
Single Ended/Differential Mode Select (To Analog Input Section, Pin 1)	"0": Single-Ended Mode "1": Differential Mode (+4.0V min) 3TTL Loads	* * *
DIGITAL OUTPUT SIGNALS[4] (All Codes Positive True)		
Parallel Data		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary/Two's Complement	*
Output Drive	2TTL Loads	*
Serial Data (NRZ Format)		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary	*
Output Drive	2TTL Loads	*
Status ($\overline{\text{Status}}$)	Logic "1" ("0") During Conversion	*
Output Drive	2TTL Loads	*
Internal Clock		
Output Drive	2TTL Loads	*
Frequency	500kHz	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±10mV	*
Max External Current	±1mA	*
Voltage Temp. Coefficient	±20ppm/°C, max	±20ppm/°C, max
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ +45mA max (+38mA typ)	*
	-15V, ±5% @ -45mA max (-38mA typ)	*
	+5V, ±5% @ +136mA max (+113mA typ)	*
Total Power Dissipation	2 watts max (1.7 watts typ)	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[3]	-55°C to +150°C
PACKAGE OPTIONS[5]		
Analog Input Section (DH-32A)	AD363KD	AD363SD
ADC Section (DH-32C)	AD363KD	AD363SD

NOTES
[1] With 50Ω, 1% fixed resistor in place of Gain Adjust pot.
[2] Conversion time of ADC Section.
[3] AD363K External Hold Capacitor is limited to +85°C; Analog Input Section and ADC Section may be stored at up to +150°C.
[4] One TTL Load is defined as I_{IL} = -1.6mA max @ V_{IL} = 0.4V, I_{IH} = 40μA max @ V_{IH} = 2.4V.
One LS TTL Load is defined as I_{IL} = -0.36mA max @ V_{IL} = 0.4V, I_{IH} = 20μA max @ V_{IH} = 2.7V.
[5] See Section 13 for package outline information.
*Specification same as AD363K.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply	+5.5V	V_{IN}, Signal	±V, Analog Supply
+V, Analog Supply	+16V	V_{IN}, Digital	0 to +V, Digital Supply
-V, Analog Supply	-16V	A_{GND} to D_{GND}	±1V

PIN FUNCTION DESCRIPTION

ANALOG INPUT SECTION

Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Ground
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 20
14	Offset Adjust
15	Offset Adjust
16	Analog Output Normally Connected to ADC "Analog In"
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"

ANALOG TO DIGITAL CONVERTER SECTION

Pin Number	Function
1	Data Bit 12 (Least Significant Bit) Out
2	Data Bit 11 Out
3	Data Bit 10 Out
4	Data Bit 9 Out
5	Data Bit 8 Out
6	Data Bit 7 Out
7	Data Bit 6 Out
8	Data Bit 5 Out
9	Data Bit 4 Out
10	Data Bit 3 Out
11	Data Bit 2 Out
12	Data Bit 1 (Most Significant Bit) Out
13	$\overline{\text{Data Bit 1}}$ ($\overline{\text{MSB}}$) Out
14	Short Cycle Control Connect to +5V for 12 Bits Connect to Bit (n+1) Out for n Bits
15	Digital Ground
16	Positive Digital Power Supply, +5V
17	$\overline{\text{Status}}$ Out "0": Conversion in Progress (Parallel Data Not Valid) "1": Conversion Complete (Parallel Data Valid)
18	+10Volt Reference Out
19	Clock Out (Runs During Conversion)
20	Status Out "0": Conversion Complete (Parallel Data Valid) "1": Conversion in Progress (Parallel Data Not Valid)
21	Convert Start In Reset Logic : ↑ Start Convert : ↓
22	Comparator In
23	Bipolar Offset Open for Unipolar Inputs Connect to ADC Pin 22 for Bipolar Inputs
24	10V Span R In
25	20V Span R In
26	Analog Ground
27	Gain Adjust
28	Positive Analog Power Supply, +15V
29	Buffer Out (For External Use)
30	Buffer In (For External Use)
31	Negative Analog Power Supply, -15V
32	Serial Data Out Each Bit Valid On Trailing (↓) Edge Clock Out, ADC Pin 19

Contact local sales office for further product details.

SPECIFICATIONS

(typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

PARAMETER	AD364J	AD364K	AD364S	AD364T	UNITS
ANALOG INPUTS					
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)				
Input Voltage Range	±10	*	*	*	V
T_{min} to T_{max}	±50	*	*	*	nA
Input (Bias) Current per Channel	10^{10}/100	*	*	*	Ω/pF
Input Impedance ON Channel	10^{10}/10	*	*	*	Ω/pF
OFF Channel	20	*	*	*	mA max (Internally Limited)
Input Fault Current (Power ON or OFF)					
Common Mode Rejection	70 min (80 typ)	*	*	*	dB
Differential Mode 1kHz 20Vp-p					
Mux Cross Talk (Any OFF Channel to Any ON Channel) 1kHz	-80 max (-90 typ)	*	*	*	dB
20V p-p	±5	*	*	*	mV max
Offset, Channel to Channel					
ACCURACY					
Gain Error[1]	0.3	*	*	*	% of FSR
Unipolar Offset Error[2]	±10	±8	*	**	mV
Bipolar Offset Error[2]	±50	±20	*	**	mV
Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Differential Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Noise Error	1mV p-p 0.1Hz to 1MHz	*	*	*	
TEMPERATURE COEFFICIENTS					
Gain	54	31	*	**	ppm/°C
Offset (±10V Range)	12	7	*	**	ppm/°C
Operating Temperature Range	0 to +70°C	*	-55°C to +125°C	***	ppm/°C
SIGNAL DYNAMICS					
Conversion Time	32 max (25 typ)	*	*	*	μs
Throughput Rate, Full Accuracy	20 min (25 typ)	*	*	*	kHz
Sample Hold					
Aperture Delay	100 max (50 typ)	*	*	*	ns
Aperture Uncertainty	500 max (100 typ)	*	*	*	ps
Acquisition Time					
To 0.01% of Final Value					
For Full Scale Step	18 max (10 typ)	*	*	*	μs
Feedthrough at 1kHz	-70 max (-80 typ)	*	*	*	dB
Droop Rate	2 max (1 typ)	*	*	*	mV/ms
DIGITAL INPUT SIGNALS					
Analog Input Section					
Input Channel Select	4 Bit Binary Address	*	*	*	
	1 LS TTL Load	*	*	*	
Channel Select Latch	"1" Latch Transparent	*	*	*	
	"0" Latched	*	*	*	
	4 LS TTL Loads	*	*	*	
Single Ended/Differential	"0" Sirgle Ended	*	*	*	
Mode Select	"1" Differential	*	*	*	
	3TTL Loads	*	*	*	
Sample and Hold Command	"0" Sample Mode	*	*	*	
	"1" Hold Mode	*	*	*	
	1TTL Load	*	*	*	
ADC Section[3] $4.5 \leq V_L \leq 5.5$					
Logic Input Threshold					
T_{min} to T_{max}		*	*	*	V min
Logic "1"	2.0	*	*	*	V max
Logic "0"	0.8				
Logic Input Current					
T_{min} to T_{max}		*	*	*	μA max
Logic "1"	10	*	*	*	μA max
Logic "0"	10				

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PARAMETER	AD364J	AD364K	AD364S	AD364T	UNITS
DIGITAL OUTPUT SIGNALS					
Logic Outputs T_{min} to T_{max}					
Sink Current V_{OUT} = 0.4V	1.6	*	*	*	mA min
Source Current V_{OUT} = 2.4V	0.5	*	*	*	mA min
Output Leakage When In Three State	±40	*	*	*	μA max
Output Coding					
Unipolar	Positive True Binary	*	*	*	
Bipolar	Positive True Offset Binary	*	*	*	
POWER REQUIREMENTS					
Supply Voltages/Currents	+15V, ±5% @ 36mA max	*	*	*	
	−15V, ±5% @ 65mA max	*	*	*	
	+5V, ±5% @ 75mA max	*	*	*	
PACKAGE OPTIONS[4]					
Analog Input Section (DH-32A)	AD364J	AD364K	AD364S	AD364T	
ADC Section (D-28)	AD364J	AD364K	AD364S	AD364T	

NOTES

[1] With 50Ω resistor from REF IN to REF OUT. Adjustable to zero.
[2] Adjustable to zero.
[3] 12/$\overline{8}$ line must be hard wired to V_{LOGIC} or digital common.
[4] See Section 13 for package outline information.
*Specifications same as AD364J.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
−V, Analog Supply	−16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

PIN FUNCTION DESCRIPTION

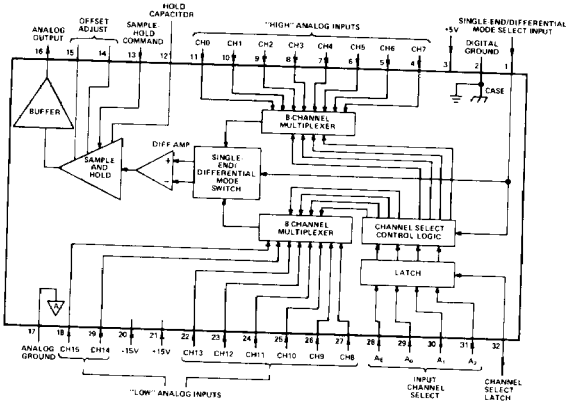
ANALOG INPUT SECTION

Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Common
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 28
14	Offset Adjust
15	Offset Adjust
16	Analog Output Normally Connected to ADC "Analog In"
17	Analog Common
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"

ANALOG TO DIGITAL CONVERTER SECTION

Pin Number	Function
1	Logic Power Supply, +5V
2	Data Mode Select (12/$\overline{8}$) "0": 8 Upper Bits or 4 Lower Bits as Selected by Byte Select (A_0)
3	Chip Select ($\overline{CS}$) "0": Device Selected "1": Device Inhibited
4	Byte Address/Short Cycle (A_0) "0": Upper 8 Bits Enabled (12/$\overline{8}$ "0")/ 12 Bit Cycle "1": Lower 4 Bits Enabled (12/$\overline{8}$ "1")/ 8 Bit Cycle
5	Read Convert (R/$\overline{C}$) "0": Convert Start "1": Read Enable
6	Chip Enable (CE) ↓: R/$\overline{C}$ "0", $\overline{CS}$ "0" Initiates Conversion ↓: R/$\overline{C}$ "1", $\overline{CS}$ "0" Initiates Read "0": Device Disabled "1": Device Enabled
7	Analog Power Supply, +15V (V_{CC})
8	Reference Out, +10V
9	Analog Common (AC)
10	Reference In
11	Analog Power Supply, -15V (V_{EE})
12	Bipolar Offset
13	10 Volt Span Input
14	20 Volt Span Input
15	Digital Common (DC)
16	Data Bit 0
17	Data Bit 1
18	Data Bit 2
19	Data Bit 3
20	Data Bit 4
21	Data Bit 5
22	Data Bit 6
23	Data Bit 7
24	Data Bit 8
25	Data Bit 9
26	Data Bit 10
27	Data Bit 11
28	Status Out

Contact local sales office for further product details.



AD362 Functional Block Diagram

Concept

The AD362 is intended to be used in conjunction with a high-speed precision analog-to-digital converter to form a complete data acquisition system (DAS) in microcircuit form. Figure 1 shows a general AD362-with-ADC DAS application.

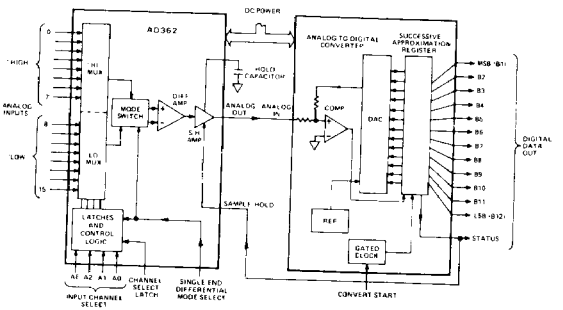


Figure 1. AD362 with ADC as a Complete Data Acquisition System

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

System Timing

Figure 2 is a timing diagram for the AD362 connected as shown in Figure 1 and operating at maximum conversion rate. The ADC is assumed to be a conventional 12 bit type such as the AD572 or AD ADC80.

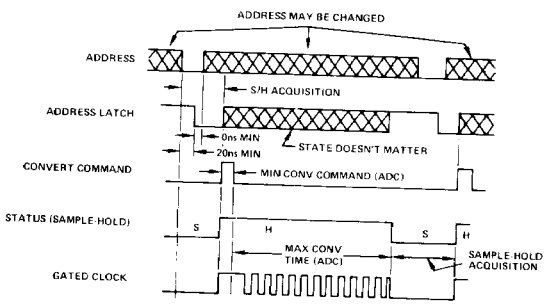


Figure 2. DAS Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy", the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

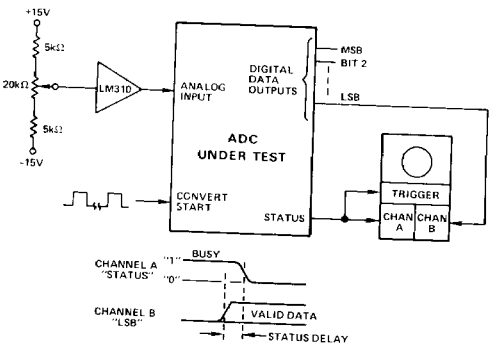


Figure 3. ADC Status Valid Test

NOTE:

Valid Output Data

Not all ADCs have all data bits available when Status indicates that the conversion is complete. Successive approximation ADCs based on the 2502/3/4 type of register must have a Status delay built in or the final data bit will lag Status by approximately 50ns. This will result in two problems:

1. The sample-and-hold will return to Sample, disturbing the analog input to the ADC as it is attempting to convert the least significant bit. This may result in an error.
2. If the falling edge of Status is being used to load the data into a register, the least significant bit will not be valid when loaded.

An external 100ns delay or use of an ADC with a valid Status output is necessary to prevent this problem. The applications shown in this data sheet ensure that all data bits will be valid.

The following test may be made to determine if the ADC Status timing is correct:

1. Connect the ADC under test as shown in Figure 3.

2. Trigger the oscilloscope on Status. Delay the display such that Status is mid-screen.
3. Observe the LSB data output of the ADC.
4. Vary the analog input control to confirm that the LSB transition precedes the Status transition.

Single-Ended/Differential Mode Control

The AD362 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a non-TTL logic input applied to pin 1 of the Analog Input Section:

"0": Single-Ended (16 channels)
"1": Differential (8 channels) (+4.0V min)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table I is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table I. Input Channel Addressing Truth Table

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "Hold" mode).

Input Channel Address Latch

The AD362 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (pin 32) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition (level-triggered).

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (pin 13) is normally connected to the Status output (pin 20) from an analog to digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1", putting the sample-and-hold into the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/ DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous Sample mode.

Hold Capacitor

A 2000pF capacitor is provided with each AD362. One side of this capacitor is wired to pin 12, the other to analog ground as close to pin 17 as possible. The capacitor provided with the AD362KD is Polystyrene while the wider operating temperature range of the AD362SD requires a Teflon capacitor (supplied).

Smaller capacitors will allow slightly faster operation, but only with increased noise and decreased precision. 1000pF will typically allow acquisition to 0.1% in four microseconds.

Larger capacitors may be substituted to reduce noise, and sample-to-hold offset, but acquisition time of the sample-and-hold will be extended. If less than 12 bits of accuracy is required, a smaller capacitor may be used. This will shorten the S/H acquisition time. In all cases, the proper capacitor dielectric must be used; i.e., Polystyrene (AD326KD only) or Teflon (AD362KD or SD). Other types of capacitors may

have higher dielectric absorption (memory) and will cause errors. CAUTION: Polystyrene capacitors will be destroyed if subjected to temperatures above +85°C. No capacitor is required if the sample-and-hold is not used.

Analog Input Section Offset Adjust Circuit

Although the offset voltage of the AD362 may be adjusted, that adjustment is normally performed at the ADC. In some special applications, however, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to the AD362 voltage offset and if a gain stage was to be inserted between the AD362 and the ADC. To adjust the offset of the AD362, the circuit shown in Figure 4 is recommended.

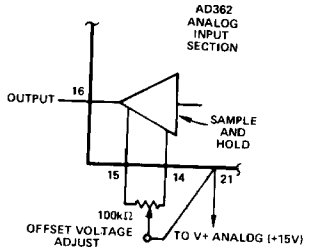


Figure 4. AD362 Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (pin 17) and Digital Ground (pin 2) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AD362 as possible. The case is connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with the AD362, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes as shown in Figure 5. This will protect the AD362 from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The device will operate properly with as much as ±200mV between grounds, however this difference will be reflected directly as an input offset voltage.

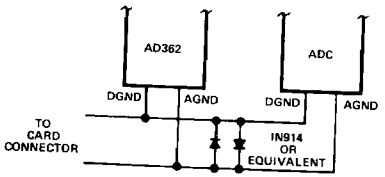


Figure 5. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

Contact local sales office for further details.