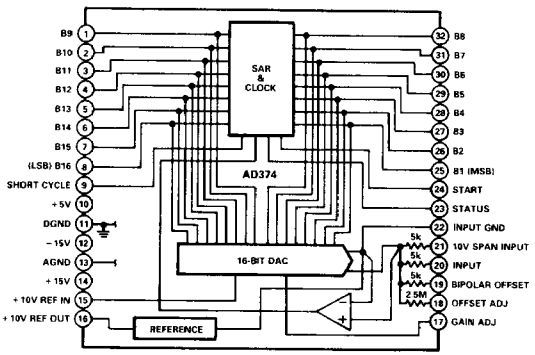
Low-Power, True 16-Bit A/D Converter

AD374

FEATURES

Complete 16-Bit Converter with Reference and Clock
± 1/2LSB Nonlinearity
No Missing Codes to 16 Bits Over Temperature
1/4LSB Transition Noise
Ultralow Power 275mW max
65μs Conversion Time
Short Cycle Capability
32-Pin Hermetic Metal DIP

AD374 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD374 is an ultralow-power, high resolution, 16-bit analog-to-digital converter including reference, clock and a segmented CMOS DAC. The segmented DAC is inherently monotonic, and is the key to providing no-missing-code performance to the 16-bit level. The AD374 also uses a proprietary CMOS Successive Approximation Register (SAR) and dissipates only 230mW (275 max.)

Important performance characteristics of the AD374 include 16-bit integral linearity at 25°C, 14-bit integral over temperature (−40°C to +85°C), 16-bit no-missing-code performance over temperature, and 60μs conversion time. The precision segmented DAC and laser-trimmed thin-film resistors provide the linearity and wide temperature range performance. The AD374 provides data in TTL or 5V CMOS compatible parallel form. The part includes an internal low drift reference; however, the reference out/in connection is external. This allows the user to take full advantage of the low converter gain drift (2ppm FSR/°C) in applications where the internal reference drift (5ppm FSR/°C) is insufficient.

Three user selectable-input voltage ranges are provided, 0 to +10V, ±5V and ±10V.

PRODUCT HIGHLIGHTS

1. The AD374 provides true 16-bit resolution with ±1LSB maximum differential linearity error over temperature.
2. The ultralow power dissipation of 275mW maximum makes the AD374 ideal for remote or battery operated data acquisition applications.
3. Conversion time is 60μs typical to 16 bits, with short cycle available.
4. Two binary codes are available on the AD374 output. Straight binary (SB) is available for the unipolar (0 to +10V) input voltage range, and offset binary (OB) for the bipolar input ranges (±5V, ±10V). Twos complement (TC) coding may be obtained by inverting Pin 25 (MSB).
5. The AD374 is a successive approximation ADC. The proprietary CMOS chips used provide for minimal chip count and high reliability. The 16-bit segmented DAC is inherently monotonic, providing for excellent stability over temperature.
6. The AD374 is packaged in a 32-pin hermetic metal DIP.

SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15, +5 volts unless otherwise noted)

Model	AD374AM	AD374BM	Units
RESOLUTION	16 (max)	*	Bits
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±5, ±10	*	Volts
Unipolar	0 to +10	*	Volts
Impedance (Direct Input)			
10V Span	2.5	*	kΩ
20V Span	5.0	*	kΩ
DIGITAL INPUTS[1]			
Convert Command	Positive Pulse 50ns Wide (min) Trailing Edge Initiates Conversion		
Logic Loading	1	*	LS TTL Load
TRANSFER CHARACTERISTICS[2]			
ACCURACY			
Gain Error	TBD	*	%
Offset Error			
Unipolar	TBD	*	% of FSR[4]
Bipolar	TBD	*	% of FSR
Linearity Error (max)	±0.0015 (±0.006 max)	*	% of FSR
Inherent Quantization Error	±1/2	*	LSB
Differential Linearity Error	±0.00153	±0.00076	% of FSR
3σNoise at Transitions (pk-pk)	1/4	*	LSB
POWER SUPPLY SENSITIVITY			
±15V dc (±0.75V)	0.001	*	% of FSR/% ΔV_S
+5V dc (±0.25V)	0.001	*	% of FSR/% ΔV_S
CONVERSION TIME[6]			
14 Bits	58 max	*	µs
15 Bits	61.5 max	*	µs
16 Bits	65 max	*	µs
WARM-UP TIME	2	*	Minutes
DRIFT[5]			
Gain	TBD	*	ppm/°C
Offset			
Unipolar	TBD	*	ppm of FSR/°C
Bipolar (Zero)	TBD	*	ppm of FSR/°C
Linearity (T_{min} to T_{max})	±0.006 (max)	*	% of FSR
Guaranteed No Missing Code Temperature Range	−40 to +85 (15 bits)	−40 to +85 (16 bits)	°C
DIGITAL OUTPUT[1]			
(All Codes Complementary)			
Parallel			
Output Codes[7]			
Unipolar	SB	*	
Bipolar	OB, TC[8]	*	
Output Drive	2	*	TTL Loads
Status		Logic "1" During Conversion	
Status Output Drive	2 (max)	*	TTL Loads
Delay, Falling Edge of Status to LSB Valid	0	*	ns (max)
REFERENCE OUTPUT			
Nominal Value	10	*	Volts
Accuracy	±0.5		%
Drift	±5 (±20 max)	*	ppm/°C
Noise	TBD	*	nV per $\sqrt{Hz}$
POWER SUPPLY REQUIREMENTS			
Power Consumption	230 (275 max)	*	mW
Rated Voltage, Analog	±15 ±0.5 (max)	*	V dc
Rated Voltage, Digital	+5 ±0.25 (max)	*	V dc
Supply Drain +15V dc	+6.3 (8.8 max)	*	mA
Supply Drain −15V dc	−6.9 (8.6 max)	*	mA
Supply Drain +5V dc	+6.6 (7.9 max)	*	mA
TEMPERATURE RANGE			
Specification	−40 to +85	*	°C
Operating (Derated)	−55 to +125	*	°C

NOTES
[1]Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min.
[2]Tested on ±10V and 0 to +10V ranges.
[3]Adjustable to zero.
[4]Full-Scale Range.
[5]Guaranteed but not 100% production tested.
[6]Conversion time may be shortened with "Short Cycle" set for lower resolution.
[7]SB – Straight Binary. OB – Offset Binary. TC – Twos Complement.
[8]TC coding obtained by inverting MSB (Pin 1).
*Specifications same as AD374AM.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	−55°C to +125°C
Storage Temperature	−55°C to +150°C
+15V Supply	+17V
−15V Supply	−17V
+5V Supply	+7V
Digital Inputs	V_{CC}
Analog Inputs	±15V

THEORY OF OPERATION

The AD374 uses a conventional successive approximation hardware algorithm, in combination with a 16-bit monotonic digital-to-analog converter (DAC) and low noise comparator, to digitize analog inputs to 16-bit resolution and accuracy. An input resistor converts the analog input voltage to a current that is subtracted from the DAC output current. The differential current generates a voltage relative to ground that is sensed by the comparator. The comparator output is used by a CMOS SAR chip to determine whether or not to keep or reset the current bit on the rising edge of the internal clock.

The 16-bit DAC's least significant 14 bits are generated from a monolithic 14-bit linear CMOS DAC, operated in the current-steering mode. The 16-bit DAC's two most significant bits (MSBs) are generated by using one of four matched bipolar current sources as the 14-bit DAC reference. When a current source is not selected as the reference, it is steered to either the DAC output or to ground.

The above is commonly referred to as a fully segmented DAC architecture. Effectively, the digital input (code) versus analog output (current) transfer function is comprised of four segments. The linearity of each segment is the linearity of the 14-bit DAC divided by four since each segment contributes to only one fourth of the 16-bit DAC's linearity. The segmentation scheme guarantees DAC monotonicity to 16 bits over time and temperature. The four current sources utilize matched NPN transistors and thin-film resistors that are trimmed at the package level to ensure an overall 16-bit linear transfer function.

The proper mix of bipolar and CMOS technologies in the AD374 is the key to the device's performance and ultralow power consumption. Attention to the separation of power and signal grounds, as well as feed-through from the SAR and clock, within the device contributes to the circuit's realization.

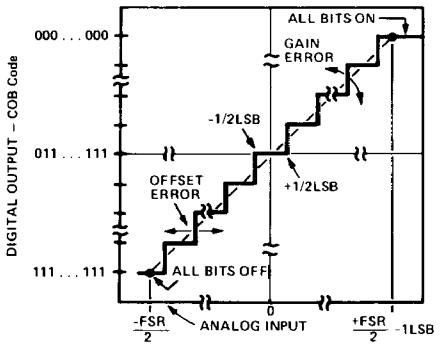


Figure 1. Transfer Characteristics for an Ideal Bipolar A/D

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD374 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

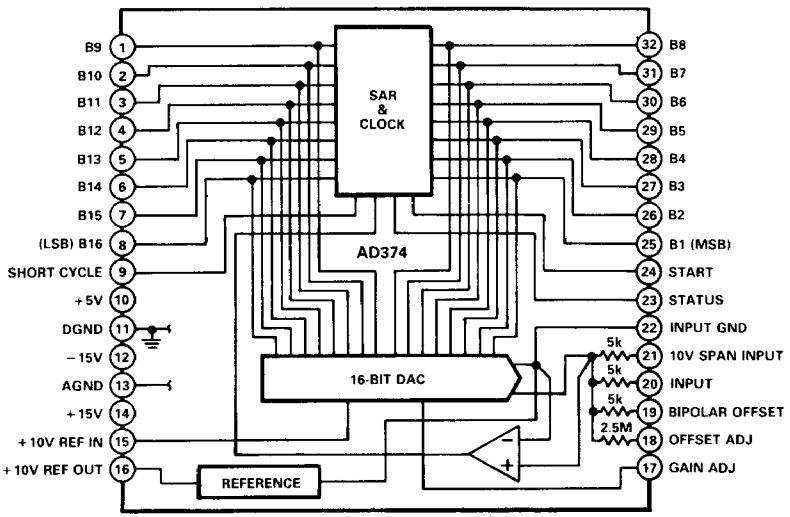


Figure 2. AD374 Functional Block Diagram and Pinout

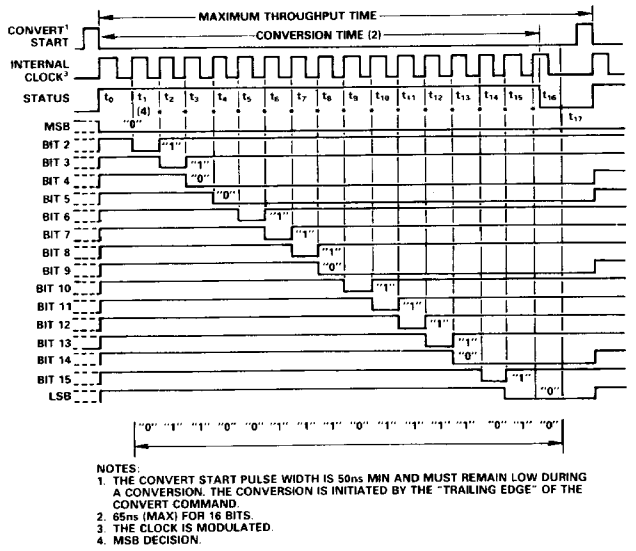


Figure 3. Timing Diagram (Binary Code 0110011101110110)

TIMING

The timing diagram is shown in Figure 3. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B1 is reset and B2 – B16 are set unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

GAIN ADJUSTMENT

Gain (or + FS) errors can be removed with an external 100ppm/°C potentiometer or a voltage output DAC. The gain adjustment sensitivity is typically 0.15% FSR/V or ±0.75% FSR when adjusted with a ±5V output DAC. A 12-bit ±5V output DAC should adjust the AD374 +FS error to within 1/4LSB$_{16}$. If gain adjustment is not required, connect Pin 17 to 22.

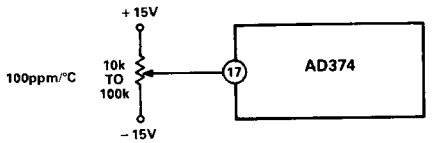


Figure 4. Gain Adjustment with Potentiometer (±2.2% FSR)

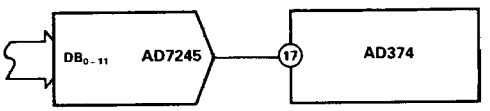


Figure 5. Gain Adjustment with DAC (±0.75% FSR)

OFFSET ADJUSTMENT

Offset (or – Full-Scale) errors can also be removed with an external 100ppm/°C potentiometer. The potentiometer is connected across ±V_S with its slider connected directly to Pin 18 (Figure 6). Pin 18 is internally decoupled from the comparator input by 2.5MΩ. The offset adjustment sensitivity is typically ±0.15% FSR.

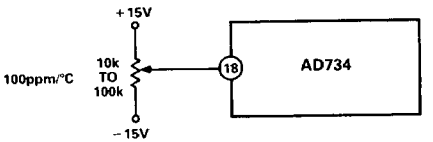


Figure 6. Offset Adjustment with Potentiometer (±0.15% FSR)

A ±5V output DAC (Figure 7) can provide 0.01% FSR/V or ±0.05% FSR adjustment sensitivity under software control. An 8-bit ±5V DAC should adjust the AD374 – FS error to within 1/4LSB$_{16}$. If offset adjustment is not required, connect Pin 18 to Pin 22.

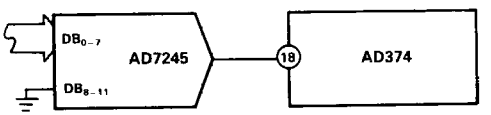


Figure 7. Offset Adjustment with DAC (±0.05% FSR)

DIGITAL OUTPUT DATA

Parallel data from HCMOS storage registers is in positive true form (Logic "1" = 0V and Logic "0" = 2.4V). Parallel data output coding is straight binary for unipolar ranges and offset binary for bipolar ranges.

Short Cycle Input: A short cycle input, Pin 9, permits the timing cycle, shown in Figure 3, to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 15-bit resolution is desired, Pin 9 is connected to Bit 16 output Pin 8. The conversion cycle then terminates and the STATUS flag resets after the Bit 15 decision (timing diagram of Figure 3). Short cycle connections and associated conversion times are summarized in Table I.

SHORT CYCLE CONNECTIONS

Bits	Conversion Time (μs) Typ	Time (μs) Max	Connect Pin 9 to
16	60.0	65.0	–
15	56.5	61.5	8
14	53.0	58.0	7
13	49.5	54.5	6
12	48.0	53.0	5

Table I.

INPUT SCALING

The AD374 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figures 8 and 9 for circuit details.

INPUT RANGE CONNECTIONS

Range	Pin 19 to	Pin 20 to	Pin 21 to
0 to + 10V	22	Input	20
− 5V to + 5V	15	Input	20
− 10V to + 10V	15	Input	22

Table II.

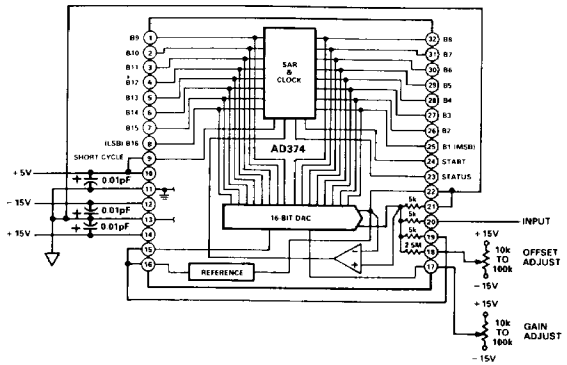


Figure 8. Connections for Bipolar ± 10V Input Range

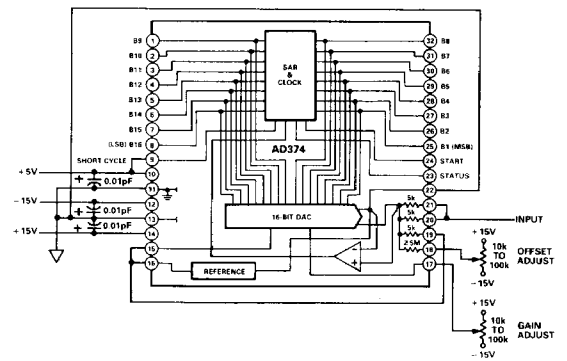


Figure 9. Connections for Bipolar ± 5V Input Range

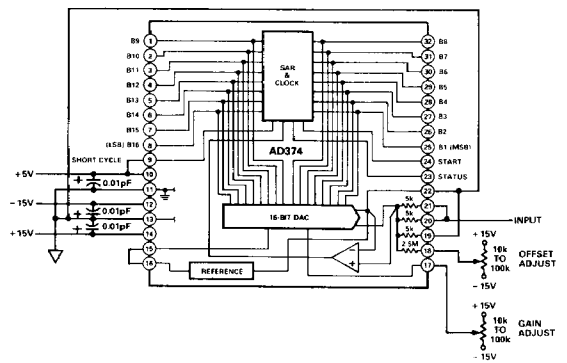


Figure 10. Connections for Unipolar 0 to + 10V Input Range

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 4 and 6, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

For 0 to +10V Range: Set analog input to +1LSB = 0.000153V. Adjust Zero for digital output = 0000 0000 0000 0001. Zero is now calibrated. Set analog input to +FSR − 2LSB = +9.999694V. Adjust Gain for 1111 1111 1111 1110 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000V; digital output code should be 1000 0000 0000 0000.

For −10V to +10V Range: Set analog input to −9.999847V; adjust zero for 1111 1111 1111 10 digital output (complementary offset binary) code. Set analog input to 9.999388V; adjust Gain for 1111 1111 1111 1110 digital output (complementary offset binary) code. Half-scale calibration check; set analog input to 0.00000V; digital output (complementary offset binary) code should be 1000 0000 0000 0000.

Other Ranges: Representative digital coding for the ±5V range is given above. Coding relationships and calibration points can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *Analog-Digital Conversion Handbook* edited by D.H. Sheingold, Prentice-Hall, Inc., 1986.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Three separate ground connections are used internal to the AD374. Digital ground (Pin 11) is used as the return path for current flowing in the digital logic, clock and comparator output stage. Analog ground (Pin 13) carries the imbalance current between the +15V and −15V power supplies. Analog ground also serves to shield the device, and a single point connection between it and the case exists internally (so don't ground the case).

Input ground (Pin 22) carries the difference current between the full scale (4mA) and input currents (0 to 4mA). The current flowing through this pin is a maximum at −FS and decreases linearly with output code to zero at +FS. The +10V reference and (−) input of the comparator are referred to this pin internally.

Code Under Test MSB LSB	Range	Low Side Transition Values ±10V	±5V	0 to +10V
111 . . . 111*	+ Full Scale	+10V −3/2LSB	+5V −3/2LSB	+10V −3/2LSB
100 . . . 000	Midscale	0-1/2LSB	0-1/2LSB	+5V-1/2LSB
000 . . . 001	− Full Scale	−10V +1/2LSB	−5V +1/2LSB	0V +1/2LSB

*Voltages given are the nominal value for transition to the code specified.

Table III. Transition Values vs. Calibration Codes

Analog Input Voltage Range		±10V	±5V	0V to +10V
Code Designation		OB* or TC**	OB* or TC**	SB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$
	n = 13	2.44mV	1.22mV	1.22mV
	n = 14	1.22mV	0.61mV	0.61mV
	n = 15	0.61mV	0.31mV	0.31mV
	n = 16	306μV	153μV	153μV

NOTES
*OB = Offset Binary.
**TC = Twos Complement – achieved by using an inverter to complement the most significant bit to produce ($\overline{MSB}$).
***SB = Straight Binary.

Table IV. Input Voltage Range and LSB Values

Sixteen-bit performance from the AD374 can be realized when all three of these pins (11, 13 and 22) are tied together with the input signal ground in a star configuration as close to the device as possible. Ideally, this point would then be tied to a low impedance ground plane underneath the device where the power supplies should be bypassed with 10μF tantalum capacitors in parallel with 0.1μF ceramic capacitors.

Printed wiring board layout is extremely critical when using high-resolution analog-to-digital converters. High-speed logic level signals are present on the same board as low-level analog signals. If signal conditioning or high-gain amplification is also included, the problems are compounded.

Figure 11 shows what can happen in an inadequate design. An amplifier with a gain of 1,000 is used to amplify a low-level 0-to-10mV signal and present the resulting 0-to-10V signal to the ADC. Suppose that, due to board strays, there are 1,000MΩ of resistance and 0.1pF of capacitance betwen the summing node of A1 and of one of the digital logic lines. The amount of dc pickup, relative to the analog input, is 10^{-6} (1,000Ω/1,000MΩ), or 5μV −0.05% of full scale. On the other hand, assuming feedback capacitance of 10pF, a 5V logic edge would be attenuated by 0.1pF/10pF, in the first stage, while the analog signal would experience a gain of 31.6, so 5V of logic would insert a 1.6mV spike, referred to the input, or 16% of full scale. However, it would be damped out within 2μs.

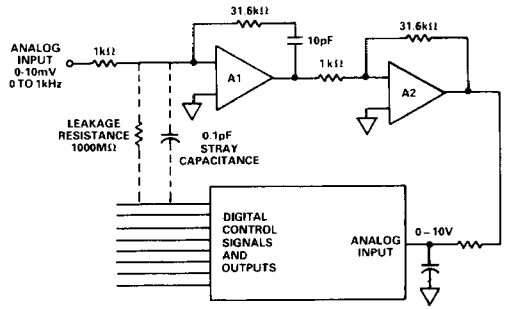


Figure 11. Example of Effects of Stray Capacitance and Leakage Resistance

Effective solutions to this problem would involve distance – keeping high-level and digital lines as far as possible from low-level analog lines; isolation – using shielding and guarding to isolate low-level signals; and orientation – where leads must cross, doing so at right angles, using twisted pairs to balance pickup, etc.

If grounded guards are placed around the summing nodes of the amplifiers, stray capacitance from digital signal leads is to ground, rather than to the sensitive nodes. Not all guards need be grounded guards; in order to be fully effective for low-frequency and dc common-mode pickup, as well as ac strays, guarding must be done at the same potential as the signal to be guarded.

Unfortunately, due to space limitations, optimum guarding and grounding practice in the neighborhood of high-resolution ADCs is sometimes difficult to achieve, and converter noise is the likely result. It is helpful to have a workable procedure for tracking down interference-noise problems. A more thorough treatment of the subject is given in Analog Devices' *Analog-Digital Conversion Handbook* (New Jersey: Prentice-Hall, 1986), by the engineering staff of Analog Devices, Inc.

SAMPLED DATA ACQUISITION

In high-resolution conversion, the dynamic characteristics, even of slowly varying signals, must be considered. In order to faithfully digitize a signal, of frequency f, and resolution n, to 1LSB, the conversion time (aperture) uncertaintly T_A, must be less than:

$$T_A = \frac{2^{-n}}{2\pi f}$$

If, for example, a 16-bit successive-approximation converter can complete a conversion within 60μs, the highest frequency that can be converted with 16-bit resolution is 0.08Hz. In order to convert at a sampling rate of 25kHz, to handle, say, 10kHz input signals, a sample-hold must be used ahead of the converter with an aperture uncertainty better than 0.5ns.

Sampling a 7kHz signal to 16 bits requires the following specifications (actually, they should be considerably better when considering worst-case performance, but these are generally considered acceptable in the industry):

Aperture Jitter	1.0ns
Slew Rate (20V pk-pk)	1.26V/μs
Feedthrough (1/2LSB max)	−102dB
Droop Rate (1/2LSB max in 60μs)	2.5μV/μs (20V pk-pk)
Acquisition Time (± LSB max with 60μs ADC)	10μs
Pedestal Shift (max)	−96.3dB
Gain Tempco (± 10°C ambient)	1.5ppm/°C
Thermal Tail (60μs)	152μV
Linearity Error (max)	± 0.0015% FSR

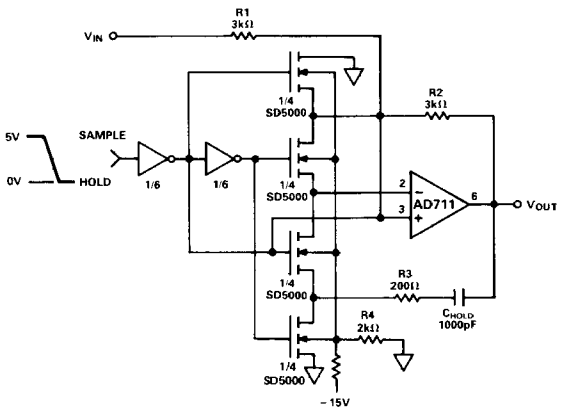


Figure 12. Sample/Hold Amplifier

Aperture jitter is the uncertainty about when a sample is taken; it must be considered, even though the T-H control line is driven by a precise clock. Aperture jitter is the result of noise within the switching network which modulates the phase of the hold command. The aperture error which results from this jitter is directly related to the dV/dt of the analog input. All high-speed sampled-data systems depend on low aperture jitter for digitizing high-frequency signals for spectrum analysis and accurate signal reconstruction.

The T-H amplifier's slew rate determines the maximum switching rate when following changes between multiplexed input signals.

The feedthrough from input to output while in the hold mode should be less than 1LSB. The hold mode droop rate should be less than 1LSB of droop in the output during the conversion time of the A/D converter. For a 16-bit ADC with a 60μs conversion time, for example, the maximum droop rate, as noted above, is 1/2LSB per 60μs; since 1LSB = $10/2^{16}$V = 152.6μV, the maximum droop rate is 2.5μV/μs.

The linearity error should be less than 1LSB over the transfer function, as set by the relative accuracy of the A/D converter. The track-hold's acquisition time and settling time (t_{A+S}), along with the conversion time of the A/D converter (t_C), determine the highest sampling rate, f_S.

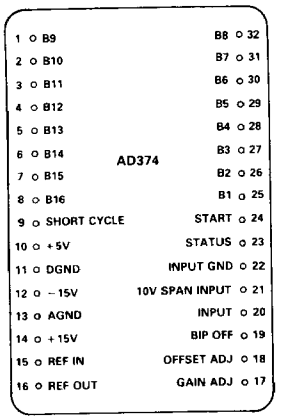
$$f_S = \frac{1}{t_{A+S} + t_C}$$

This, in turn, will determine the highest input signal frequency that can be sampled at a minimum of twice per cycle, according to Nyquist sampling theory.

The pedestal shift due to input signal changes should either be linear, to be seen as gain error, or negligible. Feedthrough should also be negligible. The temperature coefficients for drift should be low enough so that the full accuracy is maintained over some minimum temperature range. The droop rate and pedestal will shift more over temperature for temperature ranges above +70°C, generally a considerably higher temperature range than these devices will experience for most of the applications in which they are used. An additional factor to consider with high-resolution converters is the noise in the T-H during the track mode, since it will affect the value that is sampled when the T-H is switched in hold. This noise must be added (root sum-of-squares) to converter noise when calculating the actual noise error in an ADC.

Figure 12 shows a high-resolution track-and-hold circuit that can acquire a sample in 5μs to 0.003% (20V swing). The AD711 is well suited for precision track-and-hold circuits. R1 and R2 set the circuit gain. R4 and R5 insure complete shut-off of the D-MOS FET switches at logic zero. The SD5000 D-MOS switch is recommended for its fast transition speed and low on resistance.

AD374 PIN CONFIGURATION



ORDERING GUIDE

Model	Max DNL Error	Temperature Range	Package Option*
AD374AM	±0.00153% FSR	−40°C to +85°C	DH-32A
AD374BM	±0.00076% FSR	−40°C to +85°C	DH-32A
AC1H72	Two 16-Pin Strip Sockets		

*See Section 13 for package outline information.