ANALOG DEVICES

12-Bit Successive Approximation High Accuracy A/D Converters

AD5210 Series

1.1 Scope.

This specification covers the detail requirements for hybrid, 12-bit, successive approximation, high accuracy, analog-to-digital converters.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

	Device	Part Number
±5V Ext Ref	−12	AD5214TD/883B
±10V Int Ref	−13	AD5212TD/883B
±10V Ext Ref	−14	AD5215TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000:

Device Type	Package Outline
−12	DH-24E
−13, −14	

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Positive Supply Voltage ($+V_{CC}$)	+18V
Negative Supply Voltage ($-V_{EE}$)	−18V
Logic Supply Voltage ($+V_{DD}$)	+7V
Analog Input Voltage	±25V
Digital Input Voltage	+5.5V
Reference Input Voltage (Ext. Ref versions only)	0 to −15V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C
Junction Temperature	+175°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 5°C/W

θ_{JA} = 40°C/W

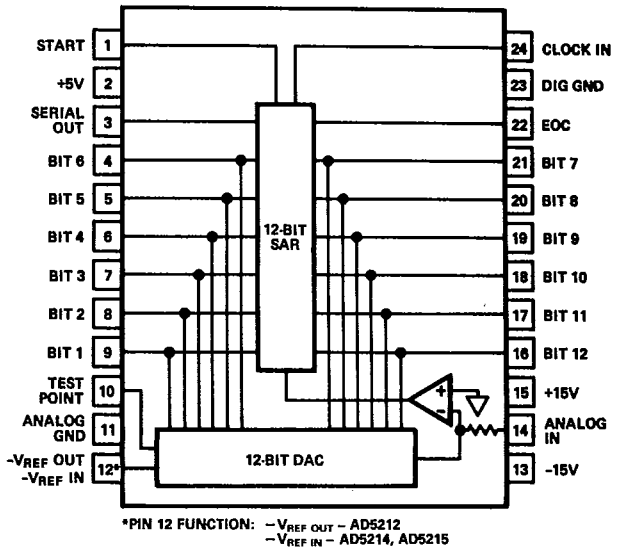
Table 1.

Test	Symbol	Device	Design Limit @+25°C	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition[1]	Units
Analog Input Voltage	V_{IN}	−12	±5				Ext. −10.000 V_{REF}	V FS
	V_{IN}	−13	±10				Internal Reference	V FS
		−14					Ext. −10.000 V_{REF}	
Linearity Error	L_E	All	1/2	1/2	1/2		At Major Carries (Abbreviated Test)	±LSB max
Differential Linearity Error[2]	DNL	All	0.9	0.9	0.9		At Major Carries	±LSB max
Zero Error	Z_E	All	1	1	2		V_{IN} = 0V	±LSB max
±FS Absolute Accuracy Error Over Temperature	TC_{AE}	−13	0.4		0.4		With Internal Reference	±% FSR max
		−12, 14	0.1		0.1		With Ext. −10.000 V_{REF}	±% FSR max
±FS Absolute Accuracy Error @ +25°C	A_E	All	2	2			With Ext. −10.000 V_{REF} on Ext. Ref. Versions	±LSB max
Conversion Time	t_{CONV}	All	13	13			With 1MHz Clock	µs max
Serial/Parallel Code Error Match	SP_{CM}	All	0	0			Random	±Bits
Logic Inputs	I_{INL} I_{INH} I_{INH}	All	0.6 0.04 1.0	0.6 0.04 1.0			V_{INL} = 0.3V V_{INH} = 2.4V V_{INH} = 5.5V	mA max
Logic Outputs	V_{OL} V_{OH}		0.4 2.4	0.4 2.4			I_{OL} = 3.2mA I_{OH} = −80µA	V max V min
Short Circuit Current	I_{SC}		16	16			@0V	mA min
Clock Input Pulse Width	t_{CW}	All	100	100				ns min
Power Supply Rejection	PSRR	All	0.005			0.005	All Supplies ±3% Variation	%/% max
Power Supply Current	I_{CC} I_{EE} I_{LOGIC}	All	28 35 68	28 35 68				mA max
Power Supplies	V_{CC} V_{EE} V_{LOGIC}	All	+15 ±10% −15 ±10% +5 ±10%					V
Power Dissipation	PD	−12, 14	0.8			0.8		Watts max
		−13	1.0			1.0		

NOTES
[1]T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V unless otherwise noted.
[2]Guaranteed no missing codes.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View



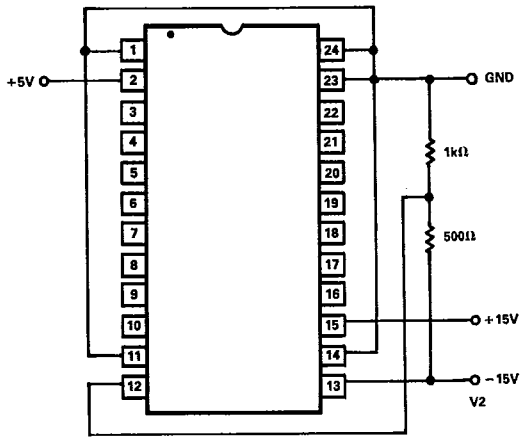
*PIN 12 FUNCTION: $-V_{REF\ OUT}$ – AD5212
$-V_{REF\ IN}$ – AD5214, AD5215

3.2.4 Microcircuit Technology Group.

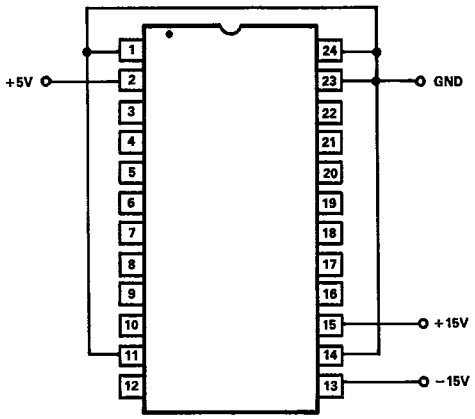
This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



Devices 12, 14



Device 13

6.0 Input Range.

The analog input range for each device is specified in Table 1.

6.1 Digital Output Data.

Both parallel and serial data from TTL storage registers are in negative true form using complementary offset binary (COB) coding. Parallel data becomes valid approximately 40ns after the EOC STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked 40ns after the "1" to "0" transition of the EOC STATUS flag on pin 22. Serial data coding is also complementary offset binary (COB) coding. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges and bit decisions are made on following rising clock edges. Serial data is guaranteed valid 200ns after the bit decision, permitting serial data to be clocked directly into a receiving register on the following falling clock edge, if it occurs 200ns after the rising edge. There are 13 negative-going clock edges in the complete 12-bit conversion cycle. Using a 12-bit serial input register, the first edge shifts in an invalid bit into the register, which is shifted out on the 13th negative going clock edge. The digital output codes corresponding to analog input voltage for calibration and test are shown in Table 2 below.

Table 2. Logic Coding (Complementary Offset Binary)

Device 12	Device 13, 14	MSB LSB
+5.0000V	+10.000V	0 0 0 0 0 0 0 0 0 0 0
0.0000V	0.000V	1 0 0 0 0 0 0 0 0 0 0
−4.9976V	−9.995V	1 1 1 1 1 1 1 1 1 1 1

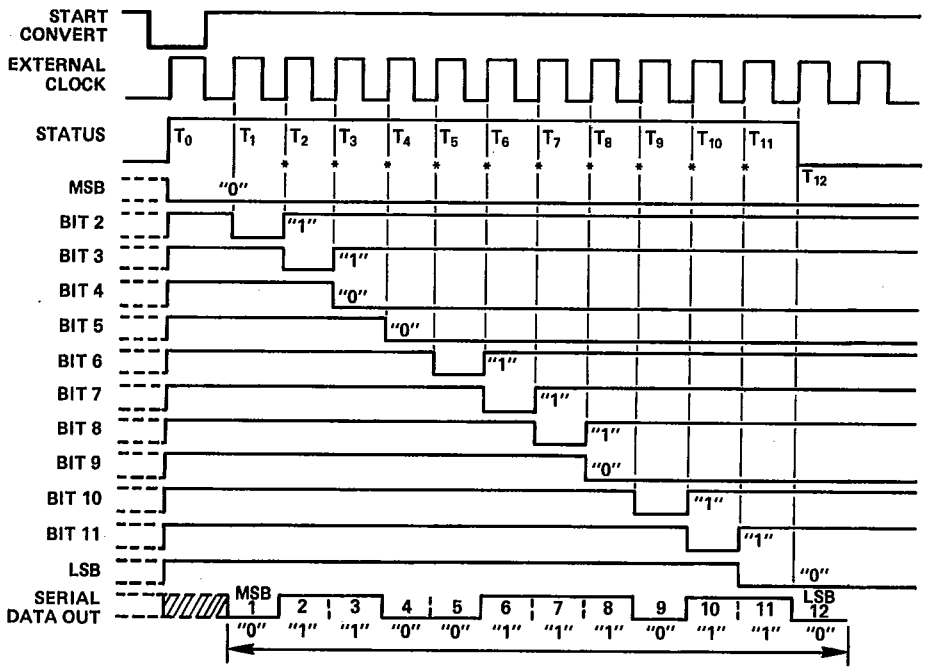


Figure 1. Timing Diagram