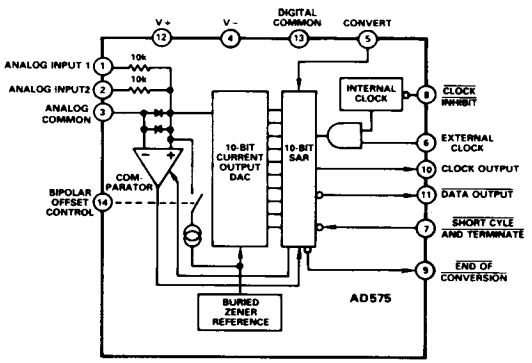
Complete 10-Bit A/D Converter with Serial Output

AD575*

FEATURES

Complete Serial Output 10-Bit A/D Converter with Reference, Clock and Comparator
30μs Conversion
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies
Low Cost Monolithic Construction
Internal or External Clock
Triggered or Continuous Conversions
Short Cycle Capability

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD575 is a complete 10-bit successive-approximation analog-to-digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and serial interface on a single chip. No additional components are required to perform a full-accuracy 10-bit conversion in 30μs.

The AD575 incorporates the most advanced integrated circuit design and processing technology available. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the SiCr thin-film resistor ladder network at the wafer stage insures high accuracy, which is maintained with a temperature-compensated sub-surface zener reference.

Operating on supplies of +5V and −12V to −15V, the AD575 will accept full scale analog inputs of 0V to +10V, 0V to +20V, −5V to +5V or −10V to +10V. The rising edge of a positive pulse on the CONVERT line initiates the conversion cycle. Eleven pulses will appear at the CLOCK OUTPUT pin with data valid on the falling edges of the clock waveform. The data is presented serially beginning with the MSB which is valid on the falling edge of the second clock pulse. The part may be programmed to perform 8-bit conversions or short cycled to 2-, 4-, 6- or 8-bit word lengths. $\overline{EOC}$ indicates that conversion is complete. The AD575 may be synchronized to an external clock if desired.

The AD575 is available in two versions for the 0 to +70°C temperature range, the AD575J and AD575K; packaging is a 14-pin plstic DIP.

PRODUCT HIGHLIGHTS

1. The AD575 is a complete 10-bit A/D converter. No external active components or control signals are required to perform a conversion.
2. The serial output of the AD575 allows a wide range of microprocessor interfacing and data transmission possibilities.
3. The device offers true 10-bit relative accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD575 adapts to unipolar or bipolar analog inputs by grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.
6. The AD575 can be synchronized to an external clock.
7. Conversions can be initiated externally or internally.
8. The AD575 can be short-cycled to 8 bits by pin programming.
9. The Short Cycle and Terminate feature allows the user to program conversions of 2, 4, 6 or 8 bits.

AD575—SPECIFICATIONS (@ +25°C, V+ = +5V, V− = −12V or −15V, unless otherwise noted.)

	AD575J			AD575K			
	Min	Typ	Max	Min	Typ	Max	Units
RESOLUTION							
For Which No Missing Codes							
is Guaranteed	10			10			Bits
T_{min} to T_{max}	9			10			Bits
UNIPOLAR OFFSET			±2			±1	LSB
T_{min} to T_{max}			±2			±1	LSB
BIPOLAR ZERO			±2			±1	LSB
T_{min} to T_{max}			±2			±1	LSB
GAIN ERROR[1]		±2				±2	LSB
GAIN DRIFT[2]							
T_{min} to +25°C			±2			±1	LSB
+25°C to T_{max}			±4			±2	LSB
RELATIVE ACCURACY[3]			±1			±1/2	LSB
T_{min} to T_{max}			±1			±1/2	LSB
POWER SUPPLY REJECTION[4]							
Positive Supply:							
+4.5V≤V+≤+5.5V			±2			±1	LSB
Negative Supply:							
−15.75V≤V−≤−14.25V			±2			±1	LSB
−12.6V≤V−≤−11.4V			±2			±1	LSB
ANALOG INPUT IMPEDANCE							
Pin 1, Pin 2	6	10	14	6	10	14	kΩ
ANALOG INPUT RANGES							
Unipolar	0 to 10			0 to 10			V
	0 to 20			0 to 20			V
Bipolar	−5 to +5			−5 to +5			V
	−10 to +10			−10 to +10			V
OUTPUT CODING							
Unipolar	NEGATIVE TRUE BINARY			NEGATIVE TRUE BINARY			
Bipolar	NEGATIVE TRUE OFFSET BINARY			NEGATIVE TRUE OFFSET BINARY			
LOGIC OUTPUTS (T_{min} to T_{max})							
V_{OL} @ I_{SINK} = 3.2mA	0		0.4	0		0.4	V
V_{OH} @ I_{SOURCE} = 0.5mA	2.4		5.0	2.4		5.0	V
LOGIC INPUTS (T_{min} to T_{max})							
I_{INH} @ V_{IN} = 5V[5]			+50			+50	μA
I_{INL} @ V_{IN} = 0V[5]	−800			−800			μA
V_{INH}	2.0		5.5	2.0		5.5	V
V_{INL}	0		0.8	0		0.8	V
CONVERSION TIME (T_{min} to T_{max})							
Internal Clock	10	20	30	10	20	30	μs
External Clock	25			25			μs
POWER SUPPLY							
V+	+4.5		+5.5	+4.5		+5.5	V
V−	−11.4		−15.75	−11.4		−15.75	V
OPERATING CURRENT							
V+		15	25		15	25	mA
V−		9	15		9	15	mA

NOTES

[1]Gain Error is specified with a 15Ω resistor in series with the 10V input (Pins 1 and 2 tied together) or a 30Ω resistor in series with the 20V input (Pin 1 with Pin 2 tied to analog common). Gain Error is guaranteed trimmable to zero (see text).

[2]The gain drift is calculated from gain measurements at the extremes of the temperature range under consideration.

[3]Relative Accuracy, also referred to as Integral Linearity, is defined as the deviation of the code transition points from the ideal transfer points on a straight line from zero to full-scale. It is also a measure of the error which remains when offset and full scale errors are trimmed to zero in an application.

[4]Measured at full scale.

[5]These specifications apply to the CONV, XCL, and $\overline{SCAT}$ inputs. $\overline{CLI}$ is hardwired to DGND or $+V_S$ in most applications. Typically I_{INH} = +350μA and I_{INL} = 120μA for the $\overline{CLI}$ input.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common . . . . . 0 to +7V
V− to Digital Common . . . . . 0 to −16.5V
Analog Common to Digital Common . . . . . ±1V
Analog Inputs . . . . . (V−) −0.3V to +22V
Control Inputs . . . . . 0 to V+
Power Dissipation 800mW

NOTE
All pins must be kept more positive than (V−) −0.3V.

ORDERING GUIDE

Model	Package Option*	Temperature Range −°C	Relative Accuracy
AD575JN	N-14	0 to +70	±1LSB max
AD575KN	N-14	0 to +70	±1/2LSB max

*N = Plastic DIP. For outline information see Package Information section.

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FUNCTIONAL DESCRIPTION

A block diagram of the AD575 is shown in Figure 1. A conversion is initiated by a positive pulse on the CONVERT line. $\overline{EOC}$ goes high within 150ns indicating that a conversion has started. The internal 10-bit current-output DAC is sequenced by the successive approximation register (SAR) from most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 10kΩ input resistor(s). The comparator determines whether the addition of each successively-weighted bit current causes the DAC current to be higher or lower than the input current. If the sum is less the bit is left on ($\overline{DO}$ set low). If the sum is more, the bit is turned off ($\overline{DO}$ set high). The result of each bit decision is passed to $\overline{DO}$ on the rising edge of CO.

After all bits have been tested, the DAC output current will match the input signal current to within 0.05% (1/2LSB). $\overline{EOC}$ returns low after the final bit decision to indicate that the AD575 has been reset and is ready to perform a new conversion. The output data stream can be synchronized to an external clock using the XCL input and short cycled to any desired word length using the $\overline{SCAT}$ line.

The AD575 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is to connect the power supplies (+5V and −12V or −15V), and the analog input. The pinout is shown in Figure 2.

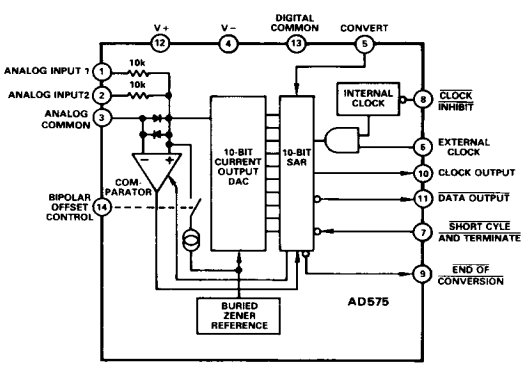

Figure 1. AD575 Functional Block Diagram

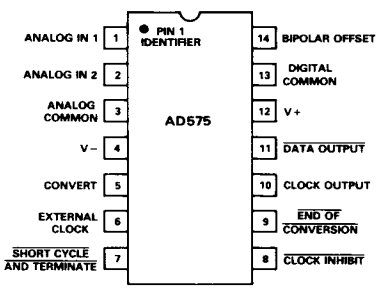

Figure 2. AD575 Pin Connections

ANALOG INPUT CONNECTIONS

The AD575 can be configured for unipolar or bipolar operation on 10V span or 20V span input signals. The appropriate input range is selected by connecting pins 2 and 14 according to the table of Figure 3.

The AD575's low offset and gain errors (shown in the Specifications) are adequate for most applications. For these cases, a fixed gain resistor (R2 in Figure 3) is the only external component, in addition to any power supply decoupling that may be required. Pins 3 and 13 should be connected directly together.

Figure 3 shows a trimming circuit that can be used to adjust the offset to zero, using the appropriate value of the R1 potentiometer as shown in the table. If gain trim is required, R2 should also be replaced by the appropriate potentiometer as shown in the table.

ANALOG INPUT RANGE	CONNECTIONS PIN 2	PIN 14	COMPONENTS R1 (OFFSET)	R2 (GAIN)
0V TO +10V	PIN 1	PIN 13	10Ω	15Ω FIXED OR 50Ω POT
0V TO +20V	PIN 3	PIN 13	20Ω	30Ω FIXED OR 100Ω POT
−5V TO +5V	PIN 1	OPEN	10Ω	15Ω FIXED OR 50Ω POT
−10V TO +10V	PIN 3	OPEN	20Ω	30Ω FIXED OR 100Ω POT

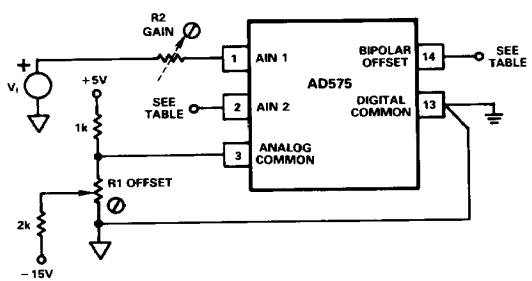

Figure 3. AD575 Input Circuit Showing Offset and Gain Adjustment

UNIPOLAR MODE OPERATION

In unipolar mode, the nominal location of the low side transition of the first code (1111111110) occurs at an input voltage of +1LSB (10mV for the 10V span, 20mV for the 20V span). The offset error of the AD575 can be trimmed out, if required, by applying an input voltage of +1LSB to the analog input and adjusting R1 until the low side transition of the first code occurs.

If the Gain Error needs to be trimmed, the gain resistor should be replaced with a potentiometer according to Figure 3. The nominal location of the low side transition of the full scale code (0000000000) in unipolar mode is full scale minus 1LSB (9.99V for 10V span, 19.98V for 20V span). Once the offset has been adjusted, the full scale range can be set by adjusting the gain potentiometer.

BIPOLAR CONNECTION

If the bipolar offset control (pin 14) is left open, the AD575 will accept bipolar input voltages with 0V as the nominal bipolar zero point. The input voltage corresponding to the low side transition of the mid-scale code (0111111111) is −1/2LSB (−5mV for 10V spans and −10mV for 20V spans). The nominal location of the code transitions are therefore offset by 1/2LSB as shown in Figure 4. This offset may be adjusted using the trim scheme shown in Figure 3 with a 1.2kΩ resistor in place of the 1kΩ resistor shown.

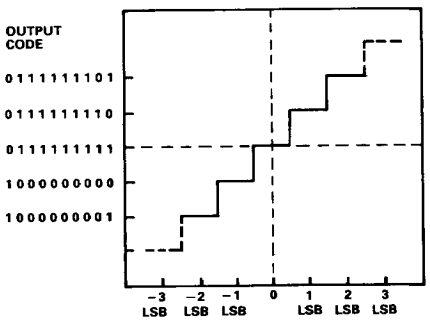

Figure 4. AD575 Transfer Characteristic (Bipolar Operation)

The gain error should be adjusted after any offset adjustment. An input voltage of full scale minus 1 1/2LSBs is applied (4.985V for −5V to +5V range, 9.971V for −10V to +10V range) and R2 is adjusted until the low-side transition of the full scale code (0000000000) occurs.

The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 5.

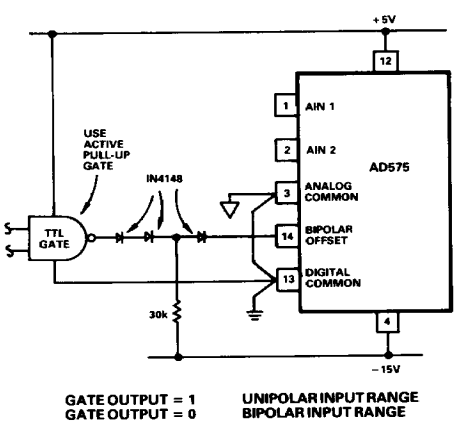

Figure 5. Bipolar Offset Controlled by Logic Gate

CONTROL AND TIMING OF THE AD575

The AD575 has a flexible control architecture which supports several operating modes. It can provide its own clock or it can be synchronized to an external clock. Conversions can be initiated externally, or the part can perform continuous conversions yielding a stream of output data. In addition, the AD575 can be short-cycled to any of several convenient data word lengths to tailor the output to the specific input requirements of the system. Figure 6 shows the control logic diagram of the AD575. The four inputs which control the operation of the AD575 are CONV (convert), $\overline{CLI}$ (clock inhibit), XCL (external clock), and $\overline{SCAT}$ (short cycle and terminate). Three outputs are provided: $\overline{DO}$ (Data Out), CO (Clock Out), and $\overline{EOC}$ (End of Conversion).

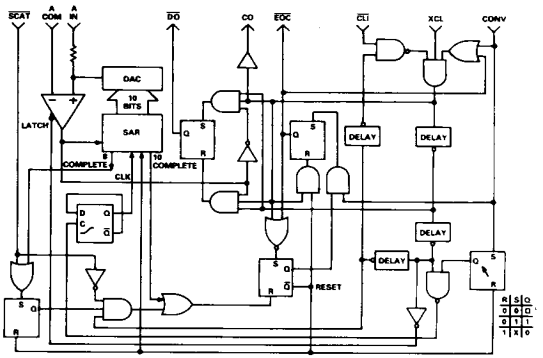

Figure 6. AD575 Control Logic Diagram

EXTERNALLY INITIATED CONVERSIONS

Figure 7 is the timing diagram which illustrates the operation of the AD575 with an externally applied convert signal. Conversions are initiated by a positive-going pulse applied to the CONV (convert) input. This pulse should be at least 250ns wide and should return low before $\overline{EOC}$ returns low to prevent the initiation of a second conversion. If the internal clock is used, the clock will start on the rising edge of the convert start pulse. If an external clock is used, the falling edge of the clock must occur no earlier than 900ns following the rising edge of the convert command.

INTERNAL CLOCK MODE

The AD575 can be configured for internal clock operation by tying $\overline{CLI}$ and XCL to +5V. CO (clock output) provides the necessary synchronizing information in this mode. Data is transferred to $\overline{DO}$ on the rising clock edge and is stable on the falling edge. The duty cycle of the CO waveform in this mode will be in the range of 30% to 70%.

EXTERNAL CLOCK MODE

When $\overline{CLI}$ is connected to digital common, an external clock can be applied to XCL. The external clock should have a maximum frequency of 450kHz with a minimum of 900ns in the high or low phase. Arbitrarily slow clocks may be used as long as these minimum high and low periods are observed. Conversion time will increase as clock frequency decreases. Each data bit will be stable within 150ns of the rising edge of the associated external clock pulse and will remain stable until the rising edge of the subsequent clock pulse. Data is guaranteed to be stable on the falling edge of the clock pulse.

The state of the $\overline{DO}$ output during the first clock period is undefined but it is stable until the rising edge of the second clock period. The MSB appears at $\overline{DO}$ during the second clock period. The subsequent data bits are then clocked out until the N^{th} bit or LSB is clocked out on the $(N+1)^{th}$ clock pulse. $\overline{EOC}$ returns low within 150ns of the rising edge of this final clock pulse. In internal clock mode, the output clock pulse associated with the LSB is shorter than the others but the LSB is guaranteed to be stable on the falling edge of this pulse. The LSB will remain stable until a new conversion is initiated. The value of N will be 10 unless the conversion has been short cycled (see "short cycle and terminate" text).

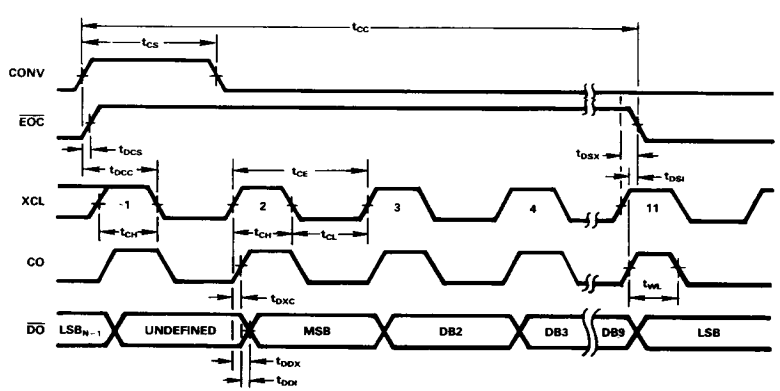

Figure 7. Externally Initiated Conversions

CONTINUOUS CONVERSIONS

Figure 8 is the timing diagram associated with the continuous conversion mode of operation. If CONV is high when $\overline{EOC}$ goes low, another conversion will begin immediately. $\overline{EOC}$ will be set (high) following the falling edge of the $(N+1)^{st}$ CO pulse and conversion commences with the rising edge of the next CO pulse. The $(N+1)^{st}$ CO pulse is not shortened in this mode. If CONVERT is held high the AD575 will put out a continuous stream of conversions, punctuated by $\overline{EOC}$ which will mark the last clock pulse of a conversion. $\overline{EOC}$ will remain low until the falling edge of CO, the output clock, in this mode. Therefore, the rising edge of $\overline{EOC}$ may be used to signal that conversion is complete and that data is transferred. This sequence is useful for initiating parallel dumps from a serially loaded shift register.

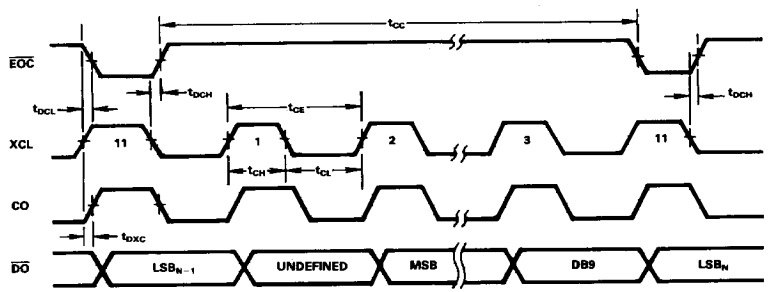

Figure 8. Continuous Conversion Mode (CONV. Held High)

SHORT CYCLE AND TERMINATE

For normal 10-bit operation, the Short Cycle and Terminate ($\overline{SCAT}$) line should be tied high. If 8-bit conversions are required, $\overline{SCAT}$ should be tied low. In this mode, $\overline{EOC}$ will go low after the rising edge of the ninth clock pulse to indicate that the eighth and final data bit is valid. This mode is useful when parallel loads to 8-bit data buses are desired since it avoids the complication of suppressing the 9th and 10th data bits.

Conversions of 2, 4, 6 or 8 bits can be performed by pulling $\overline{SCAT}$ low during the negative clock phase prior to the positive clock associated with the desired LSB. Figure 9 illustrates the timing associated with this mode of operation. For example, to terminate the conversion after six data bits, $\overline{SCAT}$ should be driven low during the negative clock phase following the sixth clock pulse. $\overline{EOC}$ will then go low following the rising edge of the seventh clock pulse to indicate that the sixth and final data bit is valid.

This terminate feature can also be used to program conversions of 1, 3, 5, 7 or 9 bits. However, the conversion immediately following a conversion of an odd number of data bits will be spurious. All subsequent conversions will be normal until the conversion following another odd data word length conversion.

The negative edge of the $\overline{SCAT}$ signal should always occur during the negative phase of a clock cycle and it should be held low for a minimum of 900ns. $\overline{SCAT}$ may be held low into the next conversion but it must be restored high at least one clock cycle prior to being used to terminate a conversion. If $\overline{SCAT}$ is not restored high prior to the eighth clock pulse, $\overline{EOC}$ will go low and an 8-bit short cycle will occur. Care should be taken not to pulse $\overline{SCAT}$ from high to low between conversions (when $\overline{EOC}$ is low). This would initiate a terminate sequence which will execute on the rising edge of the first clock pulse following the next Convert command.

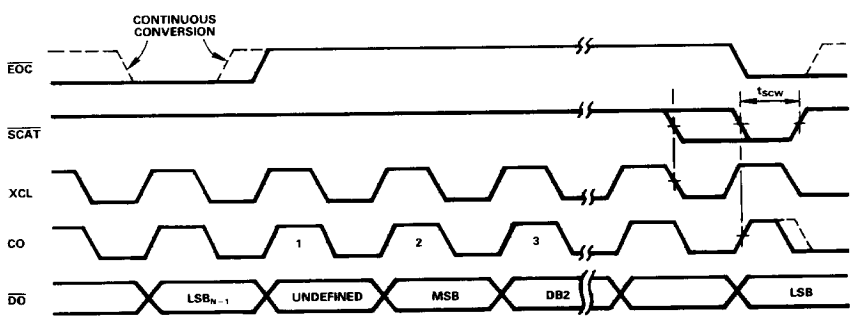

Figure 9. Short Cycle and Terminate Operation

Parameter	Symbol	Min	Typ	Max	Units
EXTERNALLY-INITIATED CONVERSIONS					
Convert Pulse Width	t_{CS}	300			ns
Convert to $\overline{EOC}$ Delay	t_{DCS}			150	ns
CO LSB Clock Pulse Width	t_{WL}	400			ns
XCL to $\overline{EOC}$ Reset	t_{DSX}	50		150	ns
↑ CO to ↓ $\overline{EOC}$ Reset Delay	t_{DSI}	20		150	ns
CONTINUOUS CONVERSIONS					
↑ XCL to ↓ $\overline{EOC}$ Reset Delay	t_{DCL}	50		150	ns
↓ XCL to ↑ $\overline{EOC}$ Delay	t_{DCH}	50		1000	ns
INTERNAL CLOCK TIMING					
Conversion Time	t_{CC}	10	20	30	µs
CO to $\overline{DO}$ Output Delay	t_{DDI}	−100		+100	ns
EXTERNAL CLOCK TIMING					
Conversion Time	t_{CC}	25			µs
↑ XCL to $\overline{DO}$ Output	t_{DDX}	30		150	ns
XCL to CO Output	t_{DXC}	30		160	ns
↑ Convert to ↓ XCL Set-Up Time	t_{DOC}	900			ns
XCL Period	t_{CE}	2.2			µs
XCL High	t_{CH}	900			ns
XCL Low	t_{CL}	900			ns
SHORT CYCLE TIMING					
$\overline{SCAT}$ Pulse Width	t_{SCW}	900			ns

Table I. AD575 Timing Specifications

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD575

Many data acquisition systems for digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A/D converter. A SHA can be used to accurately define the exact point in time at which the signal is sampled. A SHA can also serve as a high input-impedance buffer for the AD575.

Figure 10 shows the AD575 connected to the AD585 monolithic SHA. In this configuration, the AD585 will acquire a 10V signal in less than 2µs and droop less than 1mV/ms using the on-chip hold capacitor.

$\overline{EOC}$ goes high after the conversion is initiated to indicate that a conversion is underway. In Figure 10 it is also used to put the AD585 into the hold mode while the AD575 begins its conversion cycle. (The AD585 output settles to final value well in advance of the first comparator decision within the AD575.) $\overline{EOC}$ goes low when the conversion is complete placing the AD585 back in the sample mode.

Configured as shown in Figure 10, the next conversion can be initiated after a 2µs delay to allow for signal acquisition by the AD585.

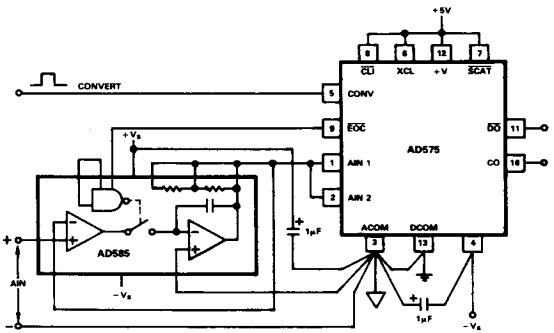

Figure 10. AD575 to AD585 Sample and Hold Interface

SUPPLY DECOUPLING AND LAYOUT

For proper operation, the AD575's power supplies should be free from high-frequency noise. The stability of the transfer function is especially sensitive to noise on the V− supply. Noise on the V+ supply can also propagate to the digital outputs.

If decoupling is required, tantalum capacitors are suggested. Best results will be obtained if the capacitors are connected directly to the appropriate pins of the AD575. Decoupling capacitors for V− should be connected between pin 4 and Analog Common (pin 3). Decoupling capacitors for V+ should be connected between pin 12 and Digital Common (pin 13).

Good circuit layout practice suggests that the AD575 and its associated analog input circuitry be kept separate from system logic circuitry to avoid unwanted interactions.

GROUNDING CONSIDERATIONS

The AD575 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common-mode voltage between the two commons. The absolute maximum voltage rating between the two commons is ±1V. A parallel pair of back-to-back protection diodes should be connected between the commons if they are not connected locally.

In normal operation, the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

AD575 TO 8085 INTERFACE

The 8085 has both serial output (SOD) and serial input (SID) capability. A simple 3 hardware line interface can be constructed between the AD575 and 8085. These leads can be opto-coupled in order to establish galvanic isolation between the two devices as shown in Figure 11.

The software routine in Table II will read a complete 10-bit data word from the AD575 in 180μs (3MHz 8085). The software generates the clock for the AD575 in order to synchronize the data output with the 8085 serial read operation.

The DATA procedure loads appropriate constants into the 8085 registers and initiates the conversion. The CONV procedure assumes that the AD575 clock was in the high state when the CONVERT pulse was generated (upon completion, this sample routine leaves the SOD line in the appropriate state to insure this). A low clock pulse is generated, and the data bit is read into the MSB of the accumulator. The data bit is then shifted into the LSB of the temporary register (L), the clock is set high, and the procedure is repeated.

After the loop has executed three times, a logical AND is performed to set the first bit (the undefined bit) to zero, and the result is placed into the high byte (H) register. The loop counter is then reset, and the CONV procedure is executed 8 more times. Upon completion of the sample routine, 10 bits of right-justified data will reside in the HL register pair.

Note that the opto-isolators invert the clock and data lines. If these are not used (no inversion present), the constants in the D and E registers should be swapped, a CMA instruction should be inserted after the RIM instruction, and an inverter should be connected between the address decoder and the CONVERT pin. Also, the results of the first pass through the routine should be ignored following power up and reset cycles to insure that the AD575 has been reset.

LABEL	MNEMONIC	OPERAND	COMMENT
DATA	MVI	B,03	Set inner loop counter to 3
	MVI	C,02	Set outer loop counter to 2
	MVI	D,CO	Setup register D for clock low
	MVI	E,40	Setup register E for clock high
	MVI	H,10	AD575 address location
	MVI	L,00	Clear temp register
	MOV	M,B	Generate CONVERT pulse
CONV	MOV	A,D	Setup ACC for clock low
	SIM		Output clock low
	RIM		Read AD575 data bit into ACC
	RAL		Shift data bit into Carry
	MOV	A,L	Move temp to ACC
	RAL		Shift data bit from Carry to ACC
	MOV	L,A	Replace temp
	MOV	A,E	Setup ACC for clock high
	SIM		Output clock high
	DCR	B	Decrement inner loop counter
	JNZ	CONV	Repeat CONV until done
	DCR	C	Decrement outer loop counter
	JZ	DONE	Skip to DONE on 2nd pass
	MOV	A,L	Move temp to ACC
	ANI	03	Mask undefined bit
	MOV	H,A	Store temp in H register
	MVI	B,OB	Set inner loop counter to 8
	JMP	CONV	Repeat CONV for 8 LSBs
DONE	RET		10 bits of right-justified data now reside in HL; return

Table II. Sample Assembly Code for AD575 to 8085 Isolated Interface

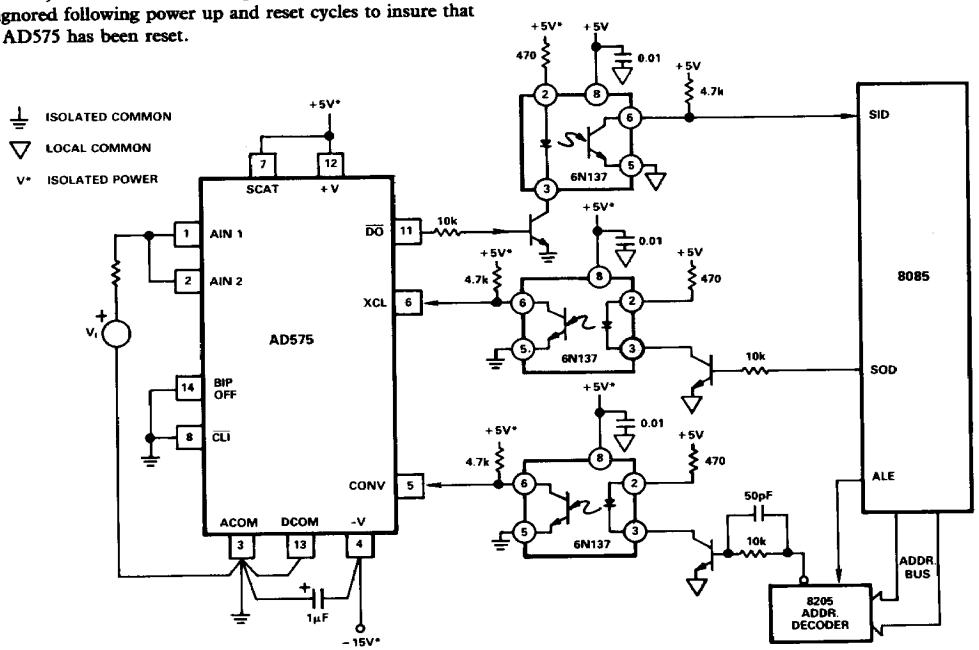

Figure 11. AD575 to 8085 Isolated Interface