ANALOG DEVICES

Very Fast, Complete 12-Bit A/D Converter

AD578

T-51-10-12

1.1 Scope.

This specification covers the detail requirements for a hybrid, very fast, 12-bit successive approximation analog-to-digital converter including internal clock reference and comparator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD578SD/883B
−2	AD578TD/883B
−3	AD578ZSD/883B
−4	AD578ZTD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32B.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage	±18V
Logic Supply Voltage	+7V
Analog Inputs (Pins 27 & 28)	±25V
Digital Inputs	+5.5V
Junction Temperature	+175°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10secs)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 8°C/W

θ_{JA} = 38°C/W

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Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition[1]	Units
Analog Input Voltage Ranges	V_{IN}	−1,2,3,4	±5, ±10 0 to +10 0 to +20					V
Input Impedance 0 to +10V, ±5V ±10V, 0 to +20V	R_{IN}	−1,2,3,4	5 10					kΩ typ
Gain Error	V_{GE}	−1,2,3,4	0.25	0.25			10V Unipolar 20V Bipolar	±%/FSR max
Gain Drift	V_{GD}	−1,3 −2,4	50		50 30		10V Unipolar 20V Bipolar 10V Unipolar 20V Bipolar	±ppm/°C max
Unipolar Offset Error	V_{OSE}	−1,2,3,4	0.25	0.25			10V Unipolar	±%/FSR max
Unipolar Offset Drift	V_{OSD}	−1,3 −2,4	15		15 10		10V Unipolar	±ppm/°C max
Bipolar Offset Error	V_{OSE}	−1,2,3,4	0.25	0.25			20V Bipolar	±%/FSR max
Bipolar Offset Drift	V_{OSD}	−1,3 −2,4	25		25 20		20V Bipolar	±ppm/°C max
Linearity Error	RA	−1,2,3,4	1/2	1/2	3/4		10V Unipolar 20V Bipolar	±LSB max
Differential Linearity Error[2]	DNL	−1,2,3,4	1	1	1		10V Unipolar 20V Bipolar	±LSB max
Reference Voltage Error	V_{REF}	−1,2,3,4	100	100				±mV max
Reference Voltage Drift	V_{REFD}	−1,2,3,4	20		20			±ppm/°C max
+5V Power Supply Sensitivity	PSRR	−1,2,3,4	0.005	0.005			+5V/±5%	±%/% ΔV_S max
±15V Power Supply Sensitivity	PSRR	−1,2	0.005	0.005			±15V/±10%	±%/% ΔV_S max
±12V Power Supply Sensitivity	PSRR	−3,4	0.007	0.007			±12V/±5%	±%/% ΔV_S max
Digital Output High Drive	V_{OH}	−1,2,3,4	2.4	2.4			@ −80μA	V min
Digital Output Low Drive	V_{OL}	−1,2,3,4	0.4	0.4			@ 3.2mA	V max
Conversion Speed	t_C	−1,3 −2,4	6 4.5			6 4.5		μs max
+5V Supply Drain	$+I_{DD}$	−1,2,3,4	150	150			All Bits On	mA max
+15V Supply Drain	$+I_{CC}$	−1,2,3,4	8	8			All Bits On	mA max
−15V Supply Drain	$-I_{CC}$	−1,2,3,4	35	35			All Bits On	mA max
Power Supply Range	$+V_{DD}$ $+V_{CC}$ $+V_{CC}$	−1,2,3,4 −1,2 −3,4	+5 ±15 ±12				±5% ±10% ±5%	V

NOTES
[1] V_{CC} = ±15V, (±12V for Z Model), V_{DD} = +5V, T_A = +25°C unless otherwise noted.
[2] Guaranteed No Missing Codes −55°C to +125°C.

Table 1.

REV. A

3.2.1 Functional Block Diagram and Terminal Assignments.

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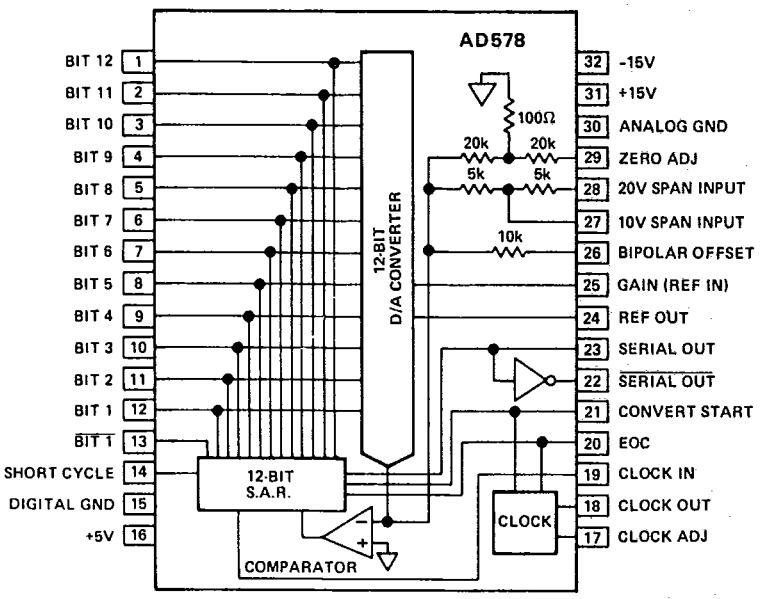
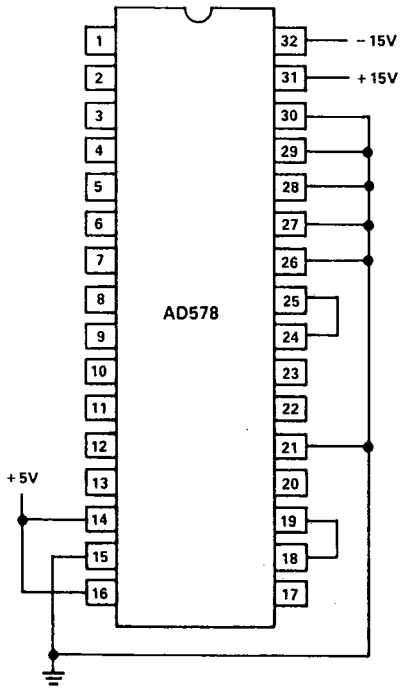


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



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5.0 Gain and Offset Adjustment.

The gain and offset adjustment circuits are shown in Figure 1 for unipolar or Figure 2 for bipolar operation. If the offset and gain specifications are sufficient, the 100Ω trimmers may be replaced by a 50Ω ±1% fixed resistor.

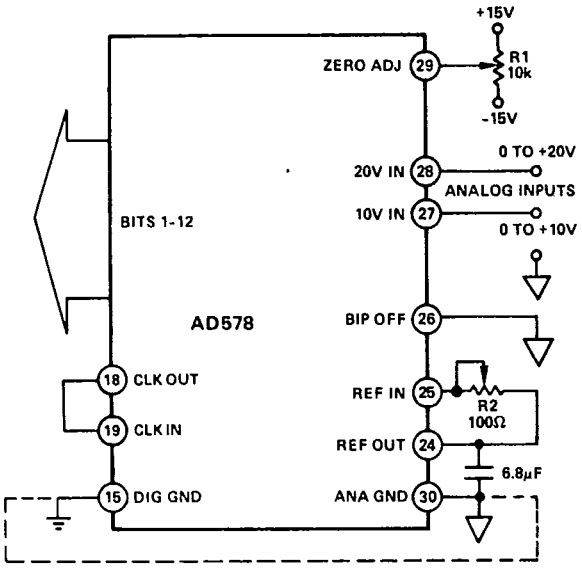

Figure 1. Unipolar Input Connections

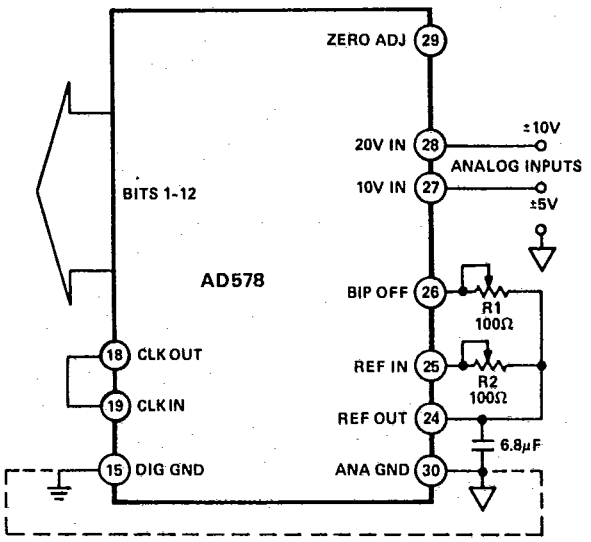

Figure 2. Bipolar Input Connections

5.1 Digital Output Data.

The digital output codes corresponding to analog input voltages are shown in Table 2.

Analog Input – Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	0 to +20V Range	−5V to +5V Range	−10V to +10V Range	B1 (MSB) B12 (LSB)
+9.9976	+19.9951	+4.9976	+9.9951	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+19.9902	+4.9952	+9.9902	1 1 1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0024	+10.0049	+0.0024	+0.0049	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0024	+0.0049	−4.9976	−9.9951	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	−5.0000	−10.0000	0 0 0 0 0 0 0 0 0 0 0 0

Table 2. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

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5.2 Clock Rate Control Alternate Connections.

The internal clock is preset to a nominal conversion time of 5.6μs. It can be adjusted for either faster or slower conversions. For faster conversion connect the appropriate 1% resistor between pin 17 and pin 18 and short pin 18 to pin 19.

For slower conversions connect a capacitor between pin 15 and pin 17.

The curves in Figure 3 characterize the conversion time for a given resistor or capacitor connection.

Note: 12-bit operation with no missing codes is not guaranteed when operating in this mode if a particular grade's conversion speed specification has been exceeded.

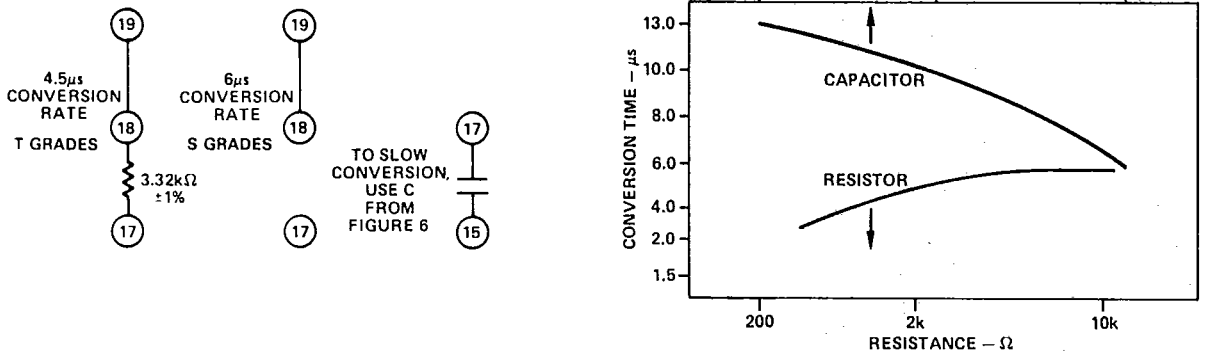

Figure 3. Conversion Time vs. R or C Values

5.2.1 External Clock.

An external clock may be connected directly to the clock input, pin 19. When operating in this mode, the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle. A positive going pulse width of 100 to 200 nanoseconds will provide a continuous string of conversions that start on the first rising edge of the external clock after the EOC output has gone low.

5.2.2 Short Cycle Input.

A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 4 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 12-bit resolution. Short cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times are summarized in Table 3.

Resolution (Bits)	12	10	8
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μs)	4.5	3.75	3

Table 3. Short Cycle Connections

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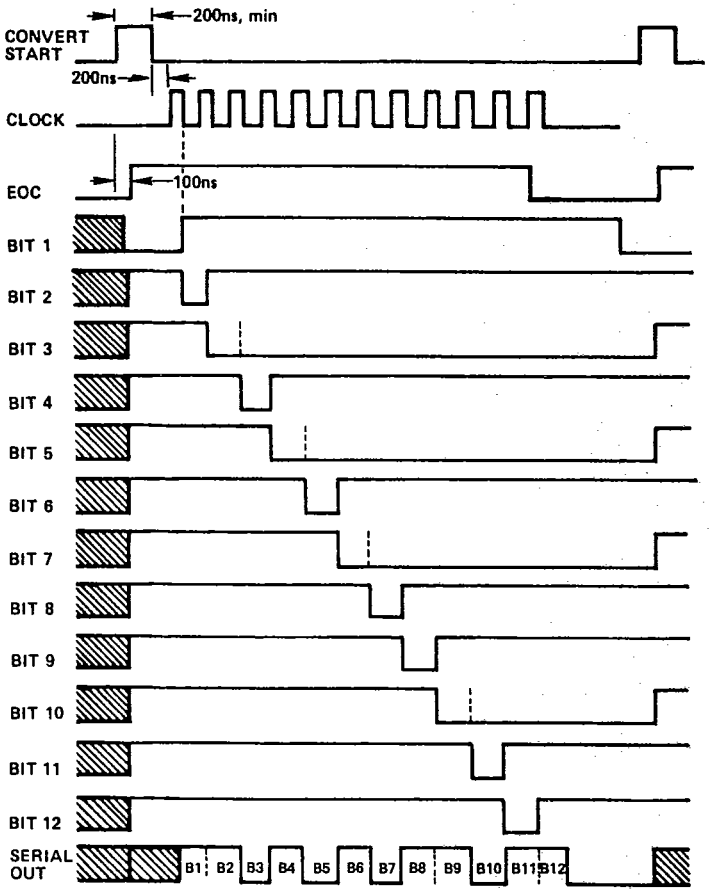

CLOCK
INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH MINIMUM PERIOD, T_{MIN} OF 100ns.

NOTE
[1]THE RISING EDGE OF CONVERT START PULSE RESETS THE MSB TO ZERO, AND THE LSBs TO ONE. THE TRAILING EDGE INITIATES CONVERSION.

Figure 4. AD578 4.5μs Timing Diagram