ANALOG DEVICES

Very Fast, Complete 10-Bit A/D Converter

T-51-10-10 **AD579**

3

FEATURES

Performance

- Complete 10-Bit A/D Converter with Reference and Clock
- Fast Successive Approximation Conversion: 1.8μs
- Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±40ppm/°C max
- Max Nonlinearity: <±0.048%
- Low Power: 775mW
- MIL-STD-883B Processing Available

Versatility

- Positive-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- Precision +10V Reference for External Applications
- Adjustable Internal Clock
- "Z" Models for ±12V Supplies

PRODUCT DESCRIPTION

The AD579 is a high speed low cost 10-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 10-bit monolithic DAC to provide superior performance and versatility with IC size, price and reliability.

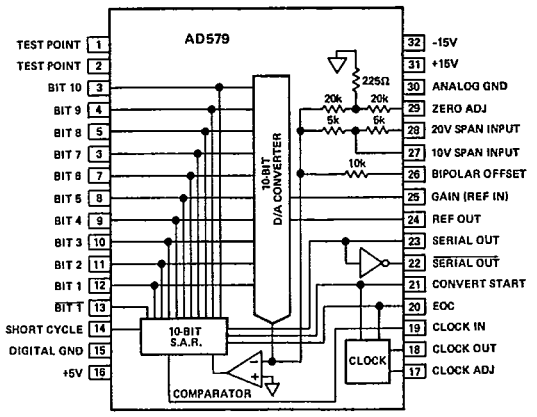
Important performance characteristics of the AD579 include a maximum linearity error at +25°C of ±0.048%, maximum gain temperature coefficient of ±40ppm/°C, typical power dissipation of 775mW and maximum conversion time of 1.8μs.

The fast conversion speeds of 1.8μs (K and T grades) and 2.2μs (J grade) make the AD579 an excellent choice in a variety of applications where system throughput rates from 454kHz to 555kHz are required. In addition, it may be short cycled to obtain faster conversion speeds at lower resolutions.

The design of the AD579 includes scaling resistors that provide analog input signal ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Adding flexibility and value is the +10V precision reference which can be used for external applications.

The AD579 is available with solder-seal (D) for harsh or rigorous surroundings and is contained in a 32-pin side-brazed, ceramic DIP.

AD579 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

PRODUCT HIGHLIGHTS

1. The AD579 is a complete 10-bit A/D converter. No external components are required to perform a conversion.
2. The fast conversion rate of the AD579 makes it an excellent choice for high speed data acquisition on systems requiring high throughput rate.
3. The internal buried Zener reference is laser trimmed to 10.00V ±0.1% and ±15ppm/°C typ T.C. The reference is available externally and can provide up to 1mA.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolutions.
6. The integrated package construction provides high quality and reliability with small size and weight.

AD579 ORDERING GUIDE

Model	Conversion Speed	Package	Temperature Range	Power Supply Range	Package Outline*
AD579JN	2.2μs	Hermetic-Seal	0 to +70°C	±15V ±10%	DH-32B
AD579KN	1.8μs	Hermetic-Seal	0 to +70°C	±15V ±10%	DH-32B
AD579TD	1.8μs	Hermetic-Seal	-55°C to +125°C	±15V ±10%	DH-32B
AD579ZJN	2.2μs	Hermetic-Seal	0 to +70°C	±12V ±5%	DH-32B
AD579ZKN	1.8μs	Hermetic-Seal	0 to +70°C	±12V ±5%	DH-32B
AD579ZTD	1.8μs	Hermetic-Seal	-55°C to +125°C	±12V ±5%	DH-32B
AD579TD/883B	1.8μs	Hermetic-Seal	-55°C to +125°C	±15V ±10%	DH-32B
AD579ZTD/883B	1.8μs	Hermetic-Seal	-55°C to +125°C	±12V ±5%	DH-32B

*See Section 14 for package outline information.

SPECIFICATIONS (typical @ +25°C; ±15V and +5V power supplies unless otherwise noted)

T-51-10-10

Model	AD579JN	AD579KN	AD579TD
RESOLUTION	10 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±5.0V, ±10V	*	*
Unipolar	0 to +10V, 0 to +20V	*	*
Input Impedance			
0 to +10V, ±5V	5kΩ (±20%)	*	*
±10V, 0 to +20V	10kΩ (±20%)	*	*
DIGITAL INPUTS			
Convert Command[1]	1LS TTL Load	*	*
Clock Input	1LS TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error[2,3]	±0.1% FSR (±0.25% FSR max)	*	*
Unipolar Offset[3]	±0.1% FSR (±0.25% FSR max)	*	*
Bipolar Offset[3,4]	±0.1% FSR (±0.25% FSR max)	*	*
Linearity Error			
+25°C	±1/2LSB max	*	*
T_{min} to T_{max}	±3/4LSB max	*	*
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)			
+25°C	10 Bits	*	*
T_{min} to T_{max}	10 Bits	*	*
POWER SUPPLY SENSITIVITY			
+15V ±10%	0.005%/%ΔV_S max	*	*
−15V ±10%	0.005%/%ΔV_S max	*	*
+5V ±10%	0.001%/%ΔV_S max	*	*
"Z" Versions			
+12V ±5%	0.007%/%ΔV_S max	*	*
−12V ±5%	0.007%/%ΔV_S max	*	*
TEMPERATURE COEFFICIENTS			
Gain	±25ppm/°C typ	*	*
	±40ppm/°C max	*	*
Unipolar Offset	±5ppm/°C typ	*	*
	±15ppm/°C max	*	*
Bipolar Offset	±8ppm/°C typ	*	*
	±20ppm/°C max	*	*
Differential Linearity	±2ppm/°C typ	*	*
CONVERSION TIME[5,6] (max)	2.2μs	1.8μs	**
Conversion Time T_{min} to T_{max}	2.4μs	2.0μs	**
PARALLEL OUTPUTS			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2LSTTL Loads	*	*
SERIAL OUTPUTS (NRZ FORMAT)			
Unipolar Code	Binary/Complementary Binary	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*
Output Drive	2LSTTL Loads	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*
Output Drive	8LSTTL Loads	*	*
INTERNAL CLOCK[7]			
Output Drive	2LSTTL Loads	*	*
INTERNAL REFERENCE			
Voltage	10.000 ±10mV typ	*	*
Temperature Coefficient	15ppm/°C	*	*
External Current	±1mA max	*	*
POWER SUPPLY REQUIREMENTS			
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.5	*	*
Supply Current +15V	3mA typ, 8mA max	*	*
−15V	22mA typ, 35mA max	*	*
+5V	100mA typ, 150mA max	*	*
Power Dissipation	775mW typ	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	−55°C to +125°C
Storage	−55°C to +150°C	*	*

NOTES
[1] Positive pulse 200ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.
[2] With 50Ω, 1% fixed resistor in place of gain adjust potentiometer.
[3] Adjustable to zero.
[4] With 50Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).
[5] Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.
[6] Each grade is specified at the conversion speed shown. See Figure 7 for appropriate connections.
[7] Externally adjustable by a resistor or capacitor.
[8] For "Z" models order AD579ZJN, AD579ZKN or AD579ZTD.
*Specifications same as AD579JN.
**Specifications same as AD579KN.
Specifications subject to change without notice.

THEORY OF OPERATION

The AD579 is a complete 10-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD579 is shown in Figure 1.

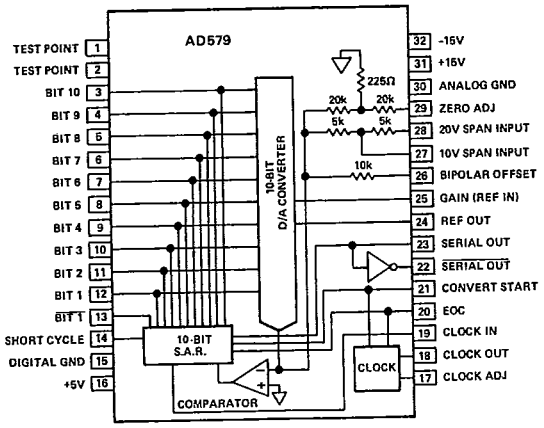


Figure 1. AD579 Functional Diagram and Pinout

On receipt of a CONVERT START command, the AD579 converts the voltage at its analog input into an equivalent bit binary number. This conversion is accomplished as follows: the 10-bit successive-approximation register (SAR) has its 10-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±0.1%; it is buffered and can supply up to 1.0mA to an external load in addition to the current required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

TIMING

The timing diagram is shown in Figure 2. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 10 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{10} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until Bit 10 (LSB) decision (keep) is made at t_{10}. After a 15ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to Logic "0" state.

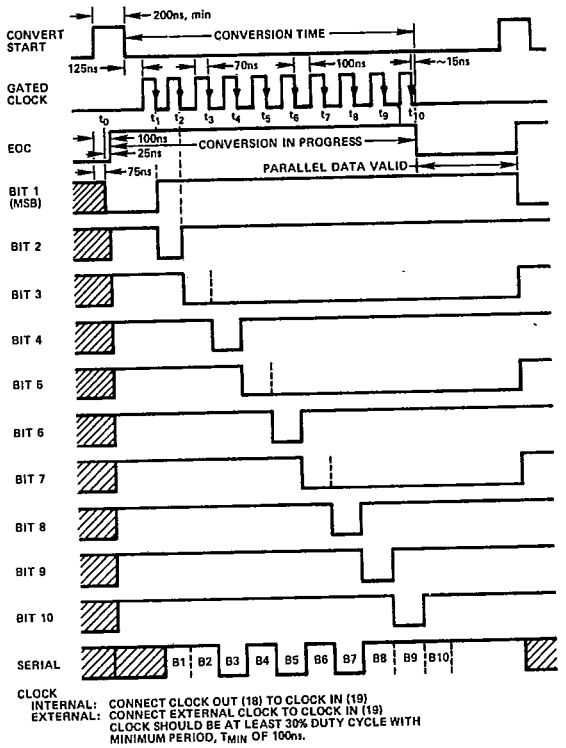


Figure 2. AD579 Timing Diagram

Serial data does not change and is guaranteed valid on negative-going clock edges, therefore; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 2).

Incorporation of this 15ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

3

UNIPOLAR CALIBRATION

The AD579 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 00 to 0000 0000 01) will occur for an input level of +1/2LSB (4.88mV for 10V range).

If pin 26 is connected to pin 30, the unit will behave in this manner, within specifications. Refer to Table I and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±50mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.985V for a 10V range). Trim R2 to give the last transition (1111 1111 10 to 1111 1111 11).

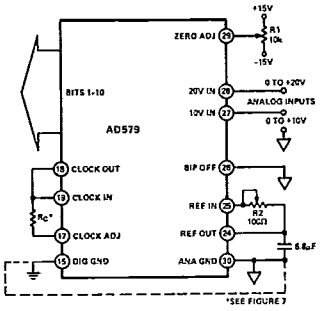


Figure 3. Unipolar Input Connections

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, the 100Ω trimmer shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2LSB above negative full scale (–4.9957V for the ±5V range) is applied, and R1 is trimmed to give the first transition (0000 0000 00 to 0000 0000 01). Then, a signel 1 1/2LSB below positive full scale (+4.9853V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 10 to 1111 1111 11).

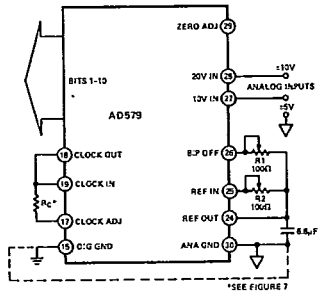


Figure 4. Bipolar Input Connections

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ERROR SOURCES

The analog continuum is partitioned into 2^{10} discrete ranges for 10-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection.

The matching and tracking errors in the AD579 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.1% FSR typical. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 3 and 4. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size (Figure 5).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can having missing codes; the AD579TD is specified as having no missing codes from -55°C to +125°C and thus is monotonic.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

Analog Input – Volts (Center of Quantization Interval)				Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10V Range	0 to +20V Range	-5V to +5V Range	-10V to +10V Range	B1 (MSB)	B10 (LSB)
+9.9902	+19.9804	+4.9902	+9.9804	1 1 1 1 1 1 1 1 1 1	
+9.9804	+19.9609	+4.9804	+9.9609	1 1 1 1 1 1 1 1 1 0	
•	•	•	•	•	
•	•	•	•	•	
+5.0097	+10.0195	+0.0097	+0.0195	1 0 0 0 0 0 0 0 0 1	
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0	
•	•	•	•	•	
•	•	•	•	•	
+0.0097	+0.0195	-4.9902	-9.9804	0 0 0 0 0 0 0 0 0 1	
+0.0000	+0.0000	-5.0000	-10.0000	0 0 0 0 0 0 0 0 0 0	

Table I. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

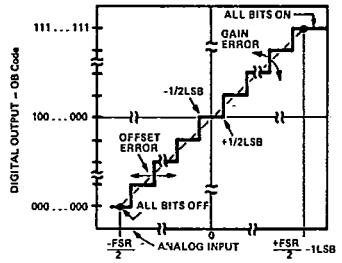

Figure 5. Transfer Characteristic for an Ideal Bipolar A/D

LAYOUT CONSIDERATIONS

Many data acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD579. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD579's supply terminals should be capacitively decoupled as close to the AD579 as possible. A large value capacitor such as 10μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

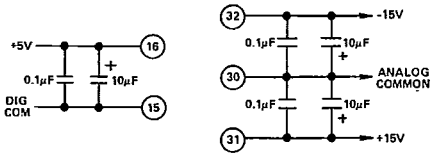

Figure 6. Basic Grounding Practice

To minimize noise the reference output (Pin 24) should be decoupled by a 6.8μF capacitor to pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 4.8μs. It can be adjusted for either faster or slower conversions. For faster conversion connect the appropriate 1% resistor between pin 17 and pin 18 and short pin 18 to pin 19.

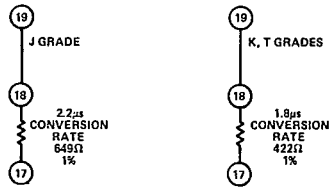

Figure 7. Clock Rate Control Connection

Short Cycle Input – A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 10-bit resolution. Short cycle pin connections and associated maximum 10- and 8-bit conversion times are summarized in Table II.

Resolution (Bits)	10	8
Connect Pin 14 to Pin	2	4
Conversion Speed (μs)	1.8	1.5

Table II. Short Cycle Connections

External Clock – An external clock may be connected directly to the clock input, pin 19. When operating in this mode the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle.

External Buffer Amplifier – In applications where the AD579 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the AD841 should be used.

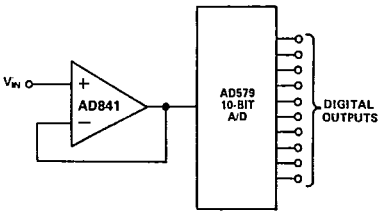

Figure 8. Input Buffer

SAMPLED DATA SYSTEMS

The conversion speed of the AD579 allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD579TD, for example, is capable of a full accuracy conversion in 1.8μs. In order to benefit from this high speed, a fast sample-hold amplifier (SHA) such as the HTC-0300 is required. This SHA has an acquisition time to 0.01% of approximately 300ns, so that a complete sample-convert-acquire cycle can be accomplished in approximately 2.5μs. This means a sample rate of 400kHz can be realized, allowing a signal with no frequency components above 200kHz to be sampled with no loss of information. Note that the EOC signal from the AD579 places the SHA in the hold mode in advance of the actual start of the conversion cycle, and releases the SHA from the HOLD mode only after completion of the conversion. After allowing at least 300ns for the SHA to acquire the next analog value, the converter can again be started.

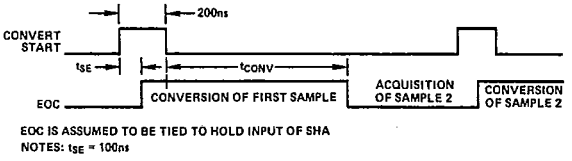

Figure 9. Start/EOC Timing for Sampled Data System

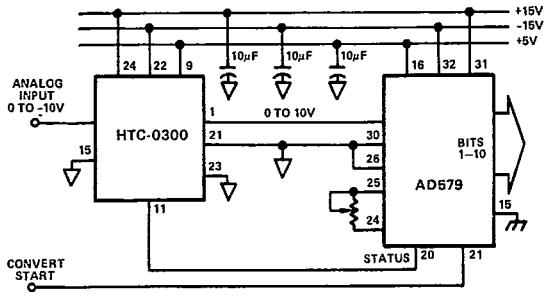

Figure 10. 400kHz — 10-Bit, A/D Conversion System

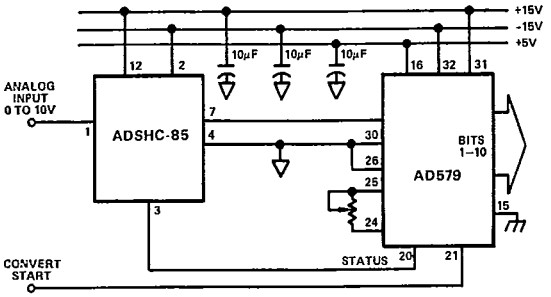

Figure 11. 154kHz — 10-Bit, A/D Conversion System

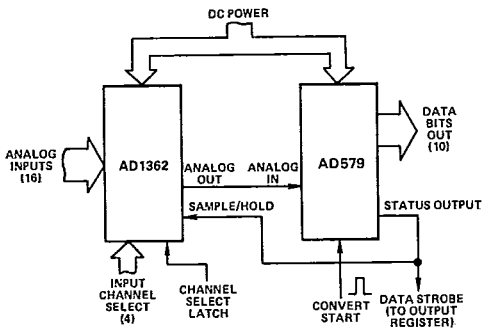

Figure 12. High Speed 10-Bit DAS

A fast (85kHz) 10-bit DAS can be configured using the AD1362 and the AD579. The AD1362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A feature of the AD1362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

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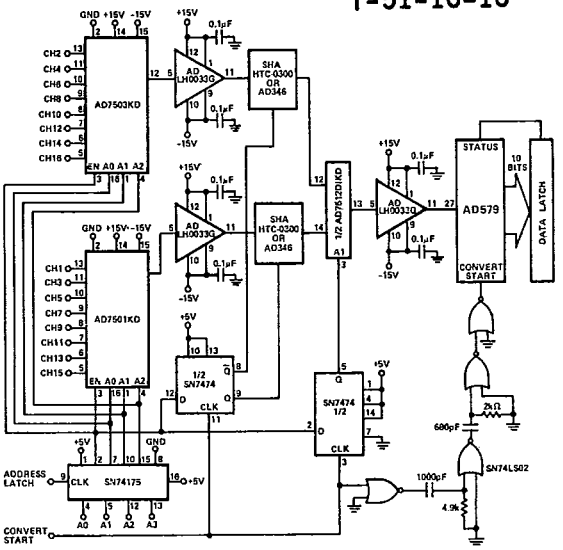

Figure 13. High Speed—165kHz—10-Bit DAS

A high speed 10-bit DAS with a throughput rate of 165kHz can be built around an AD579. The DAS of Figure 13 "Ping Pongs" two sample and hold amplifiers to eliminate the effects of the acquisition time of the sample and hold amplifiers. By applying sequential channel address the A0 of the address enables one of the two multiplexers. The incorporation of the flip-flops on the SHA mode controls and the switch address allows a new channel address to be latched in while a conversion is in progress.