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PEB 2041

Memory Time Switch Replacement (MTSR)

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General Information PEB 2041

Content

SIEMENS

Memory Time Switch Replacement (MTSR) PEB 2041

Technical Manual

G General Overview

G.1 System Background

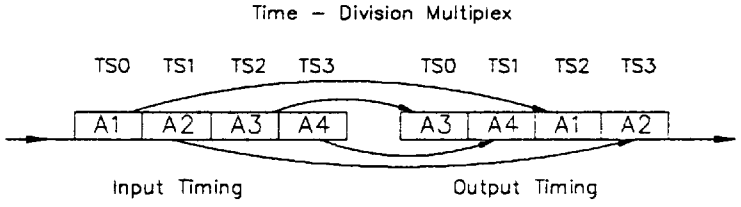
Digital exchanges put calls through by newly arranging the speech signals coded with 8-bit words (PCM time slots). The code words are transmitted serially on PCM lines. The sampling frequency of 8 kHz produces PCM frames with a duration of 125 µs. The transmission rate on the line determines how many code words (speech channels) can be accommodated within a sampling period. With a data rate of 2048 kbps for example, there are 32 time slots of 8 bits each. 4 lines with a data rate of 8192 kbps have a transmission capacity of 512 channels.

In a digital switching matrix one distinguishes between two basic switching principles:

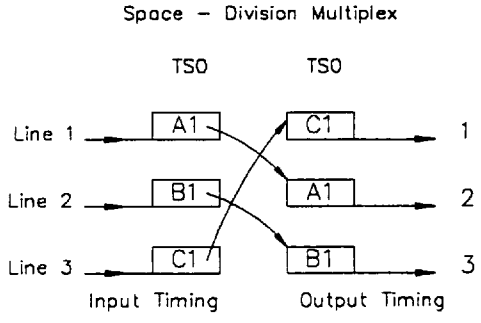
* time - division multiplex
* space - division multiplex

A method that is frequently used involves a combination of the two principles, this being called space/time division multiplex. **Figure G.1** illustrates the different principles.

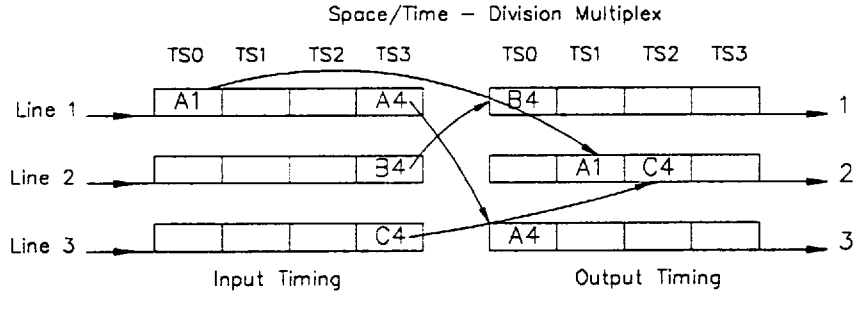
Figure G.1: Switching Principles



Characteristic: the timing of the code words is changed



Characteristic: the code words retain their timing, but the lines are changed



SWITPRIN

In time division multiplex only the time slot is altered during switching. All signals from a certain input PCM line are switched to a fixed output line, only the time slot sequence may change.

In space division multiplex incoming PCM data is only rearranged in space. The input time slot equals the output time slot. However, input from one PCM line can be switched to different output lines.

G.2 Definitions

- The PEB 2041 works with a 8192 kHz clock.
- The bits of a time slot are numbered 0 through 7. Bit 0 of a time slot is the first bit to be received or transmitted by the MTSR, bit 7 the last.

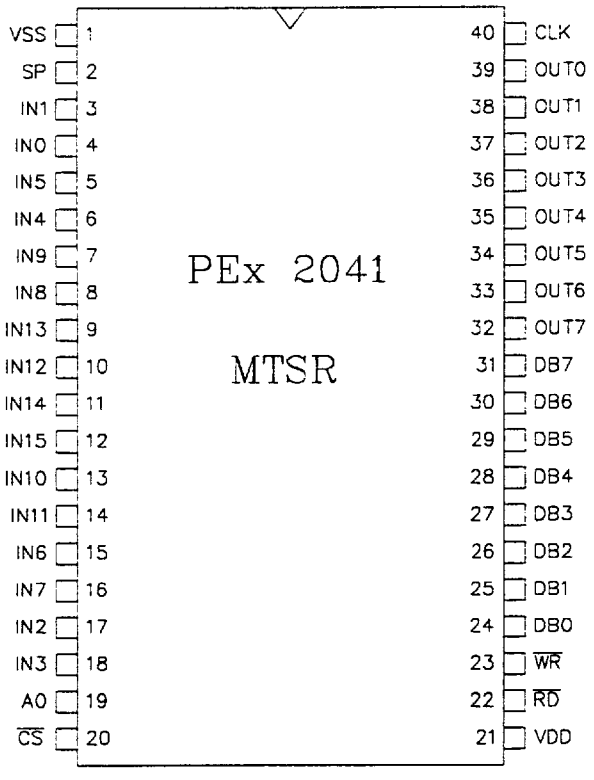
1 Introduction

1.1 Features

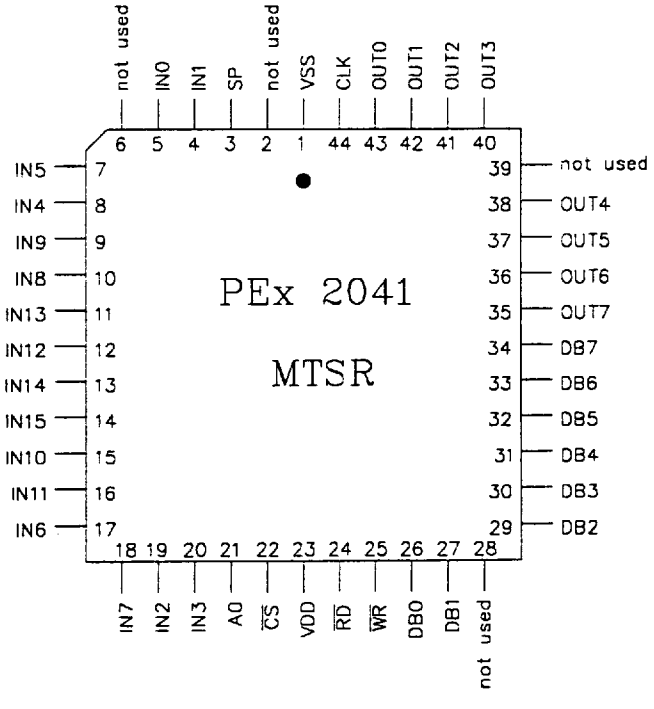
* Time/space switch for 2048, 4096 or 8192 kbps PCM systems
* Switching of up to 512 incoming PCM channels to up to 256 outgoing PCM channels
* Tristate function for further expansion and tandem operation
* Non blocking switch 512 * 512 can built with two devices
* 16 input and 8 output PCM lines
* Different kinds of modes (2048, 4096, 8192 kbit/sec or mixed mode)
* Space, Time, Space/Time switch mode
* 8 bit µP interface
* Single + 5 V power supply
* Advanced low power CMOS technology
* Pin and software compatible to the PEB 2040

1.2 Pin Configuration and Functional Diagram

Figure 1.1: Pin Configuration (top view)

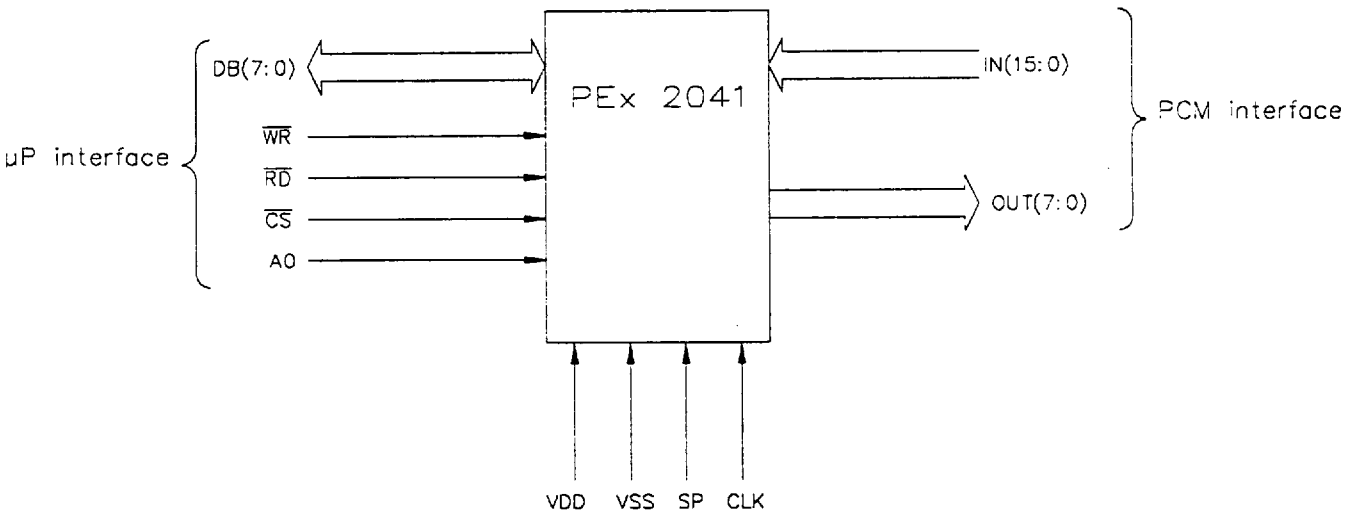


PINDIP



PINPLCC

Figure 1.2: Functional Symbol



FCTSYSC

1.3 Device Overview

The Siemens Memory Time Switch PEx 2041 is a monolithic CMOS circuit connecting any of 512 incoming PCM channels to any of 256 outgoing PCM channels. The on-chip connection memory is accessed via the 8 bit µP interface.

The PEx 2041 is fabricated using the advanced CMOS technology from Siemens and is mounted in a P-DIP 40 or a PLCC 44 package. Inputs and outputs are TTL-compatible.

The PEx 2041 is pin and software compatible to the PEB 2040. In addition, it includes the following features.

* 4096 kbps PCM data rate
* Fast connection memory access

1.4 System Integration

The main application field for the PEx 2041 is in switches. **Figure 1.3** shows a non-blocking switch for 512 input and 512 output channels using only two devices. **Figure 1.4** shows how 8 devices can be arranged to form a non-blocking 1024 channel switch. This is possible due to the tristate capability of the PEx 2041.

Figure 1.3: Memory Time Switch 16/16 for a Non-blocking 512 - Channel Switch

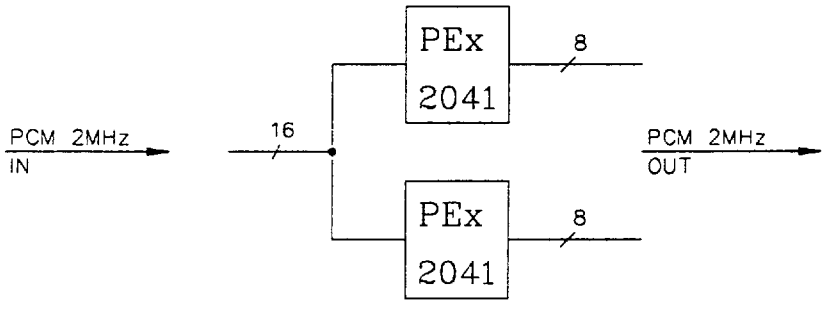
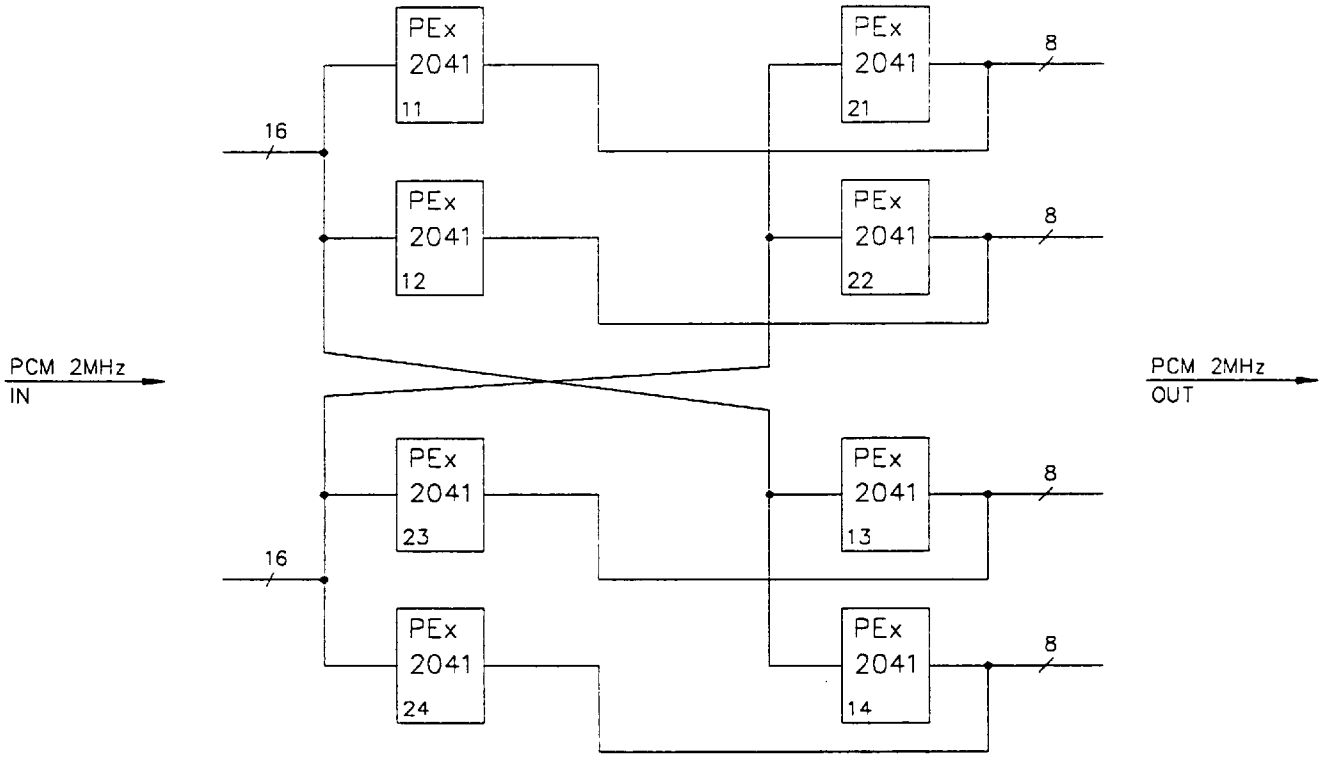


Figure 1.4: Memory Time Switch 32/32 for a Non-blocking 1024 - Channel Switch



32_32STS

Figure 1.5: Basic Connections to a Digital Switchings System

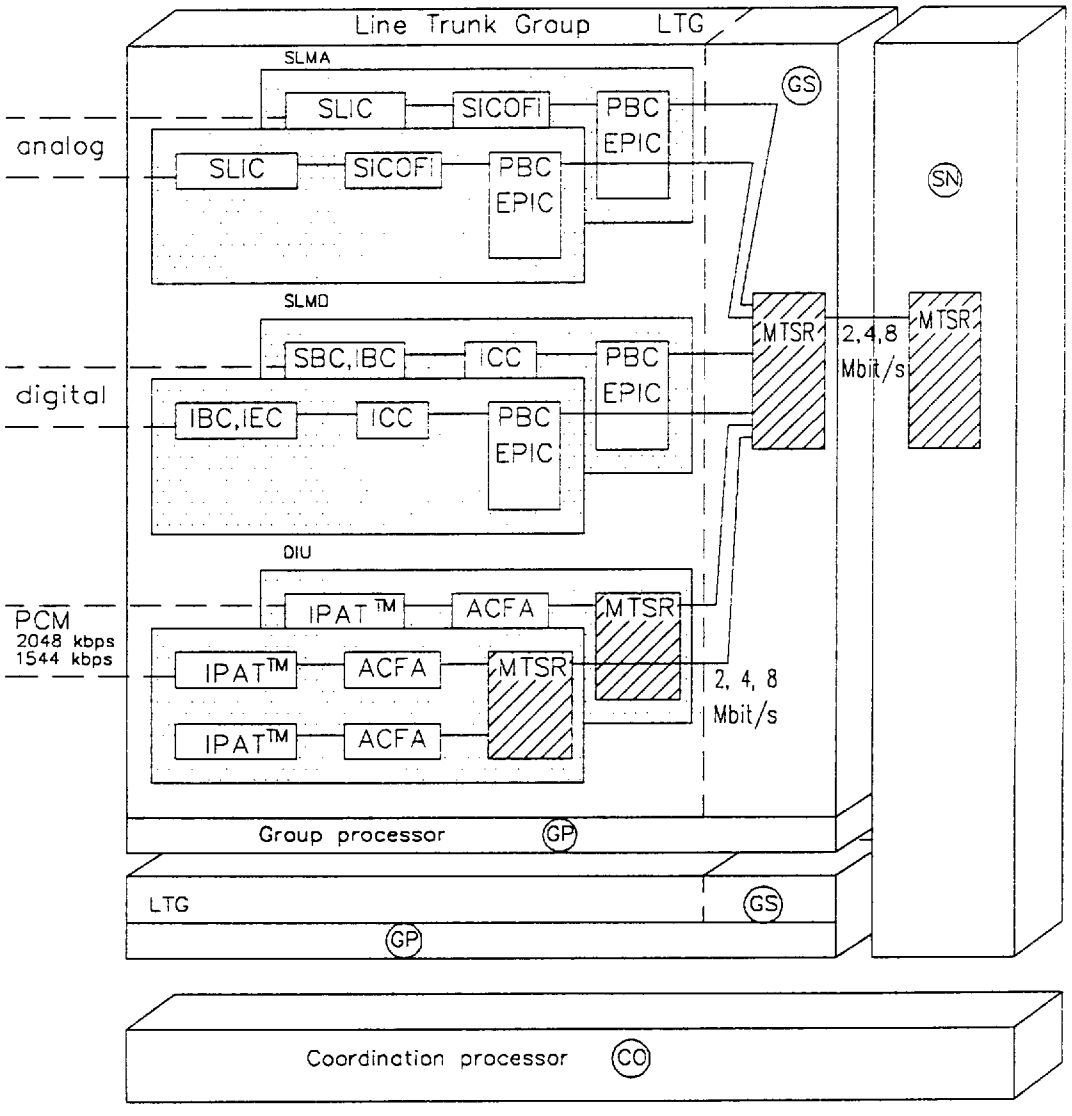


Figure 1.5 shows the PEx 2041 in its different applications in a digital switching system.It is used here as the main device in the switching network (SN), as a group switch (GS) to connect different digital or analog subscriber line modules (SLMA, SLMD) or digital interface units (DIU) with one another and as the interface device for the digital interface units. The SLICs and SICOFIs (PEB 2060) are subscriber line drivers and codec-filter devices, respectively, for the analog line. SBC (PEB 2080), IEC (PEB 2090), IBC (PEB 2095) and ICC (PEB 2070) are the layer 1 and layer 2 ISDN devices for the digital line. The peripheral board controller PBC (PEB 2050) or EPIC (PEB 2055/6) multiplex the different lines in a subscriber line module to the 2 or 4 Mbit/s highways, which are input to the group switch.

2 Functional Description

The PEx 2041 is a memory time switch device. It can connect any of 512 PCM input channels to any of 256 output channels.

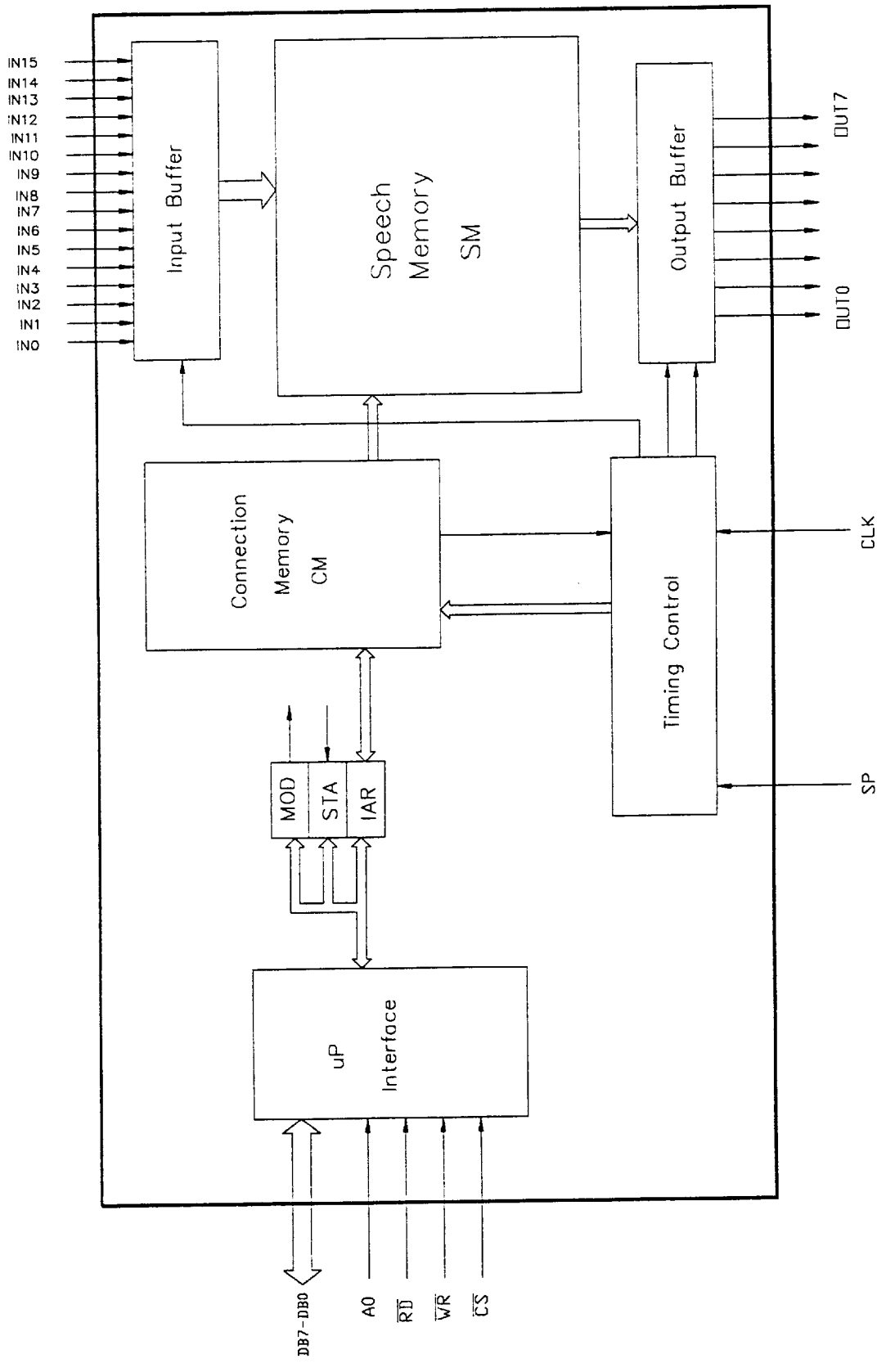
The input information of a complete frame is stored in the on - chip 4 kbit speech memory SM. (See **Figure 2.1**). The incoming 512 channels of 8 bits each are written in sequence into fixed positions in the SM. This is controlled by the input counter in the timing control block with a 8 kHz repetition rate.

For outputting, the connection memory (CM) is read in sequence. Each location in CM points to a location in the speech memory. The byte in this speech memory location is read into the current output time slot. The read access of the CM is controlled by the output counter which also resides in the timing control block.

Hence the CM needs to be programmed beforehand for the desired connection. The CM address corresponds to one particular output time slot and line number. The contents of this CM address points to a particular input time slot and line number (now resident in the SM).

In the following chapters the functions of the PEx 2041 will be covered in more detail.

Figure 2.1: Block Diagram of the PEx 2041



FUNCDESC

2.1 Basic Functional Principles

2.1.1 Preparation of the Input Data

The PEx 2041 works in 2048, 4096 or 8192 kbps PCM systems with a frame frequency of 8000 Hz. Therefore a frame consists of 32, 64 or 128 time slots of 1 byte each. In order to fill the speech memory, which has a fixed capacity of 512 channels, either 16, 8 or 4 input lines are necessary. Thus, in 4 and 8 MHz systems only some of the 16 input lines can be used.

Moreover, the PEx 2041 can also work with two different input data rates simultaneously. In this case some of the PCM input lines operate at one data rate, while others operate at another. Table 2.1 states the number of input lines operating at the different data rates for all possible input data rate combinations. In the following they will be referred to as input modes.

The input mode the PEx 2041 is actually working in has to be programmed into the mode register, bits MI1, MI0, MO1, MO0. In **chapter 4.1** you will find a complete description which input line is connected to which system, for each of the input modes.

Table 2.1: Possible Input Modes

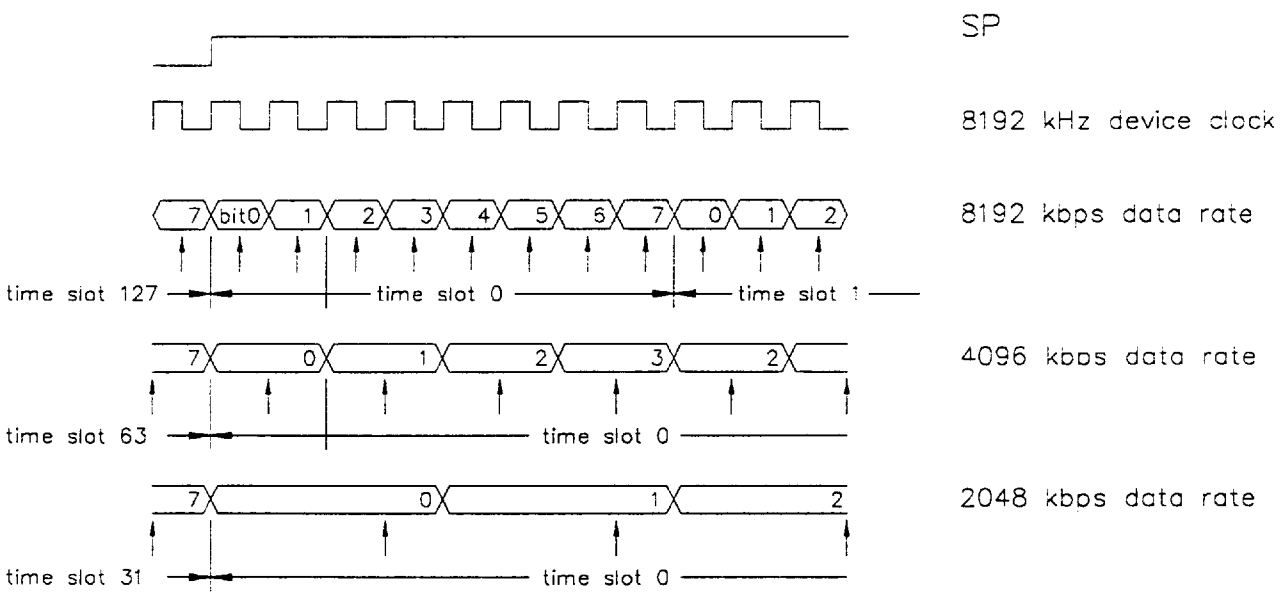
Input Lines				Type
16	x	2048	kbit/sec	single mode
8	x	4096	kbit/sec	single mode
4	x	8192	kbit/sec	single mode
2x8192	+	8x2048	kbit/sec	mixed mode
4x4096	+	8x2048	kbit/sec	mixed mode

The PEx 2041 runs with a 8192 kHz device clock.

The preparation of the input data according to the selected input mode is made in the input buffer. It converts the serial data of a time slot to parallel form.

Time slot 0 begins with the rising edge of the SP pulse as shown in **Figure 2.2**.

Figure 2.2: Latching Instant for Input Data



INLATIME

As can be seen above the beginning of an input time slot is defined such, that the input lines have settled to a stable value, when the datum is actually sampled.

4096 and 8192 kbps data is sampled in the middle of the bit period at the falling edge of the respective data clock. 2048 kbps data is sampled after 3/4 of the according bit period, i.e. with the rising edge of the 4th 8192 kHz clock cycle of the considered bit period.

2.1.2 Speech Memory

The prepared input data is written into the speech memory SM. It has a capacity of 512 bytes to store one frame of all active input lines. The destination SM addresses are supplied by the input counter, which resides in the timing control block. They ensure that a certain input channel is always written to the same physical speech memory location. The input counter is synchronized with the rising edge of the SP signal.

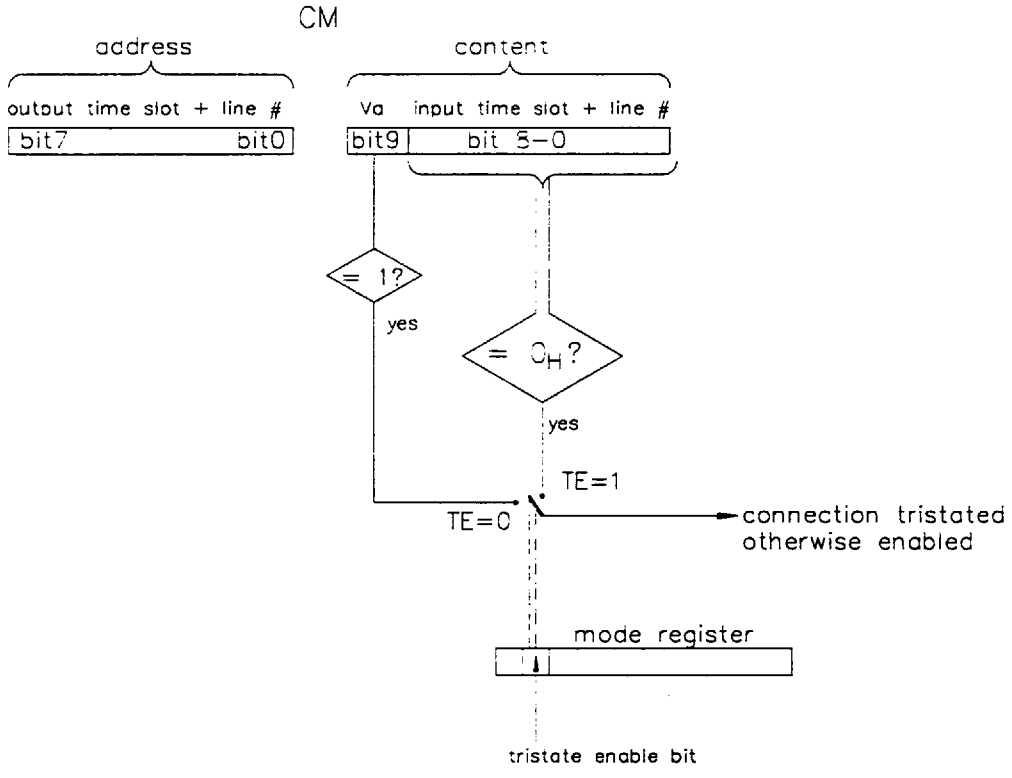
The 9 bit addresses for reading the speech memory are supplied by the connection memory. These are programmable and need not follow any recognizable sequence.

Write and read accesses of the SM occur alternately.

2.1.3 Connection Memory

The connection memory (CM) is a RAM organized as 256 x 10 bits. It contains the 9 bit speech memory address and a validity bit for the 256 possible output channels. While the speech memory address points to a location in the SM, the validity bit is processed in the timing control block: If the TE bit in the mode register (see **paragraph 4.1**) is set to logical 0, the validity bit is directly forwarded to the output buffer as the tristate control signal. Otherwise (if TE = high), an all - zero speech memory address causes the output for the associated channel to be tristate. In this case the all - zero speech memory address (time slot 0 on output line 0) cannot be used for switching purposes.

Figure 2.3: The Influence of the Connection Memory on the Output Validity



CMTRISCE

The CM is written via the µP interface using the indirect register access scheme (see **paragraph 2.2.1**). It is read using addresses supplied by the output counter which resides in the timing control block. The output counter generates addresses that form an enumerative sequence. Thus the connection memory is read cyclically and establishes the correct time slot sequence of the outputs.

The output counter is synchronized with the falling and rising edge of the SP signal.

The connection memory addresses and data encode the number of the output and input channels, respectively. For a detailed description of the code please refer to **paragraph 2.2.1** and **4.3.1**.

2.1.4 Output Buffer

The output buffer rearranges the data read from the speech memory. It basically converts the parallel data to serial data. Depending on the tristate control signal from the timing control block the output buffer outputs the data or switches the line to high impedance.

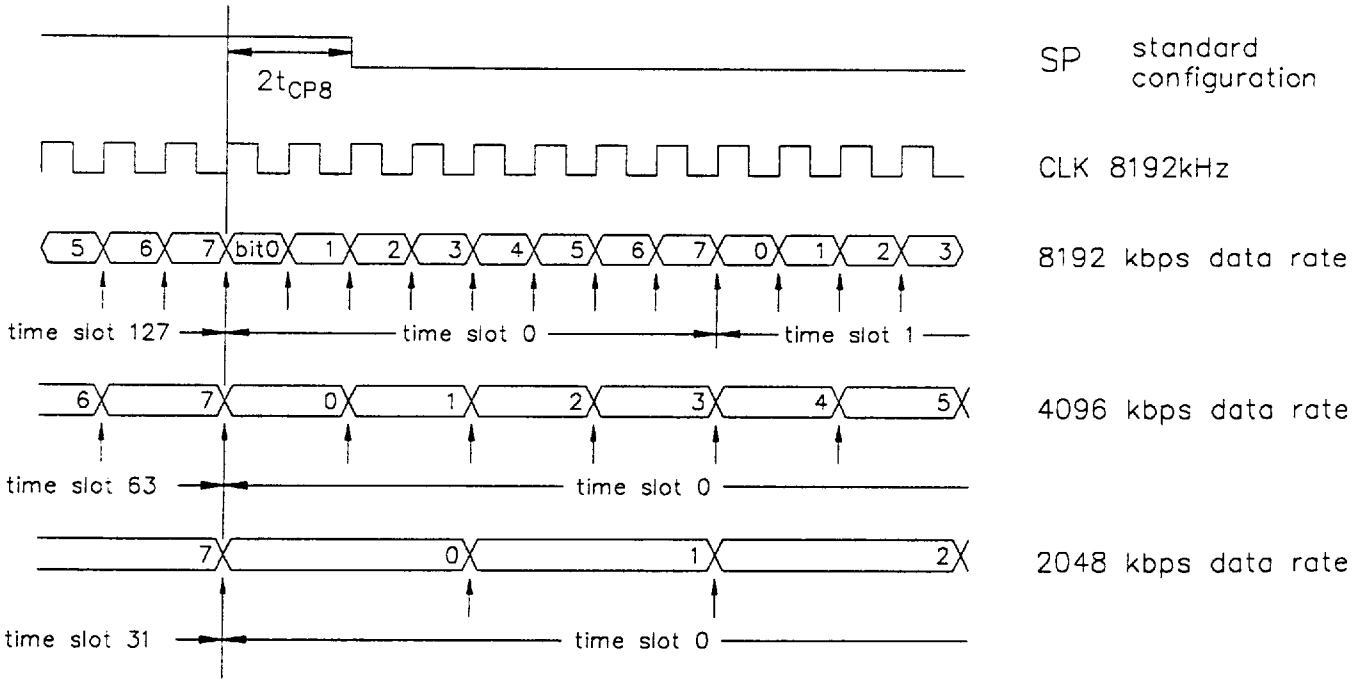
The mode register (**MOD**) bits MI1, MI0, MO1 and MO0 control this process. The possible output modes are listed in **Table 2.2**.

Table 2.2: Possible Output Modes

Output Lines				Type
8	x	2048	kbit/sec	single mode
4	x	4096	kbit/sec	single mode
2	x	8192	kbit/sec	single mode
1x8192	+	4x2048	kbit/sec	mixed mode
2x4096	+	4x2048	kbit/sec	mixed mode

Figure 2.4 shows, when the single bits are output. They are clocked off at the rising clock edge at the beginning of the considered bit period. Time slot 0 starts two t_{CP8} before the falling edge of the SP pulse.

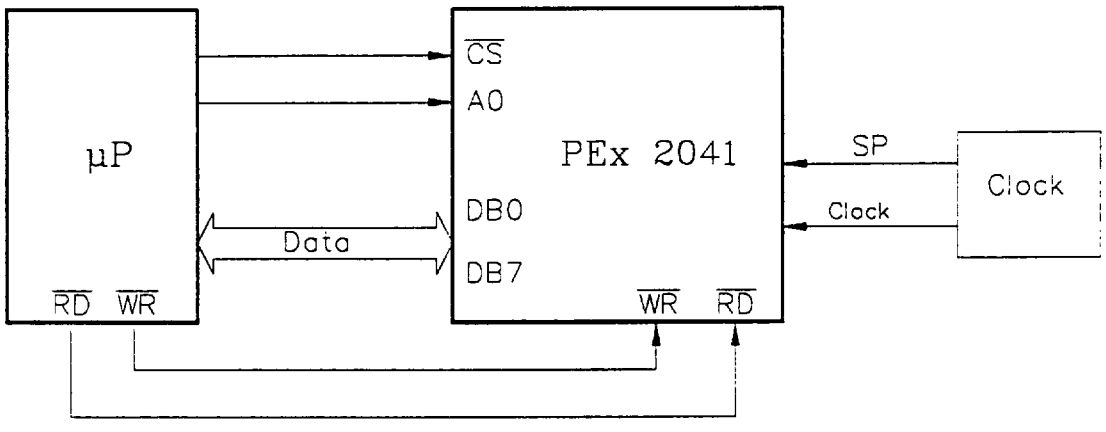
Figure 2.4: Clocking Off Instant of Output Data



2.2 Microprocessor Interface and Registers

The PEx 2041 is programmed via the µP interface. It consists of the data bus DB7...DB0, the address bit A0, the Write ($\overline{WR}$), the Read ($\overline{RD}$), the Chip Select ($\overline{CS}$) signal, as shown in **Figure 2.5**.

Figure 2.5: The PEx 2041 Controlled by a Microprocessor



UPENV

To perform any register access, $\overline{CS}$ has to be zero. This pin is provided, so that a single chip can be activated in an environment where one microprocessor controls many slave processors (see **Figure 3.2**).

The PEx 2041 incorporates 2 user accessible registers,

* the mode register (**MOD**)
* the status register (**STA**)

as well as

* the connection memory (CM).

The mode register is a write only register; the status register is a read only register; the CM can be read and written to by register access to the **IAR**! The single address bit A0 does not offer enough address space to encode all access possibilities. Therefore the indirect access scheme is used to access the CM. It uses the indirect access register (IAR), which is provided on chip.

Using the 3 signals A0, $\overline{WR}$ and $\overline{RD}$ the **IAR**, **MOD** and **STA** registers can be identified according to **Table 2.3**.

Table 2.3: Addressing of the Direct Registers

A0	Write Operation	Read Operation
0	MOD	STA
1	IAR	IAR

The A0 address distinguishes between the IAR and the directly accessible registers. The $\overline{WR}$ and $\overline{RD}$ strobes combined with an A0 equal to logical 0 identify the mode- and status registers, respectively. The data bus contains the associated information. In the following paragraphs the indirect register access and the register contents will be described.

2.2.1 Indirect Register Access (A0 = 1)

To perform an indirect register access 3 consecutive instructions have to be programmed. One indirect register access has to be completed before the next one can begin. The 3 instructions of the indirect access operate on the indirect access register. It receives in sequence the control byte, the data byte and the address byte according to **Table 2.4**.

Table 2.4: IAR Byte Structure

bit7							bit 0	
0	0	K1	K0	0	0	C1	C0	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

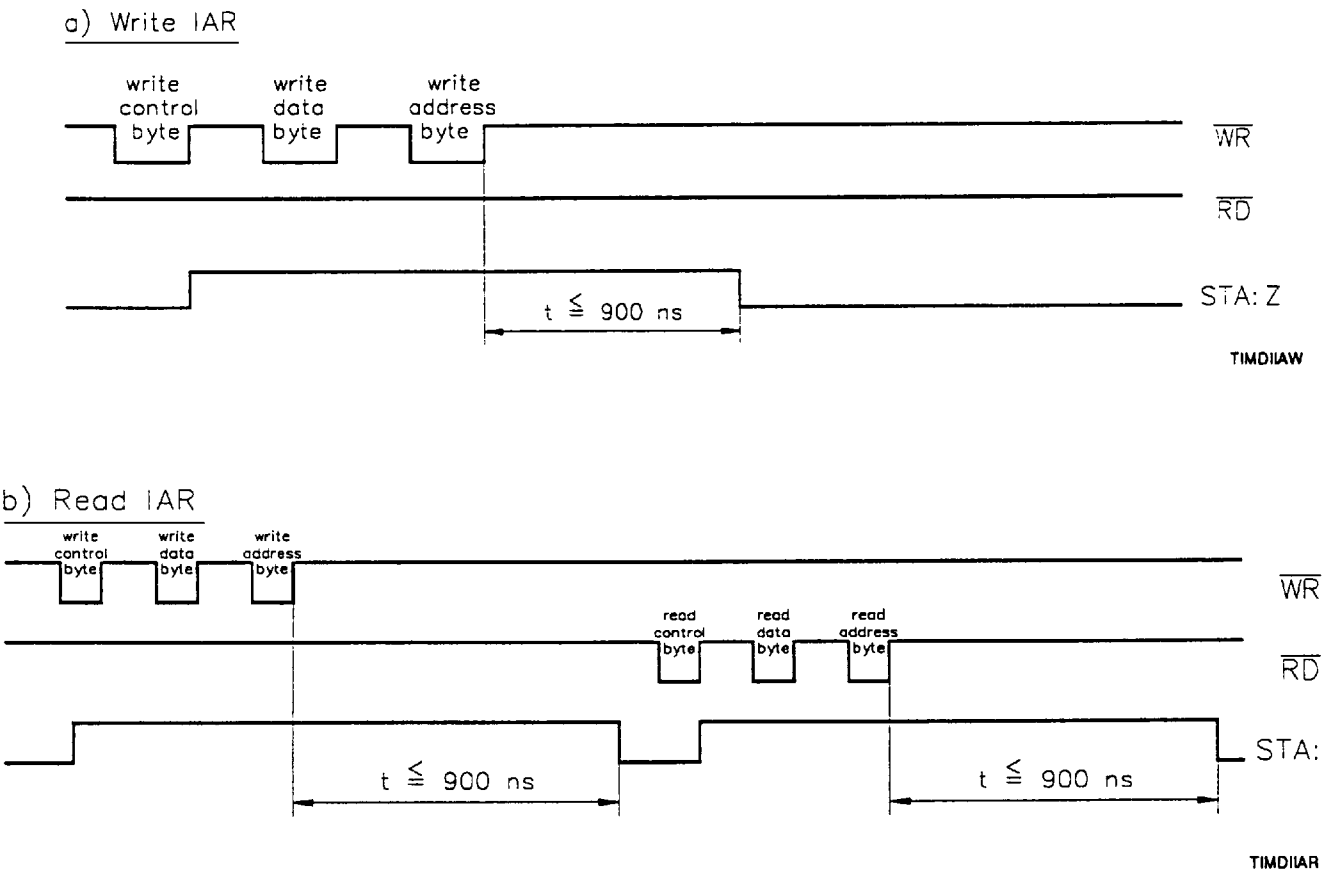
The data byte contains the information which shall be written into the connection memory. The address byte indicates in which location of the CM the data shall be written. The control byte determines whether a write or read operation shall be performed.

Before an indirect access is started, the **Z**- and **B**-bits of the status register must be 0. With the first instruction the **Z**-bit is set (see **chapter 4.2**). After the third instruction the PEx 2041 accesses the physical register or memory location. This access requires maximally 900 nsec. After the access has been finished the **Z**-bit is reset. The 3 instructions are separated by intervals where both $\overline{WR}$ and $\overline{RD}$ are in a high state.

Figure 2.6.a) illustrates a write operation on the IAR.

It is possible to read or write the direct access registers (i.e. the mode or status register) while an indirect access is in progress. Thus the status register may be read in the time intervals that separate the three sequential indirect access instructions. Also, the current indirect access may be aborted by setting the **MOD:RI**.

Figure 2.6: Timing diagrams for IAR



Bits K1 and K0 of the control byte determine whether a CM or an indirect register access shall be performed.

Table 2.5: Decoding the K1 and K0 Bits

K1	K0	Accessed Register	R/W
0	0	CM	R
0	1	CM	W
1	0	CM	W

The K1 and K0 bits also indicate the type of the access: One bit being logical 1 indicates a write, both bits being logical 0 indicates a read operation.

The address byte holds the CM address for a connection memory access.

The data to be written to the CM reside in the data byte. For CM accesses 10 bits instead of 8 bits are written into the selected location. The two additional bits come from the C0 and C1 bits of the control byte and are interpreted as the most significant bits of the data word. (D9 and D8). Accordingly the 3 CM access instructions are interpreted as shown in **Table 2.6**.

Table 2.6: Connection Memory Access IAR Byte Structure

bit 7 bit 0

0	0	K1	K0	0	0	D9	D8	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The following example illustrates how an indirect memory access works.

The instruction sequence

00010010

00000000 A0 = 1, $\overline{WR}$ = 0, $\overline{RD}$ = 1, $\overline{CS}$ = 0

10101010

writes the hexadecimal value 200_H into the connection memory location AA_H thus tristating the output.

To read the indirect registers or the CM two sequences of 3 instructions each have to be programmed.

In the first sequence the PEx 2041 is instructed which CM address has to be read. The data transferred to the PEx 2041 in this first sequence is of no importance.

With the first write instruction **STA:Z** is set.

The PEx 2041 needs 900 ns following the first 3 instructions to read the specified location and to write the result to the IAR. It overwrites the data byte and in the case of a CM read operation additionally bits 1 and 0 of the control byte. The status register bit **Z** is reset after maximally 900 nsec. Then 3 read operations follow. Again, **STA:Z** is set with the first read instruction. The 3 instructions read 3 bytes from the IAR. **Figure 2.6.b)** shows this procedure. The data byte and the C1 and C0 bits in the control byte show the values read from the CM. The K0, K1 bits and the address byte have not changed their values since the preceeding write instruction sequence.

After the third read operation the PEx 2041 needs another 900 ns to reset the indirect access mechanism and the **Z**-bit in the status register.

With the following instruction sequence

00000001

11111111 A0 = 1, $\overline{WR}$ = 0, $\overline{RD}$ = 1, $\overline{CS}$ = 0

10101010

the byte sequence

11001110

00000000 A0 = 1, $\overline{WR}$ = 1, $\overline{RD}$ = 0, $\overline{CS}$ = 0

10101010

can be read.

The CM location AA_H, which has been written to 200_H in the last example is read again.

Bits 7, 6, 3, 2, of the control byte showing logical 0 in the first byte at the beginning of the read access reappear as logical 1 in the fourth byte. This is due to the internal device architecture. These bits are unused and are recommended to be set to logical 0 to avoid future incompatibility problems.

2.2.2 Register Contents

You will find a detailed description of the different register contents in section 4. This paragraph is only a short overview of the different registers:

The mode register contains bits to determine the operation mode and the output tristating scheme, to control the CM reset mechanism, to interrupt the indirect access mechanism and to switch the chip to standby.

The status register consists of 3 bits. They tell whether the PEx 2041 is busy resetting its connection memory or performing an indirect access or whether operational conditions have occured which might lead to a partial or complete loss of data in the connection and speech memory. Bits 4 to 0 of the status register default to logical 0.

The connection memory content and address contain the connection information. Specifics are explained in the following sections.

2.3 Standard Mode

In this application 512 channels per frame are written into the speech memory. Each one of them can be connected to any output channel.

According to **Table 4.3** and **Table 4.7** and depending on the selected mode the least significant bits of the connection memory address and data contain the logical pin numbers, the most signifant bits the time slot number of the output and input channels.

The following example explains the programming sequence.

Time slot 7 of the incoming 8192 kbit/s input line IN 14 shall be connected to timeslot 6 of the output line OUT 5 of an 2048 kbit/sec system. According to **Table 4.3** in 8192 kbit/sec systems the input line IN 14 is the logical input line 2. Output line number and logical output number are identical to one another.

Therefore the following byte sequence on the data bus has to be used to program the CM properly:

(see **Table 4.6**)

00010000

00011110

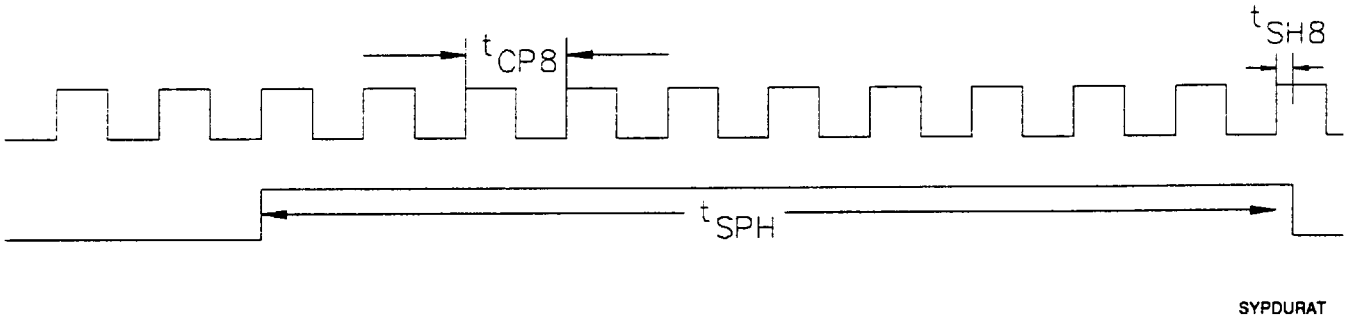
00110101

For all input channels the frame starts with the rising edge of the SP signal. The frame for all output channels begins two t_{CP8} before the falling SP edge. The period of time between the rising and falling edge of the SP pulse should be

$$t_{SPH} = (2 + N \times 4)\, t_{CP8} \qquad (0 \leq N \leq 255).$$

N is an user defined integer. By varying N, t_{SPH} can be varied in 2048 kHz clock period steps. For an example using N = 2 refer to **Figure 2.7**.

Figure 2.7: SP Duration for N =2



SYPDURAT

The device is synchronized after 3 SP pulses (see **chapter 3.2**).

2.4 Space Switch Mode

The space switch mode is selected by the mode bits MI1, MI0, MO1, MO0 = D_H.

In the space switch mode the basic operational principles differ from those outlined in **chapter 2.1**. In the speech memory only a quarter frame is stored restricting the connection capabilities of the PEx 2041.

All 16 input lines run at a data rate of 8192 kbit/sec delivering 2048 bytes of data in each frame. Since the speech memory can only hold 512 bytes, the data bytes must be read within a quarter of a frame period to be outputted on one of the two 8192 kbit/sec output lines.

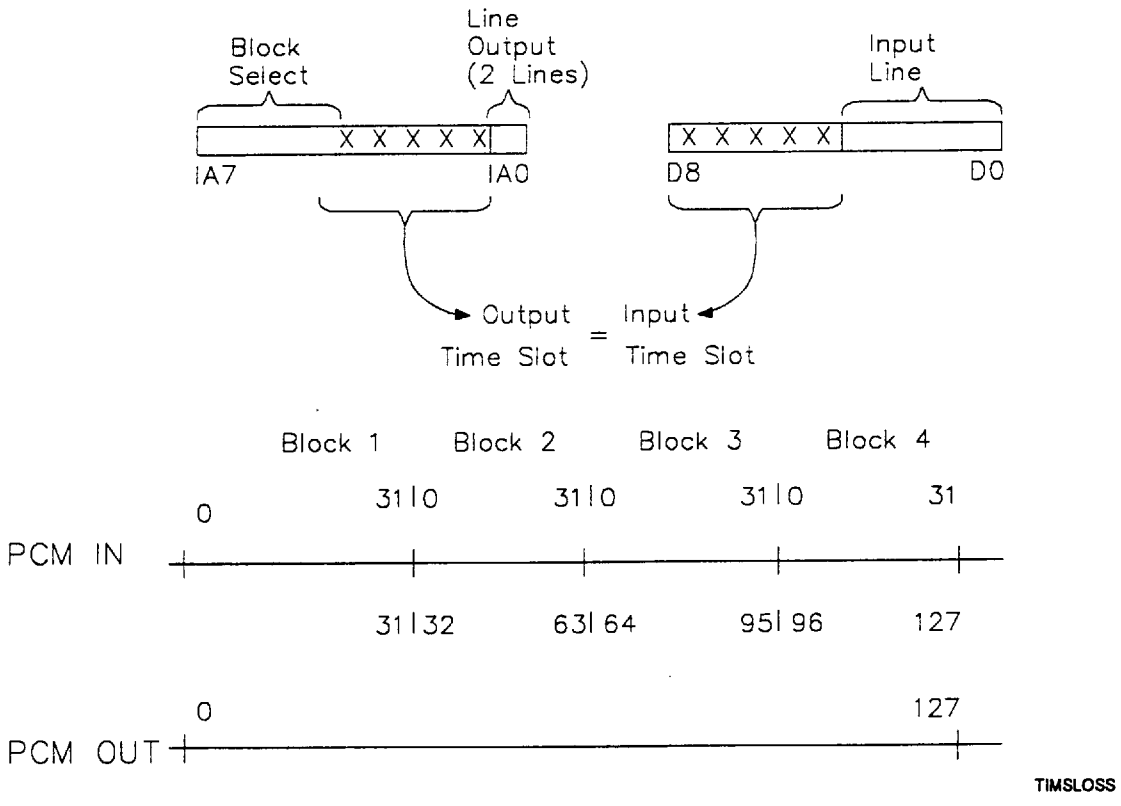
In space switch mode it is recommended that the SP pulse be 282 t_{CP8} long (N = 70). For proper functionality the time slot numbers of a programmed connection must be equal. In the following only this case considered.

The output time slot is encoded in the connection memory address. Since the input time slot has to be the same it is not necessary to fully specify it in the CM data. However the 5 least significant bits must be programmed (see **Tables 4.7** and **4.8**).

The speech memory address is composed of 4 bits (D0 through D3) for the coding of the 16 input (logical line number and pin names match) lines and 5 bits (D4 through D8) for the coding of 32 time slots. Which of the four blocks of 32 time slots each is switched to the output lines is determined by the connection memory address. This consists of 1 bit (IA0) for the marking of one of two possible output lines with 7 bits (IA1 through IA7) for the 128 time slots, as shown on the next page.

The SP signals controls the start of the input and output frame. The output frame starts two t_{CP8} before the falling SP edge. However, the rising edge marks the beginning of time slot 125.

Figure 2.8: Determination of Input- and Output Time Slots in Space Switch Mode



The following two examples show how the connection memory is programmed in the space switch mode.

input line 10, time slot 31 -> output line 1, time slot 31

00010011

11111010

00111111

input line 10, time slot 63 -> output line 1, time slot 63

00010011

11111010

01111111

3 Operational Description

3.1 Power Up

Upon power up the PEx 2041 is set to its initial state. The MOD register bits are all set to logical 1. The status register **B**-bit is undefined, the **Z**-bit contains logical 0, the **R**-bit is undefined.

This state is also reached by pulling the $\overline{WR}$ and $\overline{RD}$ signals to logical 0 at the same time, (software reset). For the software reset the state of $\overline{CS}$ is of no significance.

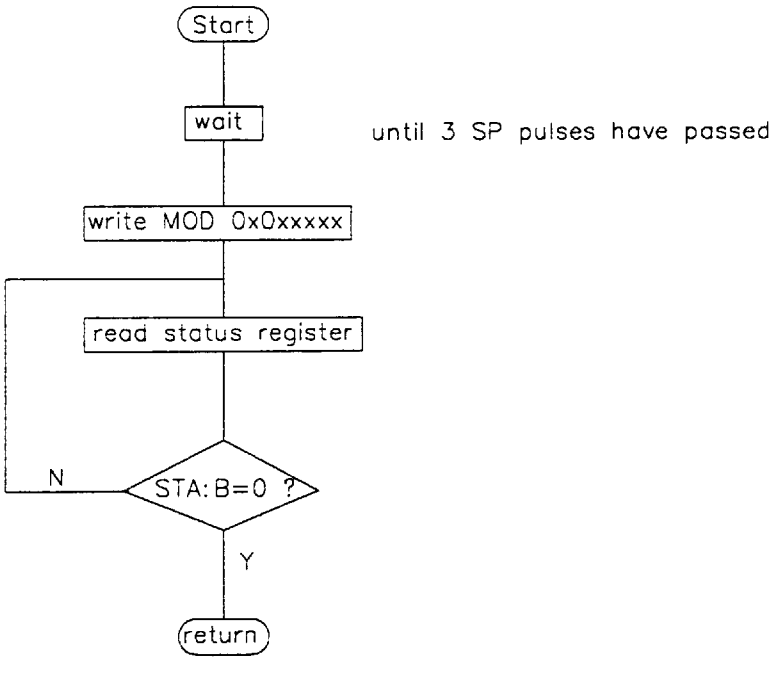
3.2 Initialization Procedure

After power up a few internal signals and clocks need to be initalized. This is done with the initialization sequence. To give all signals and clocks a defined value the MTSR must encounter 3 falling and 2 rising edges of the SP signal. The resulting SP pulses may be of any length allowed in normal operation, the time interval between the two SP pulses may be of any length down to 250 ns.

With all signals being defined, the CM needs to be reset. To do that a logical 0 is written into **MOD:RC**. **STA:B** is set. The resulting CM reset is finished after at most 250 µs and is indicated by the status register **B**-bit being logical 0. Changing the pulse shaping factor N during CM reset may result in a CM reset time longer than 250 µs.

To prepare the PEx 2041 for programming the CM, the **RI**- bit in the mode register must be reset. Note that one mode register access can serve to reset both **RC** and **RI** bits as well as configuring to chip (i.e. selecting operating mode etc.).

Figure 3.1.: Initializing the PEx 2041

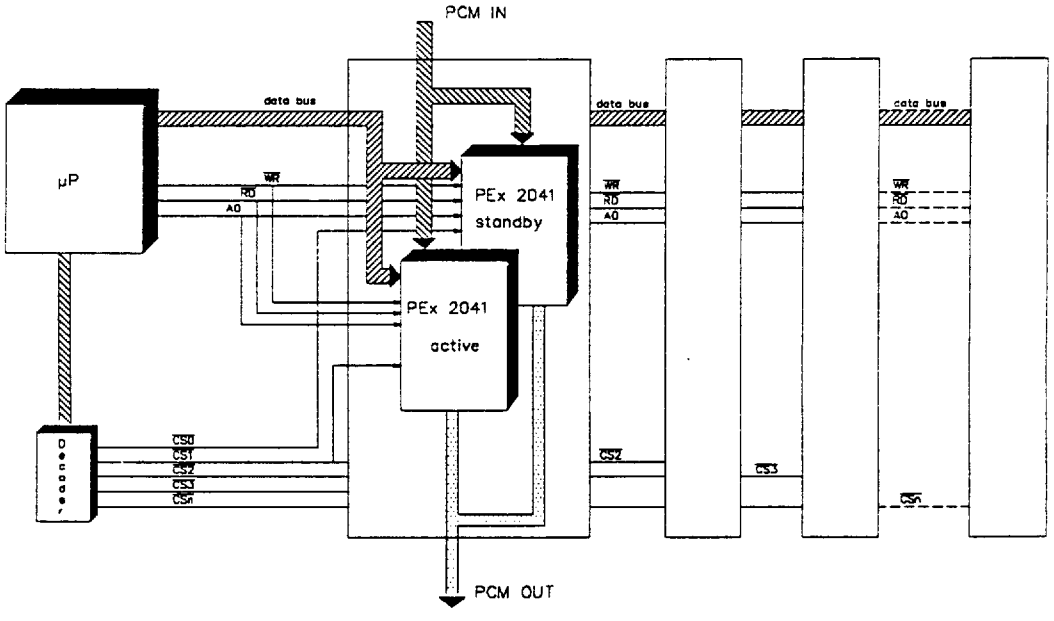


INIT8MHZ

3.3 Standby mode

With **MOD:SB** being logical 1 the PEx 2041 works as a backup device in redundant systems. It can be accessed via the µP interface and works internally like an active device. However, the outputs are high impedance. If the **SB**-bit is reset the outputs are switched to low impedance for the programmed active channels and this MTSR can take over from another device which has been recognized as being faulty. See **Figure 3.2.**

Figure 3.2: Device Setup in Redundant Systems



REDSYS

4 Detailed Register Description

The following registers may be accessed:

Table 4.1: Addressing the direct registers

Address A0	Write Operation	Read Operation
0	MOD	STA
1	IAR	IAR

The chapters in this section cover the registers in detail.

4.1 Mode Register (MOD)

Access: write on address 0

DB 7 DB 0

RC	TE	RI	SB	MI1	MI0	MO1	MO0

Value after power up: FF_H

RC reset connection memory; writing a zero to this bit causes the complete connection memory to be overwritten with 200_H (tristate). During this time **STA:B** is set. The maximum time for resetting the connection memory is 250 µs.

TE: tristate enable; this bit determines which tristating scheme is activated:

TE = 1: If the speech memory address written into the connection memory is D8 - D0 = 0, the output channel is tristated.

TE = 0: The D9 bit written into the connection memory is interpreted as a validity bit: D9 = 0 enables the programmed connection, S9 = 1 tristates the output.

Note: If TE = 1, time slot 0 of the logical input line 0 cannot be used for switching.

RI: reset indirect access mechanism; setting this bit resets the indirect access mechanism. RI has to be cleared before writing/reading IAR after reset.

SB: stand by; By selecting SB = 1 all outputs are tristated. The connection memory works normally. The PEx 2041 can be activated immediately by resetting SB.

MI1/0:

MO1/0: input/output operation mode; these bits define MO1/0: the bit rate of the input and output lines. The bit rates are given in **Table 4.2**, the corresponding pin functions in **Table 4.3**.

Table 4.2: Input/Output Operating Modes

MI1	MI0	MO1	MO0	input mode		output mode	
0	0	0	0	16x2	Mbit/s	8x2	Mbit/s
0	0	0	1	16x2	Mbit/s	2x8	Mbit/s
0	0	1	0	16x2	Mbit/s	4x2/1x8	Mbit/s
0	1	0	0	4x8	Mbit/s	8x2	Mbit/s
0	1	0	1	4x8	Mbit/s	2x8	Mbit/s
0	1	1	0	4x8	Mbit/s	4x2/1x8	Mbit/s
1	0	0	0	2x8/8x2	Mbit/s	8x2	Mbit/s
1	0	0	1	2x8/8x2	Mbit/s	2x8	Mbit/s
1	0	1	0	2x8/8x2	Mbit/s	4x2/1x8	Mbit/s
0	0	1	1	8x4	Mbit/s	4x4	Mbit/s
0	1	1	1	4x8	Mbit/s	4x4	Mbit/s
1	1	1	1	4x4/8x2	Mbit/s	4x2/2x4	Mbit/s
1	0	1	1	8x4	Mbit/s	2x8	Mbit/s
1	1	0	1	16x8	Mbit/s	2x8	Mbit/s*
1	1	0	0	unused			
1	1	1	0	unused			

* for space switch application only

Note: In the mixed modes the first bit rate refers to the odd line numbers, the second one to the even line numbers.

Table 4.3: Input and Output Pin Arrangement

Input Pin Arrangement

Pin-Nr. DIP	Pin-Nr. PLCC	16x8 Mbit/s 16x2 Mbit/s	4x8 Mbit/s	8x2 + 2x8 Mbit/s	8x4 Mbit/s	8x2 + 4x4 Mbit/s
3	4	In 1				
4	5	In 0		In 0		In 0
5	7	In 5				
6	8	In 4		In 4		In 4
7	9	In 9			In 1	In 1
8	10	In 8		In 8	In 0	In 8
9	11	In 13	In 1	In 1	In 5	In 5
10	12	In 12	In 0	In 12	In 4	In 12
11	13	In 14	In 2	In 14	In 6	In 14
12	14	In 15	In 3	In 3	In 7	In 7
13	15	In 10		In 10	In 2	In 10
14	16	In 11			In 3	In 3
15	17	In 6		In 6		In 6
16	18	In 7				
17	19	In 2		In 2		In 2
18	20	In 3				

Note: The input line numbers shown are the logical line numbers to be used for programming the connection memory. In the case of 16 input lines the logical line numbers are identical to the pin names.

Output Pin Arrangement

Pin-Nr. DIP	Pin-Nr. PLCC	8x2 Mbit/s	2x8 Mbit/s	4x2 + 1x8 Mbit/s	4x4 Mbit/s	4x2 + 2x4 Mbit/s
32	35	Out 7		Out 7		Out 7
33	36	Out 6				
34	37	Out 5		Out 5		Out 5
35	38	Out 4				
36	40	Out 3		Out 3	Out 3	Out 3
37	41	Out 2			Out 2	Out 2
38	42	Out 1	Out 1	Out 1	Out 1	Out 1
39	43	Out 0	Out 0	Out 0	Out 0	Out 0

4.2 Status Register (STA)

Access: read at address 0

DB 7 DB 0

B	Z	R	0	0	0	0	0

B busy: the chip is busy resetting the connection memory (B=1). B is undefined after power up and logical 0 after the device initialization.

Note: The maximum time for resetting the connection memory is 250 µs.

Z incomplete instruction; a three byte indirect instruction is not completed (Z=1). Z is 0 after power up.

Note: Z is reset and the indirect access is cancelled by setting **MOD:RI** or resetting **MOD:RC**

R initialization request. The connection memory has to be reset due to loss of data (R=1). The R bit is set after power failure or inappropiate clocking and reset when the connection memory reset is finished. R is undefined after power up and logical 0 after the device initialization.

4.3 Indirect Access Register (IAR)

(Read or Write Operation with Address A0 = 1)

An indirect access is performed by reading/writing three consecutive bytes (first byte = control byte, second byte = data byte, third byte = address byte) to/from IAR. The structure is shown in **Table 4.4.**

Table 4.4: The 3 Bytes of the Indirect Access

bit 7 bit 0

0	0	K1	K0	0	0	C1	C0	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The control byte bits K1 and K0 determine the type of access being performed according to **Table 4.5.**

Table 4.5: Encoding the Different Types of Indirect Accesses

K1	K0		C1	C0	address byte		type of access	
0	0		D9	D8	CM-Address		Read	CM
1	0		D9	D8	CM-Address		Write	CM
0	1		D9	D8	CM-Address		Write	CM

4.3.1 Connection Memory Access

For a connection memory access the control byte bits C1 and C0 contain the data bits D9 and D8, respectively. D9 is the validity bit which together with D8 and the data byte D7-D0 is written to the CM address IA7-IA0.

The function of the validity bit is controlled by **STA:TE** (see 5.2). D8-D0 and IA7-IA0 contain the information for the logical line and time slot numbers of the programmed connection, D8-D0 for the inputs, IA7-IA0 for the outputs. **Tables 4.6** through **4.8** show the programming of these bits for the different configurations and modes.

Standard Mode

Table 4.6: Time Slot and Line Programming for Standard Mode

All modes except space switch mode					
2 Mbit/s input lines	bit	D3	to	D0	logical line number
	bit	D8	to	D4	time slot number
	bit	D9			validity bit
4 Mbit/s input lines	bit	D2	to	D0	logical line number
	bit	D8	to	D3	time slot number
	bit	D9			validity bit
8 Mbit/s input lines	bit	D1	to	D0	logical line number
	bit	D8	to	D2	time slot number
	bit	D9			validity bit
2 Mbit/s output lines	bit	IA2	to	IA0	line number
	bit	IA7	to	IA0	time slot number
4 Mbit/s output lines	bit	IA1	to	IA0	line number
	bit	IA7	to	IA2	time slot number
8 Mbit/s output lines	bit	IA0			line number
	bit	IA7	to	IA1	time slot number

The pulse shape factor N may take any integer value from 0 to 255.

Space Switch Mode

Table 4.7: Time Slot and Line Programming for Space Switch Mode

Space-switch-mode	(MI1=1, MI0=1; MO1=0, MO0=1)				
8 Mbit/s input lines	bit	D0	to D3		logical line number
	bit	D4	to	D8	the lower 5 bits of the time slot number
	bit	D9			validity bit
8 Mbit/s output lines	bit	IA0			logical line number
	bit	IA1	to	IA7	time slot number

N is fixed to 70. The selection of one specific input time slot is possible by writing the connection memory (CM) as shown below.

Table 4.8: Programming Input and Output Lines and Time Slots in Space Switch Mode

In CM address 00-3F: D8-D4 (SM addr.)	=	TS0	-	TS3
In CM address 40-7F: D8-D4 (SM addr.)	=	TS32	-	TS63
In CM address 80-BF: D8-D4 (SM addr.)	=	TS6	-	TS95
In CM address C0-FF: D8-D4 (SM addr.)	=	TS96	-	TS127

In space switch mode the leading edge of the SP pulse must be applied with the first bit of time slot 125. The input and output time slot number must match.

5 Electrical Specification

5.1 Pin Definitions and Functions

Table 5.1: MTSR Pin Definitions and Functions

PIN No. DIP	PIN No. PLCC	Symbol	Input (I) Output (O)	Function
1	1	Vss	I	Ground (OV)
2	3	SP	I	Synchronization Pulse: The PEx 2041 is synchronized relative to the PCM system via this line.
3	4	IN1	I	PCM Input Ports: Serial data is received at these lines at standard TTL levels.
4	5	IN0	I	
5	7	IN5	I	
6	8	IN4	I	
7	9	IN9	I	
8	10	IN8	I	
9	11	IN13	I	
10	12	IN12	I	
11	13	IN14	I	
12	14	IN15	I	
13	15	IN10	I	
14	16	IN11	I	
15	17	IN6	I	
16	18	IN7	I	
17	19	IN2	I	
18	20	IN3	I	
19	21	A0	I	Address 0: When high, the indirect register access mechanism is enabled. If A0 is logical 0 the mode and status registers can be written to and read respectively.
20	22	$\overline{CS}$	I	Chip Select: A low level selects the PEx 2041 for a register access operation.
21	23	V_{DD}	I	Supply Voltage 5V ± 5 %.
22	24	$\overline{RD}$	I	Read: This signal indicates a read operation and is internally sampled only if $\overline{CS}$ is active. The MTSR puts data from the selected internal register on the data bus with the falling edge of $\overline{RD}$. $\overline{RD}$ is active low.

PIN No. DIP	PIN No. PLCC	Symbol	Input (I) Output (O)	Function
23	25	$\overline{WR}$	I	Write: This signal initiates a write operation. The $\overline{WR}$ input is internally sampled only if $\overline{CS}$ is active. In this case the MTSR loads an internal register with data from the data bus at the rising edge of $\overline{WR}$. $\overline{WR}$ is active low.
24	26	DB0	I/O	Data Bus: The data bus is used for communication between the MTSR and a processor.
25	27	DB1	I/O	
26	29	DB2	I/O	
27	30	DB3	I/O	
28	31	DB4	I/O	
29	32	DB5	I/O	
30	33	DB6	I/O	
31	34	DB7	I/O	
32	35	OUT7	0	PCM Output Port: Serial data is sent by these lines at standard CMOS or TTL levels. These pins can be tristated.
33	36	OUT6	0	
34	37	OUT5	0	
35	38	OUT4	0	
36	40	OUT3	0	
37	41	OUT2	0	
38	42	OUT1	0	
39	43	OUT0	0	
40	44	CLK	I	8192 kHz device clock

5.2 Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

PEB 2041 Ambient temperature under bias	0 to 70°C
PEB 2041 Storage temperature	-65 to 125°C
PEF 2041 Ambient temperature under bias	-40 to +85°C
PEF 2041 Storage temperature	-65 to +125°C
Voltage on any pin with respect to ground	-0.4 to V_{DD} +0.4V

5.3 DC Characteristics

Ambient temperature under bias range; V_{DD} = 5V ± 5%, V_{SS} = 0V.

Table 5.2: DC Characteristics of the MTSR

Symbol	Parameter	Limit Value min	Limit Value max	Unit	Test Condition
V_{IL}	Input low voltage	-0.4	0.8	V	
V_{IH}	Input high voltage	2.0	V_{DD}+0.4	V	
V_{OL}	Output low voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output high voltage	2.4		V	I_{OH} = -400 µA
V_{OH}	Output high voltage	V_{DD} -0.5		V	I_{OH} = -100 µA
I_{CC}	Operational power supply current		10	mA	V_{DD} = 5V, Inputs at 0V or V_{DD}, no output loads.
I_{LI}	Input leakage current		10	uA	0V < V_{IN} < V_{DD} to 0V
I_{LO}	Output leakage current				0V < V_{OUT} < V_{DD} to 0V

5.4 Capacitances

Table 5.3: Input/Output Capacitanes of the MTSR

TA = 25°C, V_{DD} = 5V ± 5%, V_{SS} = 0V.

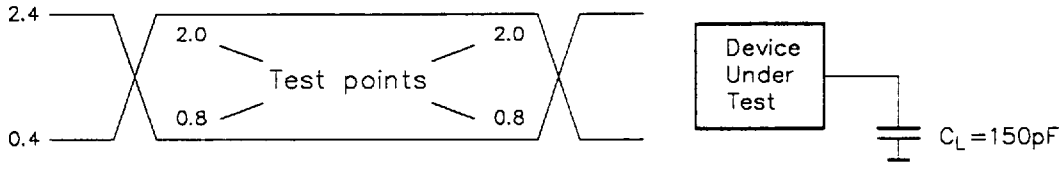
Symbol	Parameter	Limit Value min	Limit Value max	Unit	Test Condition
C_{IN}	Input capacitane		10	pF	
C_{IO}	I/O capacitane		20	pF	
C_{OUT}	Output capacitane		15	pF	

5.5 AC Characteristics

Ambient temperature under bias range, V_{DD} = 5V ± 5%

Inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown below.

Figure 5.1: I/O Waveform for AC Tests



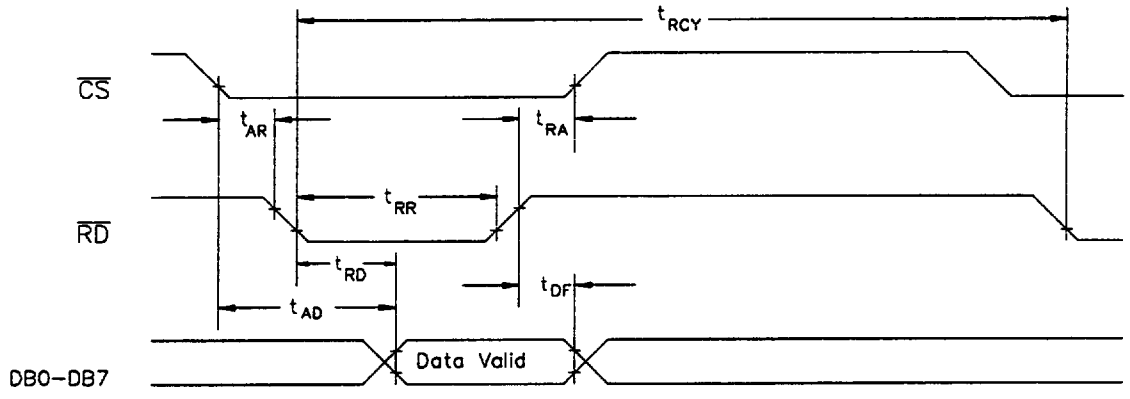
TIMDICON

5.5.1 µP Interface Timing

Table 5.4: Microprocessor Interface Timing

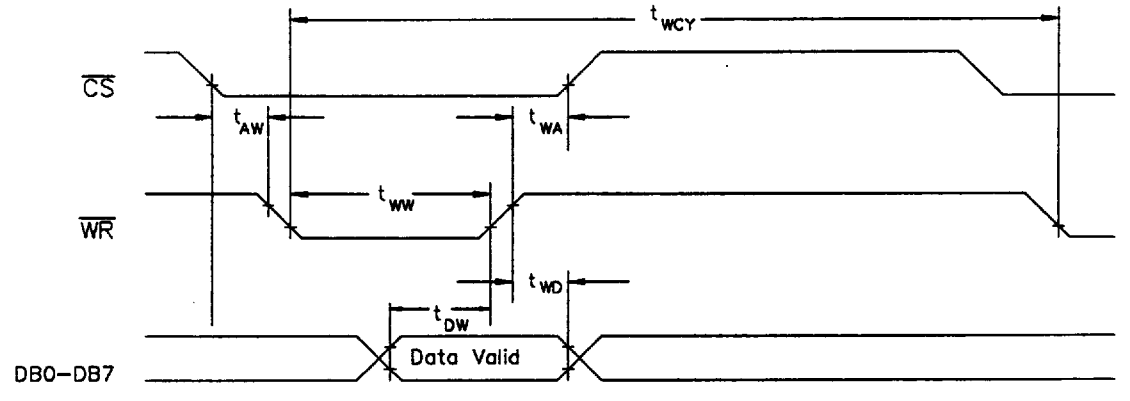
Symbol	Parameter	Limit Values min	max	Unit
t_{AR}	Address stable before $\overline{RD}$	0	-	ns
t_{RA}	Address hold after $\overline{RD}$	0	-	ns
t_{RR}	$\overline{RD}$ width	90	-	ns
t_{RD}	$\overline{RD}$ to data valid	-	90	ns
t_{AD}	Address stable to data valid	-	90	ns
t_{DF}	Data float after $\overline{RD}$	5	25	ns
t_{RCY}	Read cycle time	160	-	ns
t_{AW}	Address stable before $\overline{WR}$	0	-	ns
t_{WA}	Address hold time	0	-	ns
t_{WW}	$\overline{WR}$ width	60	-	ns
t_{DW}	Data setup time	5	-	ns
t_{WD}	Data hold time	15	-	ns
t_{WCY}	Write cycle time	160	-	ns

Figure 5.2: µP Read Cycle



TIMDIUPR

Figure 5.3: µP Write Cycle



TIMDIUPW

5.5.2 PCM Interface Timing

Table 5.5: PCM Interface Timing

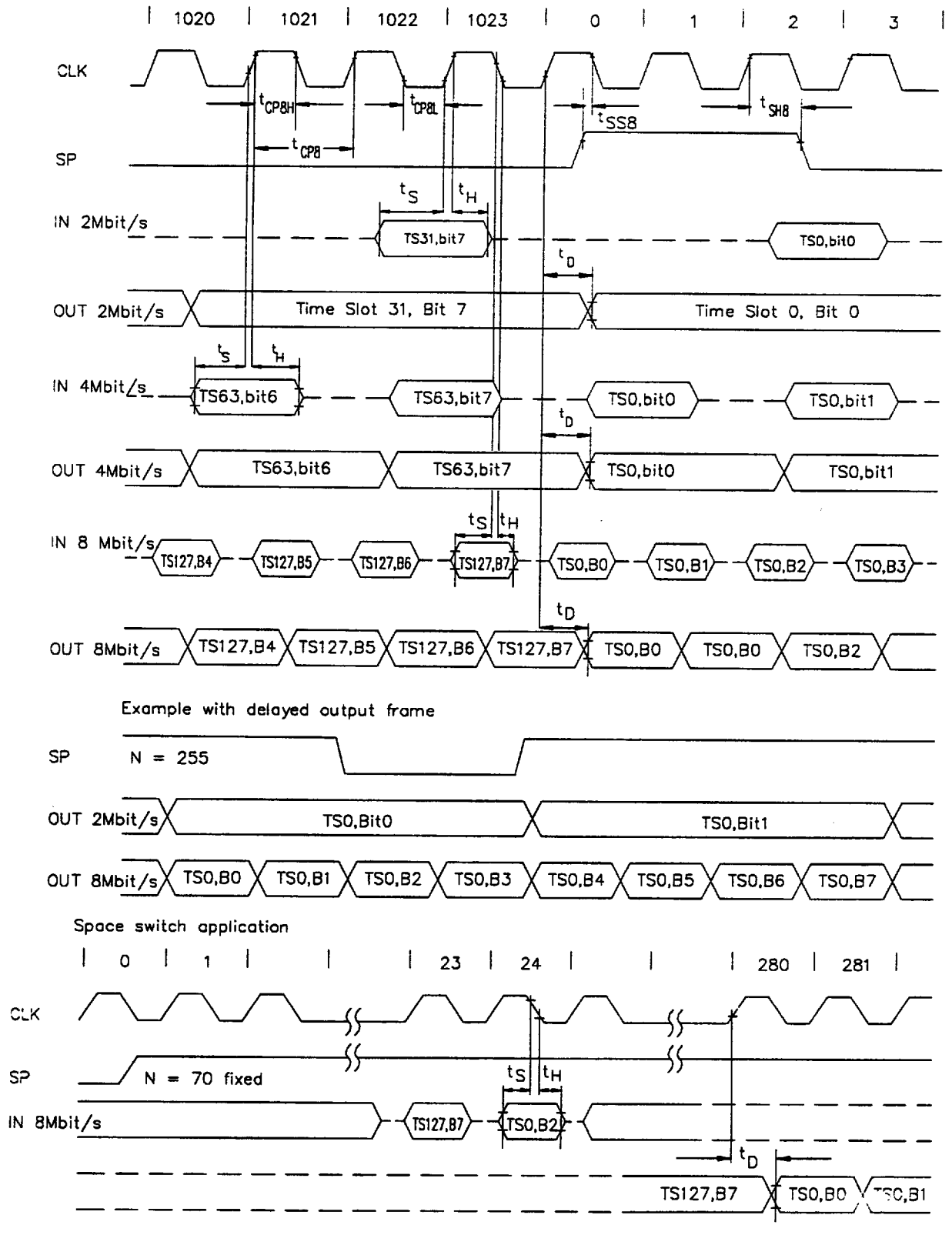
Symbol	Parameter	Limit Values min	max	Unit
t_S	PCM input setup	0	-	ns
t_H	PCM input hold	30	-	ns
t_D	Output Delay	-	45	ns
t_T	tristate delay	-	55	ns

5.5.3 Clock and Synchronization Timing

Table 5.6: PCM Interface Timing

Symbol	Parameter	Limit Values min	max	Unit
t_{CP8H}	Clock period 8 MHz high	40	-	ns
t_{CP8L}	Clock period 8 MHz low	48	-	ns
t_{CP8}	Clock period 8 MHz	120	-	ns
t_{SS8}	Synchronization pulse setup 8 MHz	10	t_{CP8}-20	ns
t_{SH8}	Synchronization pulse delay 8 MHz	0	t_{CP8}-20	ns

Figure 5.4: PCM Line Timing



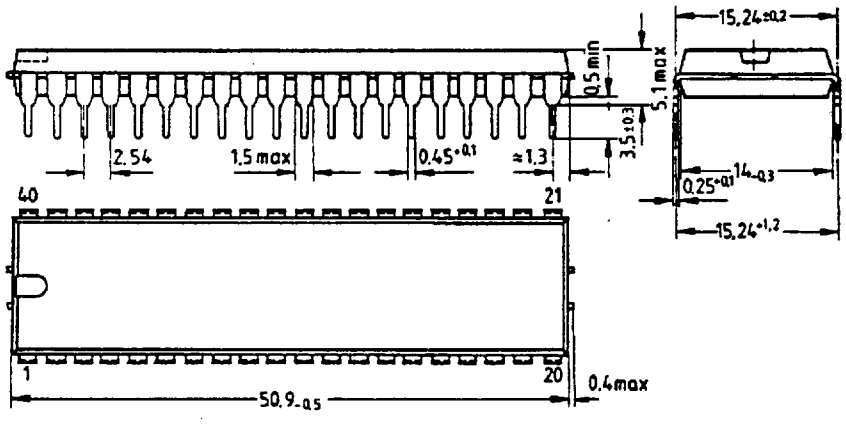
5.6 Busy Time

Table 5.6: Busy times

Operation	Max. Value	Unit
Indirect register access	900	ns
Connection memory reset	250	µs

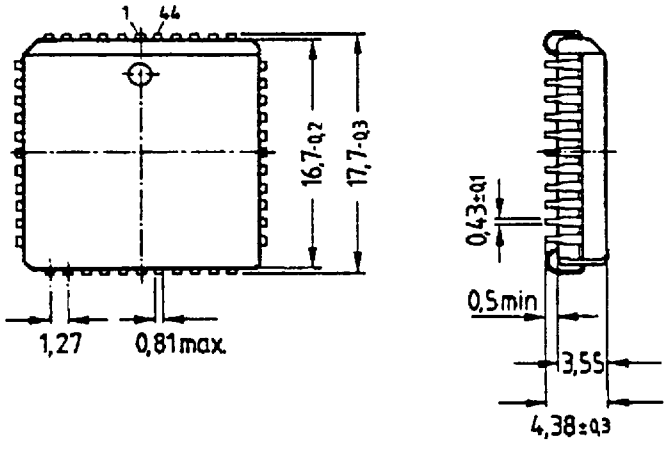
5.7 Package Outline

Figure 5.5: Plastic Package, 40 Pins, P-DIP40



P-DIP_40

Figure 5.6: Plastic Leadless Package, 44 Pins, PLCC 44



PLCC_44

5.8 Ordering Information

Type	Ordering Code	Package Outline
PEx 2041P	Q67100-H6196	P-DIP 40
PEx 2041N	Q67100-H6195	PLCC 44

6 Application Notes

6.1 Operational Examples

In the following examples the output lines are assumed to be routed to ground via a resistor so that they show ground potential if they are not driven.

The examples given for each operating mode are divided up into

- application
- principial timing diagram
- connection memory content
- timing diagrams

Please note that in the timing diagrams the input voltage shape may be somewhat delayed relative to the input time slot structure. This is due to the settling time of the lines. It can be tolerated as long as the lines have settled at the sampling instants.

6.1.1 2048 Mbit/s Mode, Standard Configuration

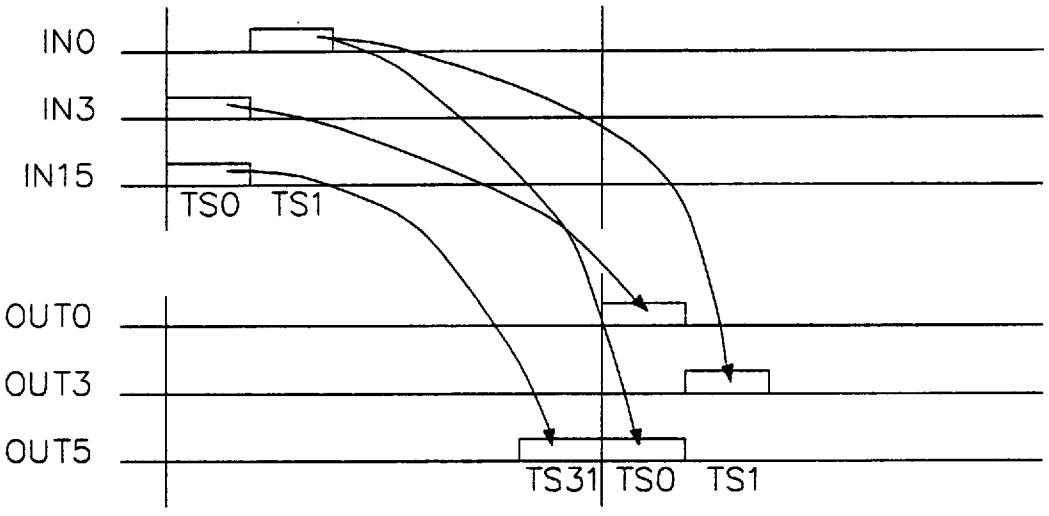
(MI1=0, MI0=0, MO1=0, MO0=0)

Application:

PCM IN:	line 0 time slot 1	connected to	PCM OUT:	line 5 time slot 0 line 3 time slot 1
	line 3 time slot 0	connected to		line 0 time slot 0
	line 15 time slot 0	connected to		line 5 time slot 31

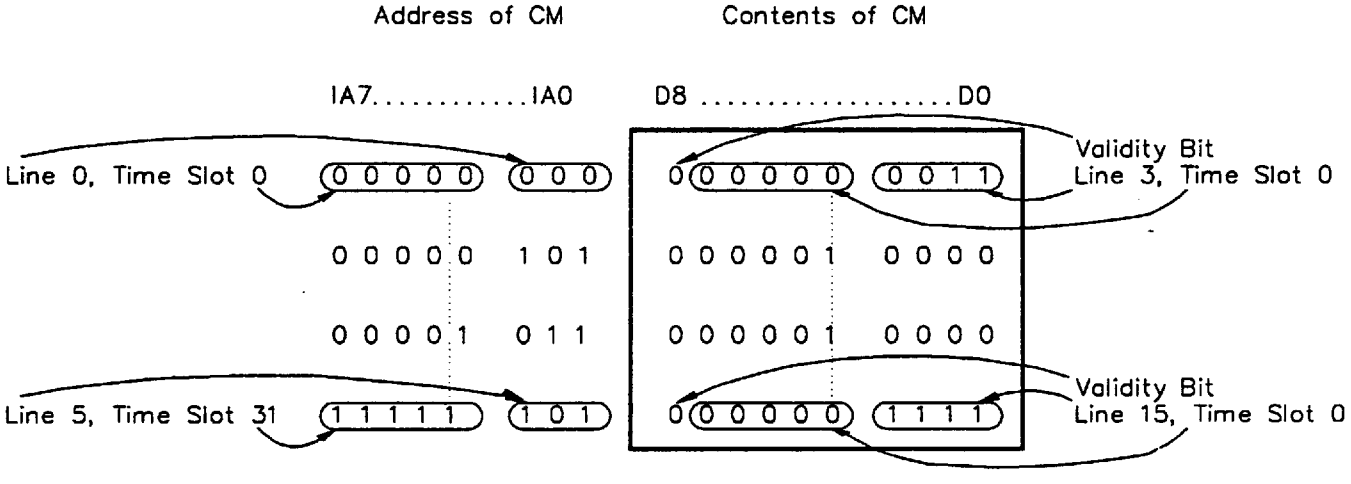
The pin names and the logical line numbers coincide.

Figure 6.1: Principal Timing Diagram for this 2048 kbps Mode Example



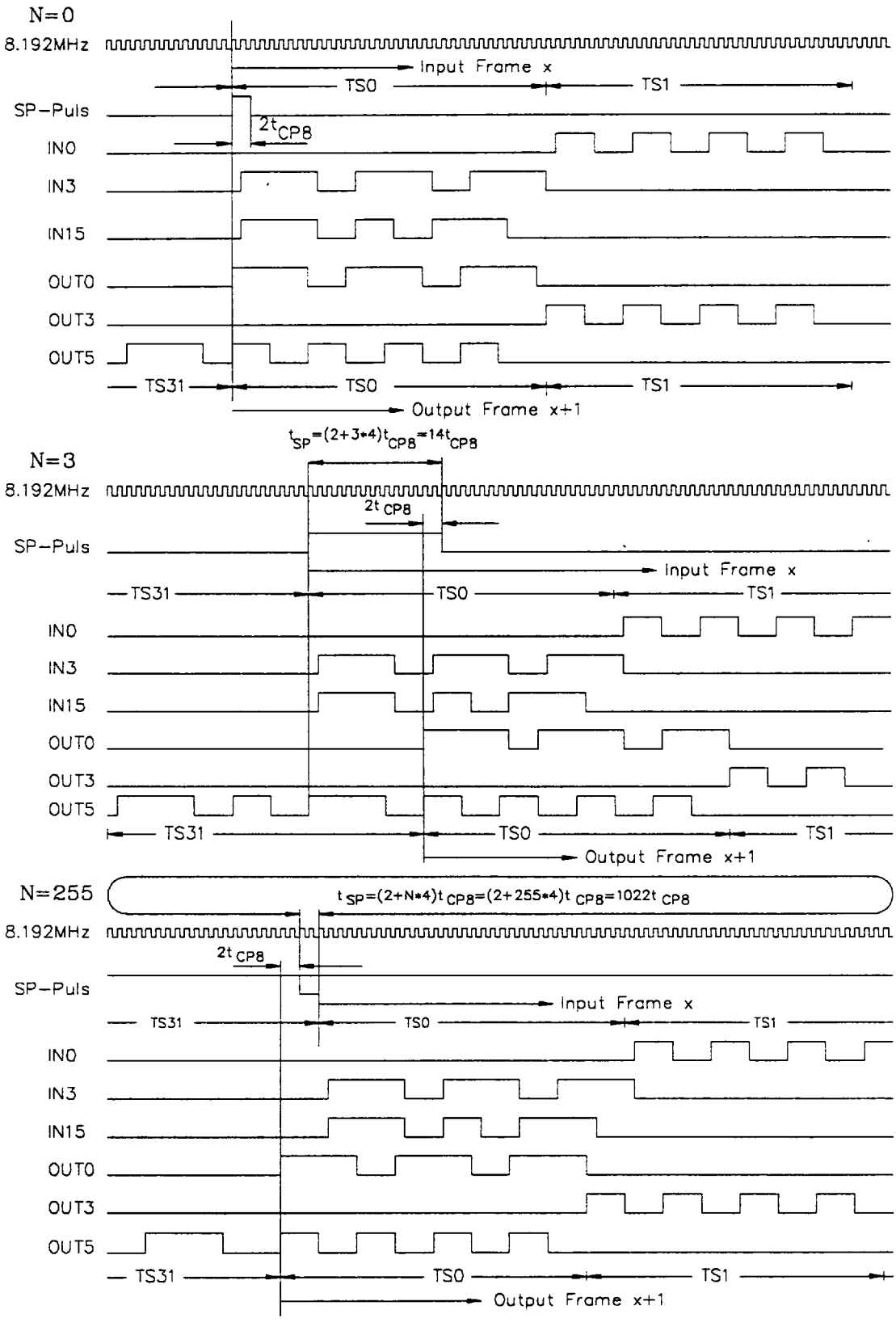
PTIMD12

Figure 6.2: CM Content for this 2048 kbps Mode Example



CMC2

Figure 6.3: Timing Diagrams in this 2048 kbit/s Mode Example for N equalling 0, 3 and 255



TIMDI2

6.1.2 Mixed Mode

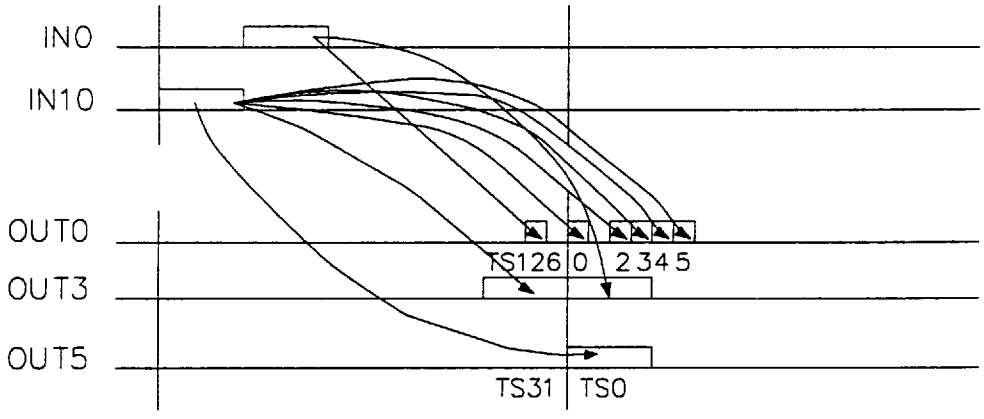
(MI1=1, MI0=0, MO1=1, MO0=0)

Application

PCM IN:	line 0 time slot 1	connected to	PCM OUT:	line 0 (8192 kbps) time slot 126 line 3 (2048 kbps) time slot 0
	line 10 time slot 0	connected to		line 3 (2048 kbps) time slot 31 line 0 (8192 kbps) time slot 0 time slot 2 time slot 3 time slot 4 time slot 5 line5 (2048 kbps) time slot 0

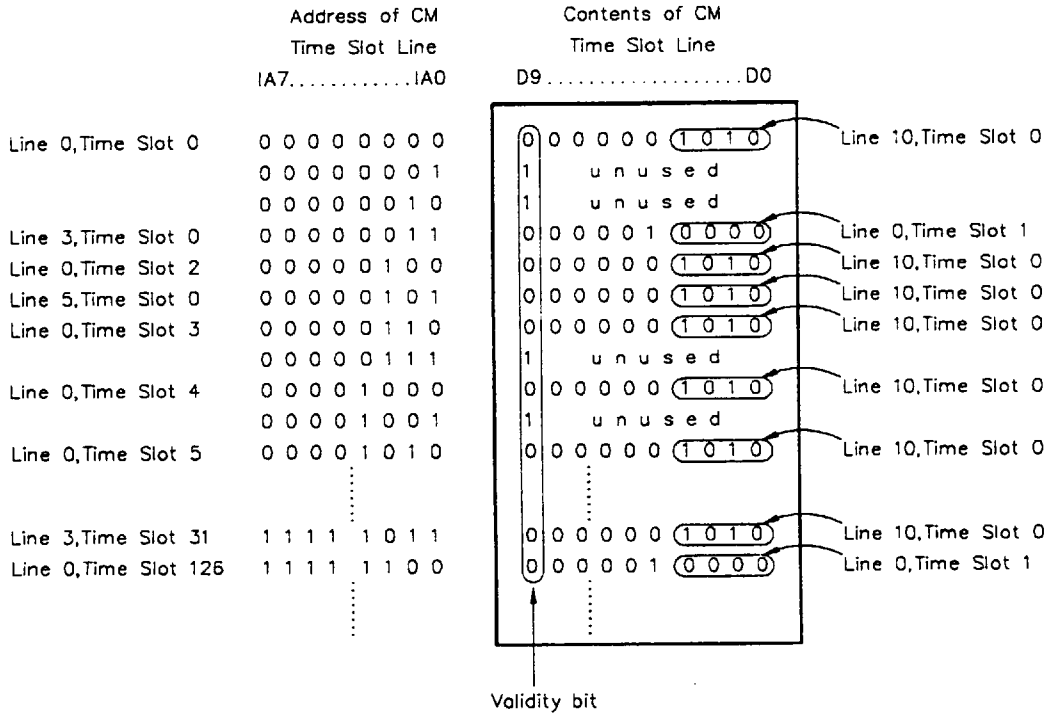
In this application pin names and logical line numbers match.

Figure 6.4: Principle Timing for this Mixed Mode Example



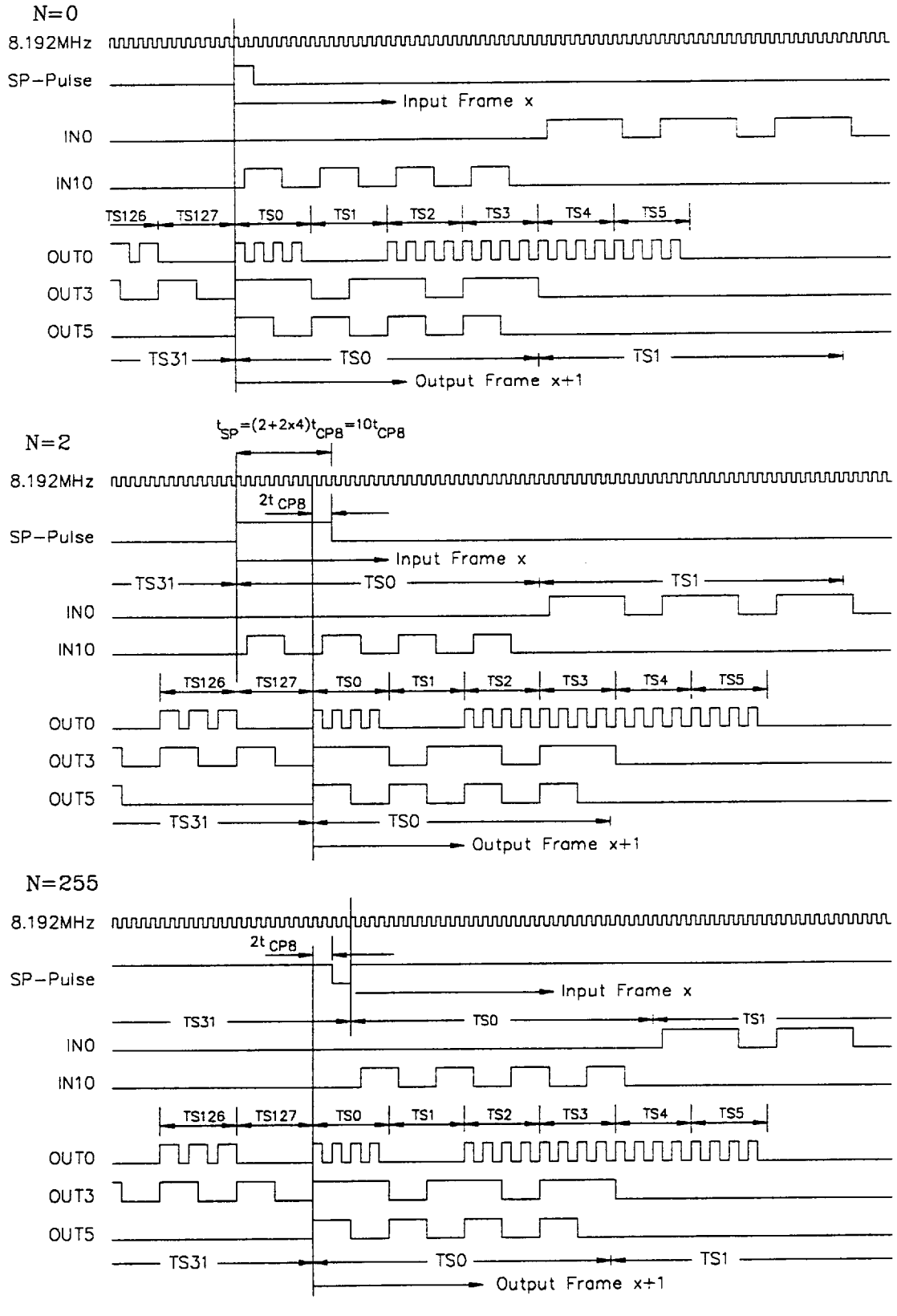
PTIMDIM

Figure 6.5: Connection Memory Content for this Mixed Mode Example



CMCM

Figure 6.6: Timing Diagrams in this Mixed Mode Example for N equalling 0, 2 and 255.



TIMDIM

6.1.3 8192 kbit/s Mode

(MI1=0, MI0=1, MO1=0, MO0=1)

Application

PCM IN:	line 12 time slot 1	connected to	PCM OUT:	line 0 time slot 0 line 1 time slot 127
	line 13 time slot 2	connected to		line 0 time slot 2
	line 14 time slot 0	connected to		line 1 time slot 1

The pin names In 12, 13 and 14 correspond to the logical lines numbers 0, 1 and 2, respectively.

Figure 6.7: Principle Timing Diagram for this 8192 kbps Mode Example

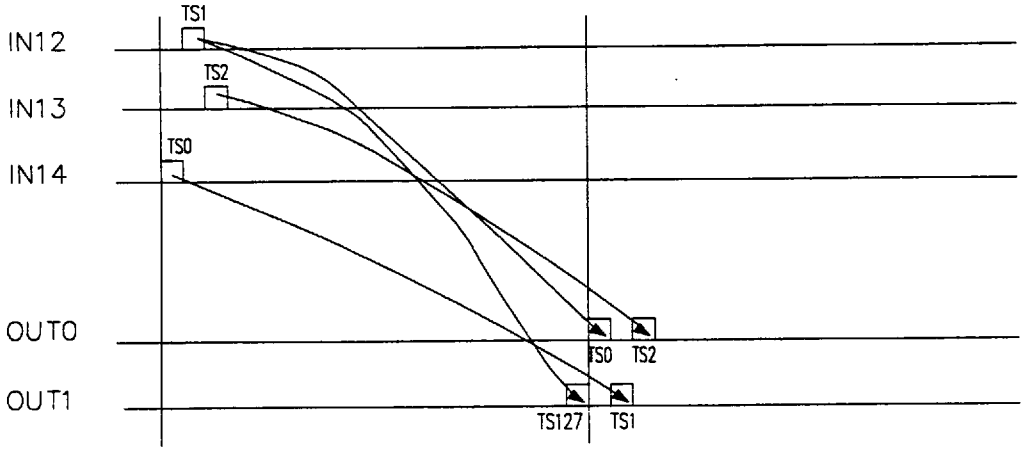


Figure 6.8: Connection Memory Content for this 8192 kbps Mode Example

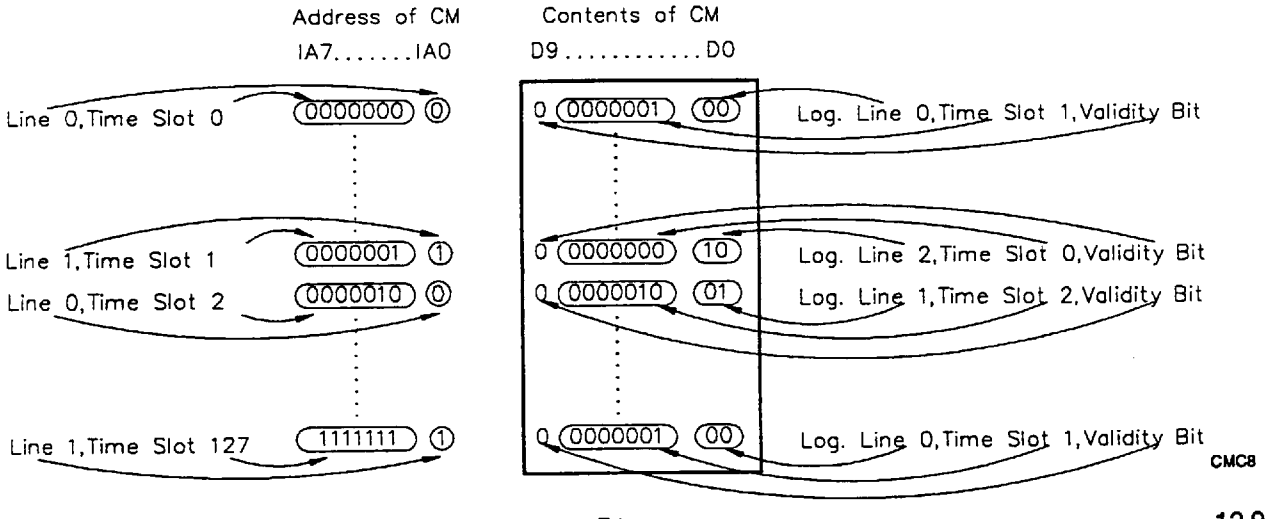
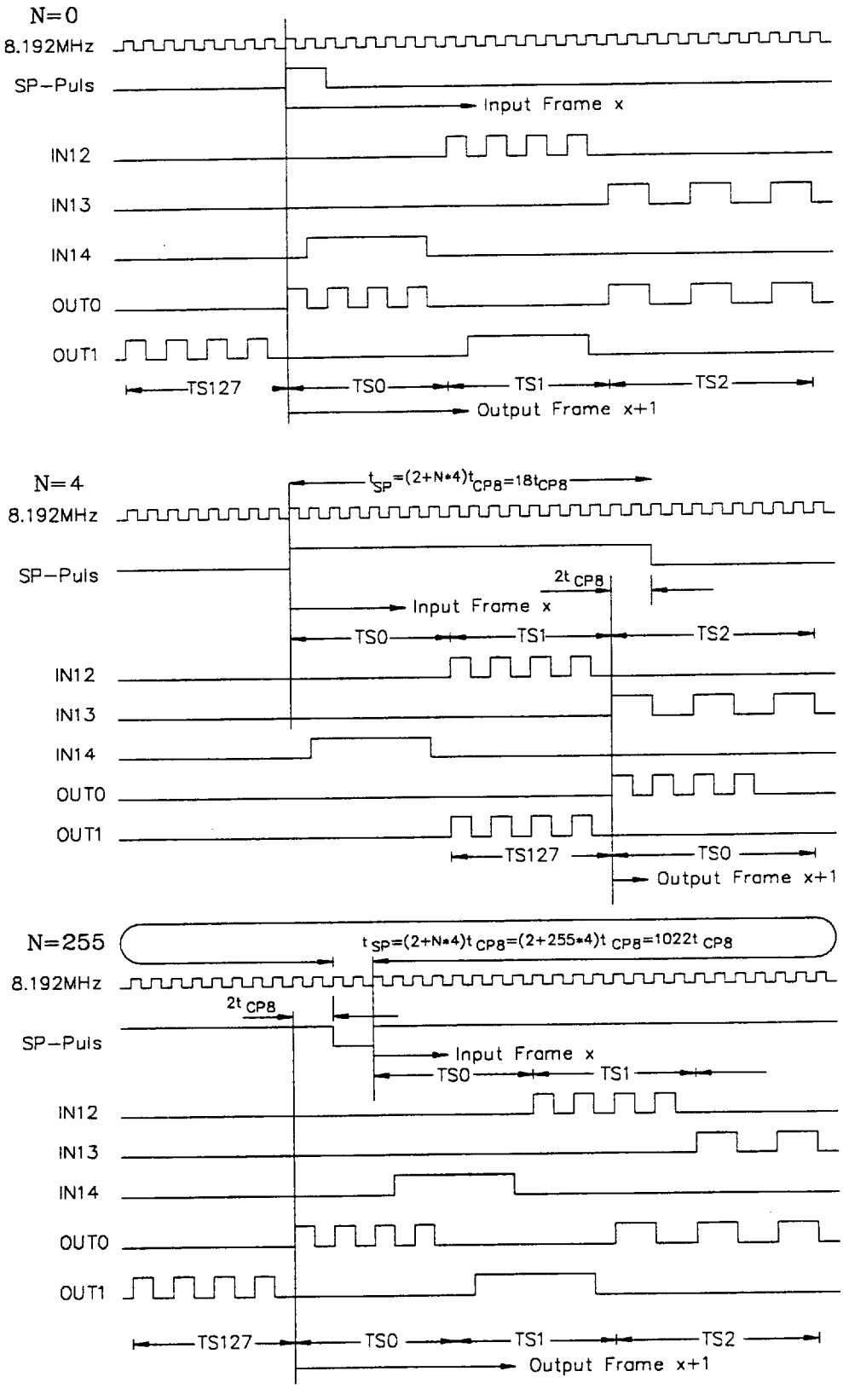


Figure 6.9: Timing Diagrams in this 8192 kbit/s Mode Example for N equalling 0, 4 and 255.



TIMDI8

6.1.4 Space Switch Mode

(MI1=1, MI0=1, MO1=1, MO0=0)

Application

PCM IN	line 12 time slot 126	connected to	PCM OUT:	line 0 time slot 126
	line 12 time slot 0	connected to		line 1 time slot 0
	line 14 time slot 126	connected to		line 1 time slot 126
	line 14 time slot 0	connected to		line 1 time slot 0

The pin names and logical line numbers are identical.

Figure 6.10: Principle Timing Diagram in this Space Switch Mode Example

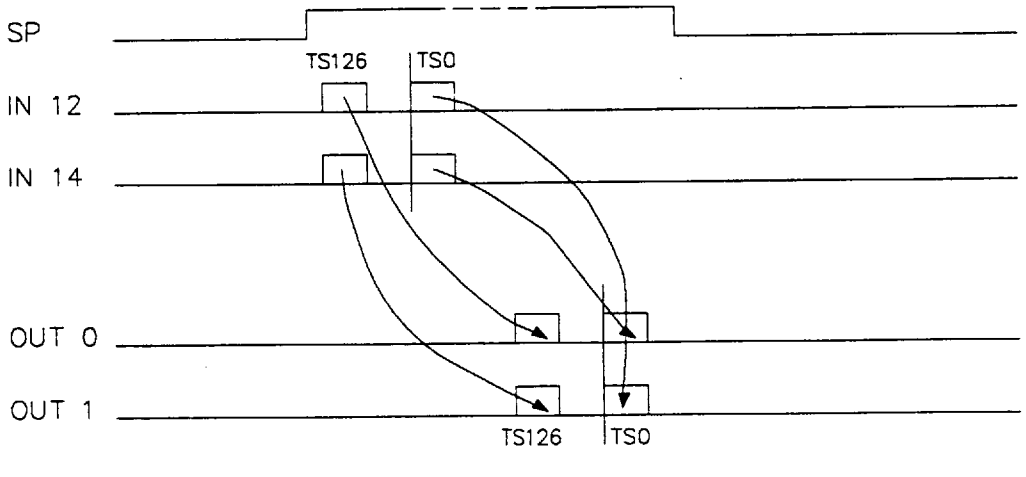


Figure 6.11: Connection Memory Content in this Space Switch Mode Example

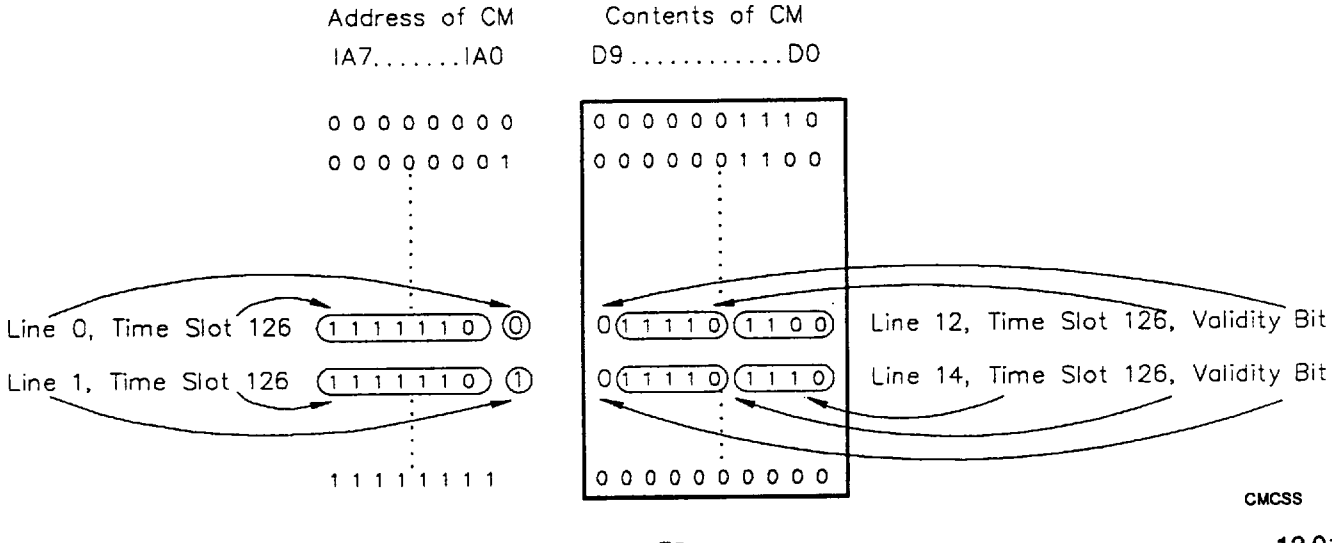
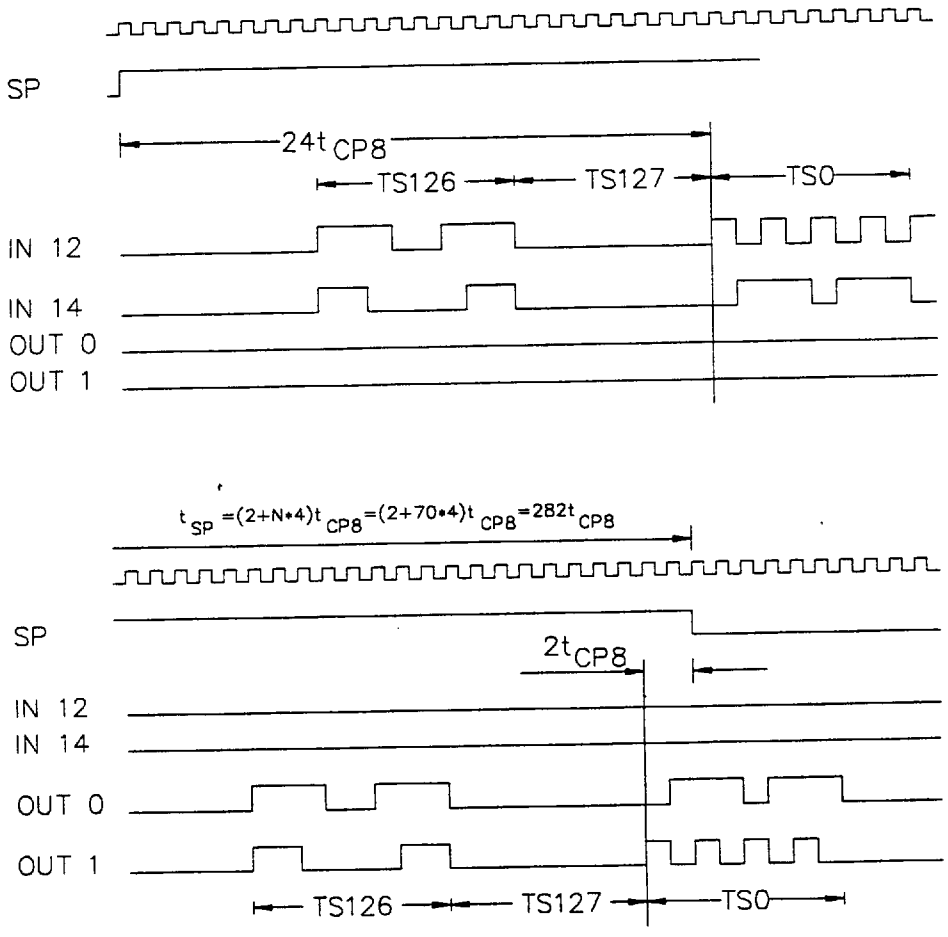


Figure 6.12: Timing Diagram for this Space Switch Mode Example (N=70)



TIMDISS

6.2 Creating Nonblocking Switching Matrix Arrays

If more than 256 subscribers are to be connected without blocking, it is necessary to combine several devices in what is a switching matrix. Without blocking means that it is possible to switch all incoming subscribers simultaneously. For this purpose there must be just as many outgoing time slots as incoming ones.

The switching matrixes are divided up, according to the switching principles spoken of in section G, into space/time switches and space switches. In both application fields single-time-slot connections and broadcast connections are possible. In the latter case one incoming time slot is connected to several outgoing time slots (the reverse is not possible).

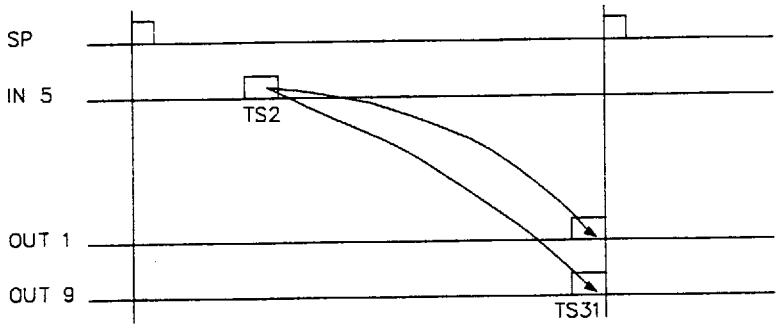
6.2.1 16/16 Space/Time Mode

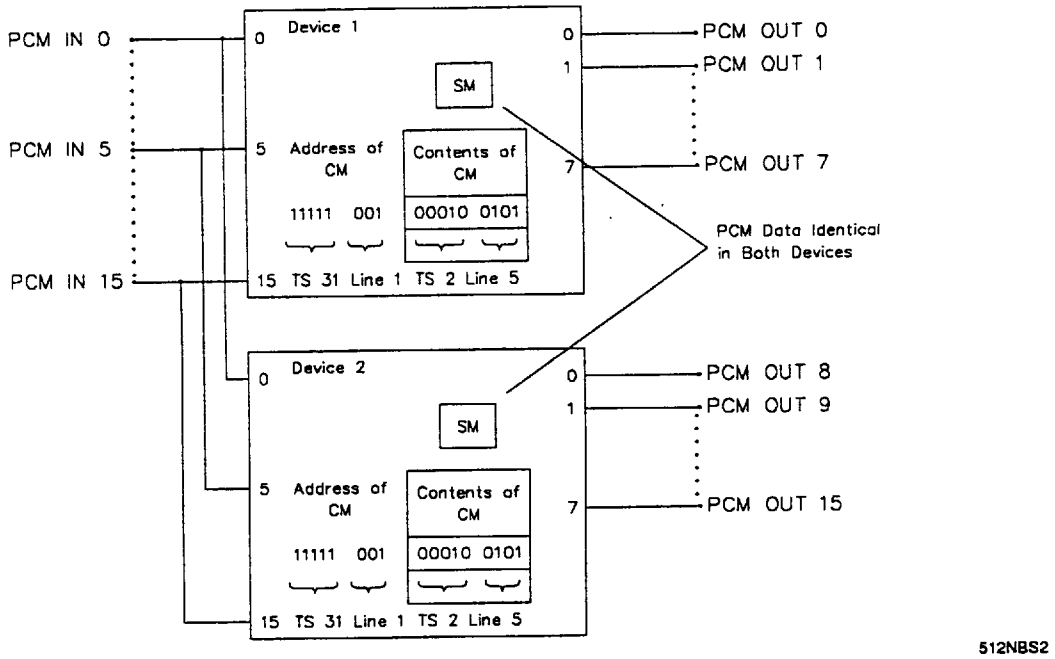
(2048 kbit/s)

By connecting the 16 PCM input lines in parallel to two MTSR's, a nonblocking switching matrix for 512 subscribers can be implemented. An example of such an arrangement is shown in Figure 1.4. There are 16 PCM output lines, PCM OUT 0 through 7 are assigned to device 1 and PCM OUT 8 through 15 to device 2. An incoming subscriber on line 5/time slot 2 is switched to line 1/time slot 31 and to line 9/time slot 31. The required CM entries for such a task are shown in **Figure 6.13**.

In device 2 the 8 output pins, OUT 0 through OUT 7, correspond in the system to PCM OUT 8 through PCM OUT 15. However, in programming device 2 the pins themselves must be referenced. Hence, for example, PCM OUT 9 is programmed as OUT 1.

Figure 6.13: Space-time Switch for 512 Subscribers in a 2048 kbps System





6.2.2 32/32 Space/Time Mode

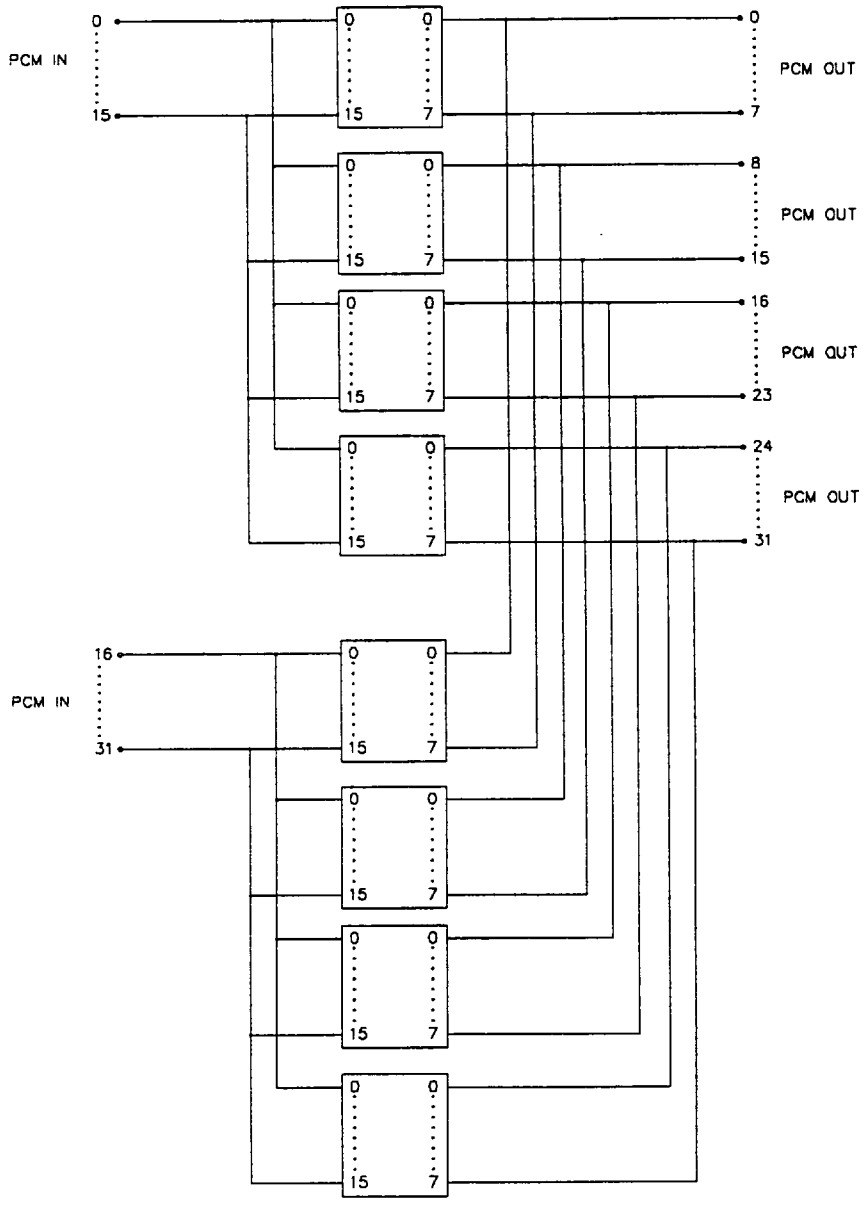
(2048 kbit/s)

A nonblocking switching matrix for 1024 subscribers is implemented with eight devices. A system of this kind is shown in **Figure 6.14**.

Two groups of four devices each are formed. In eachgroup the 16 input lines are connected in parallel. The output lines of the two groups are coupled together. The tristate function enables the output lines to be connected up directly.

Note: If the **STA:TE** = 1 tristate mode is set, line 0/time slot 0 and line 16/time slot 0 cannot be switched, i.e. only 1022 subscribers can be switched.

Figure 6.14: Space-time Switch for 1024 Subscribers in a 2048 kHz System



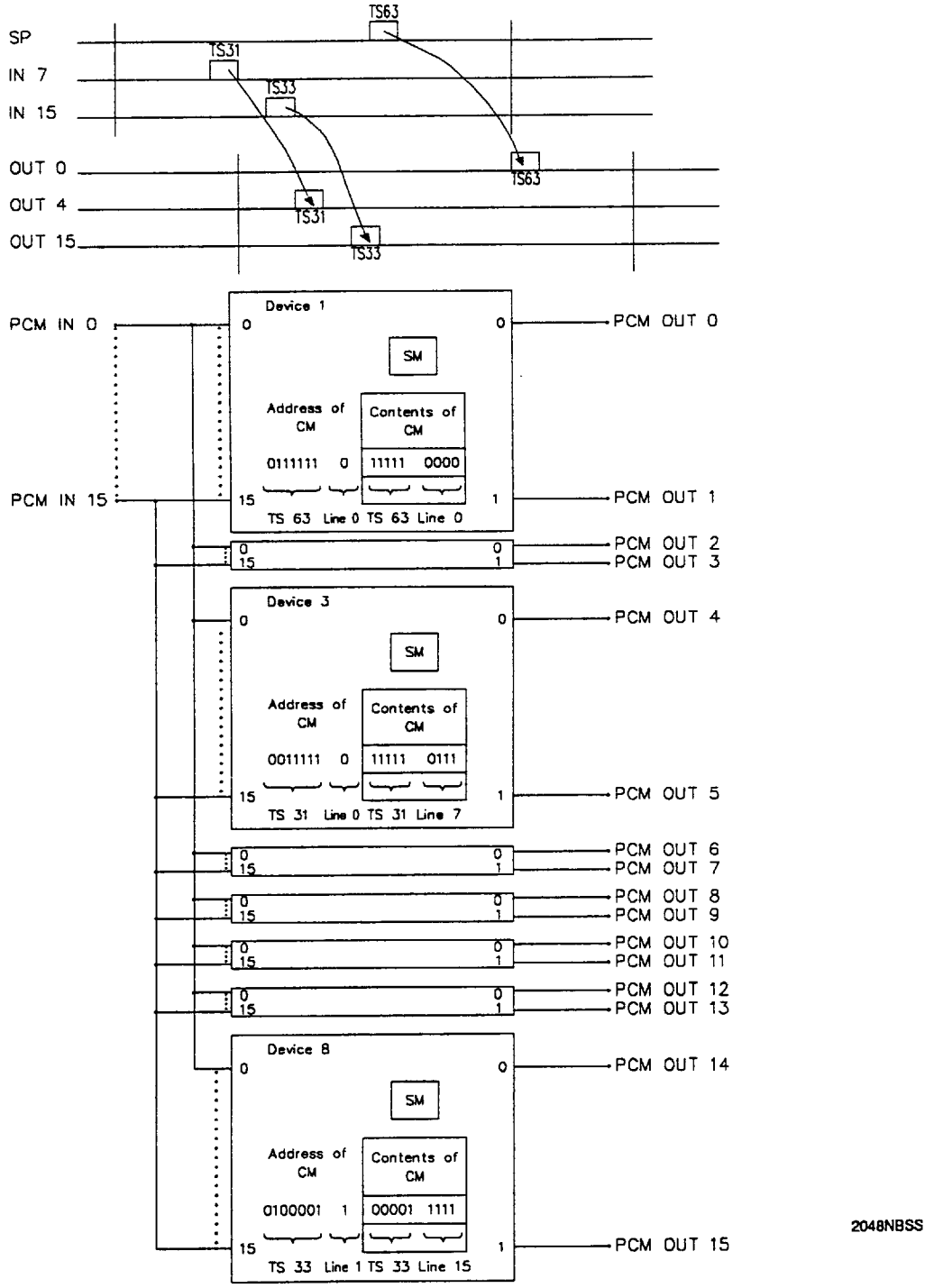
1024NBS2

6.2.3 16/16 Space Mode

(8192 kbit/s)

The space mode with a bit rate of 8192 kbit/s allows for a nonblocking switching matrix for 2048 subscribers with just eight devices. For three subscribers, coming in on the lines 0,7 and 15 and switched to the lines 0, 4 and 15, the associated CM addresses and entries are shown in the devices concerned of **Figure 6.15**.

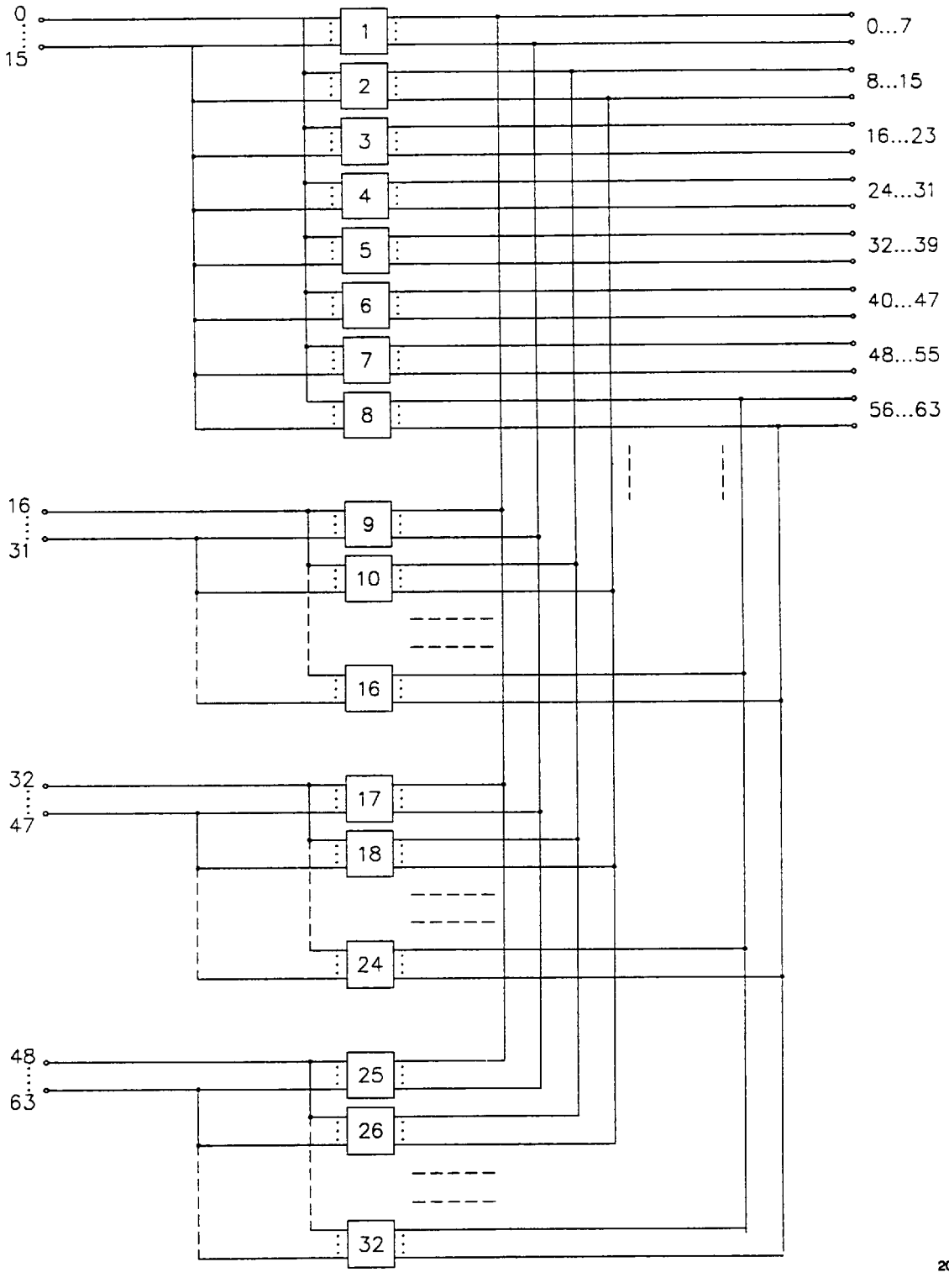
Figure 6.15: Space Mode for 2048 Subscribers (8192 kbit/s)



6.2.4 64/64 Space/Time Mode

(2048 kbit/s)

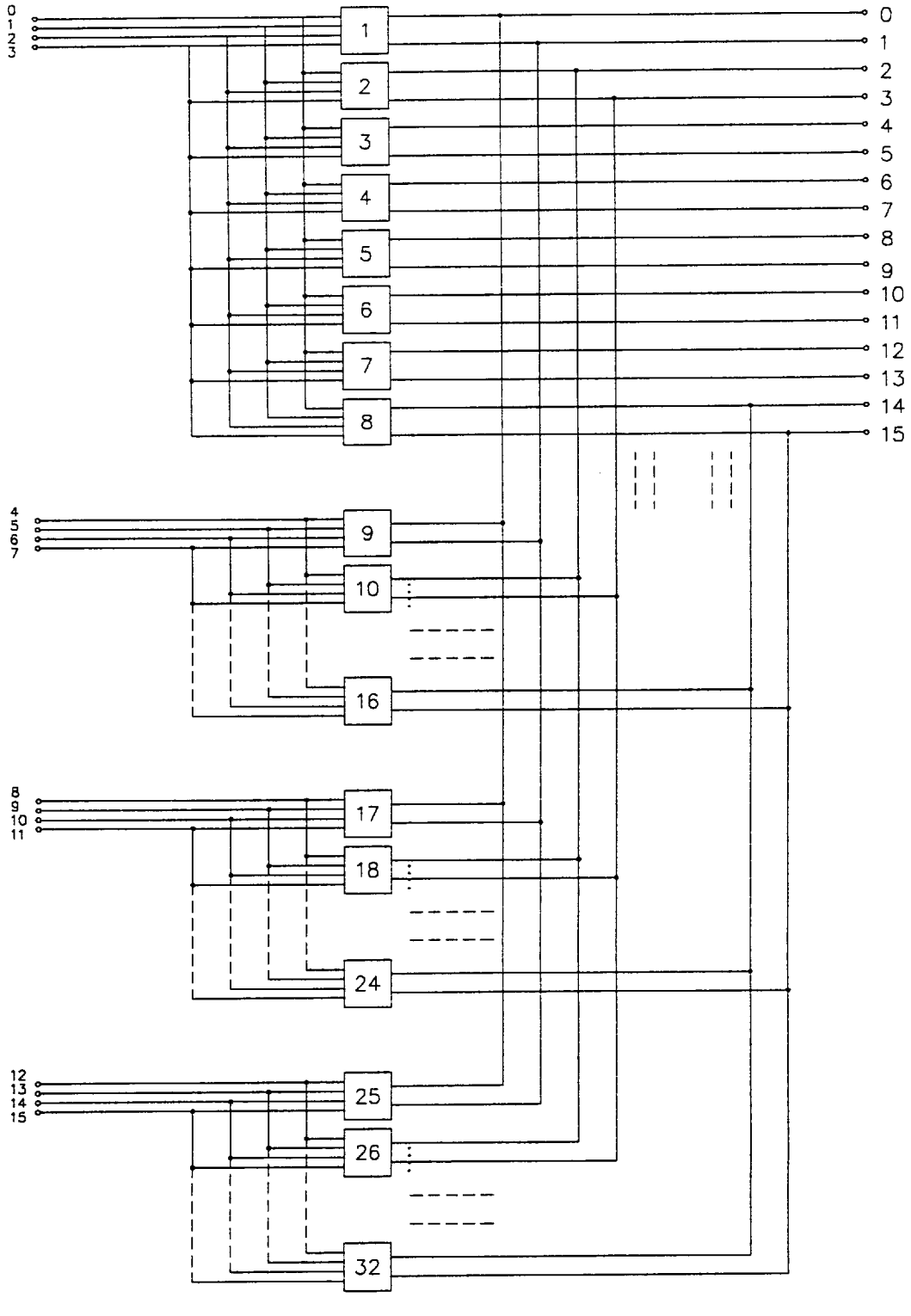
Figure 6.16: Space-time Switch for 2048 Subscribers in a 2048 kHz System



6.2.5 16/16 Space/Time Mode

(8192 kbit/s)

Figure 6.17: Space-time Switch for 2048 Subscribers in a 8192 kHz System

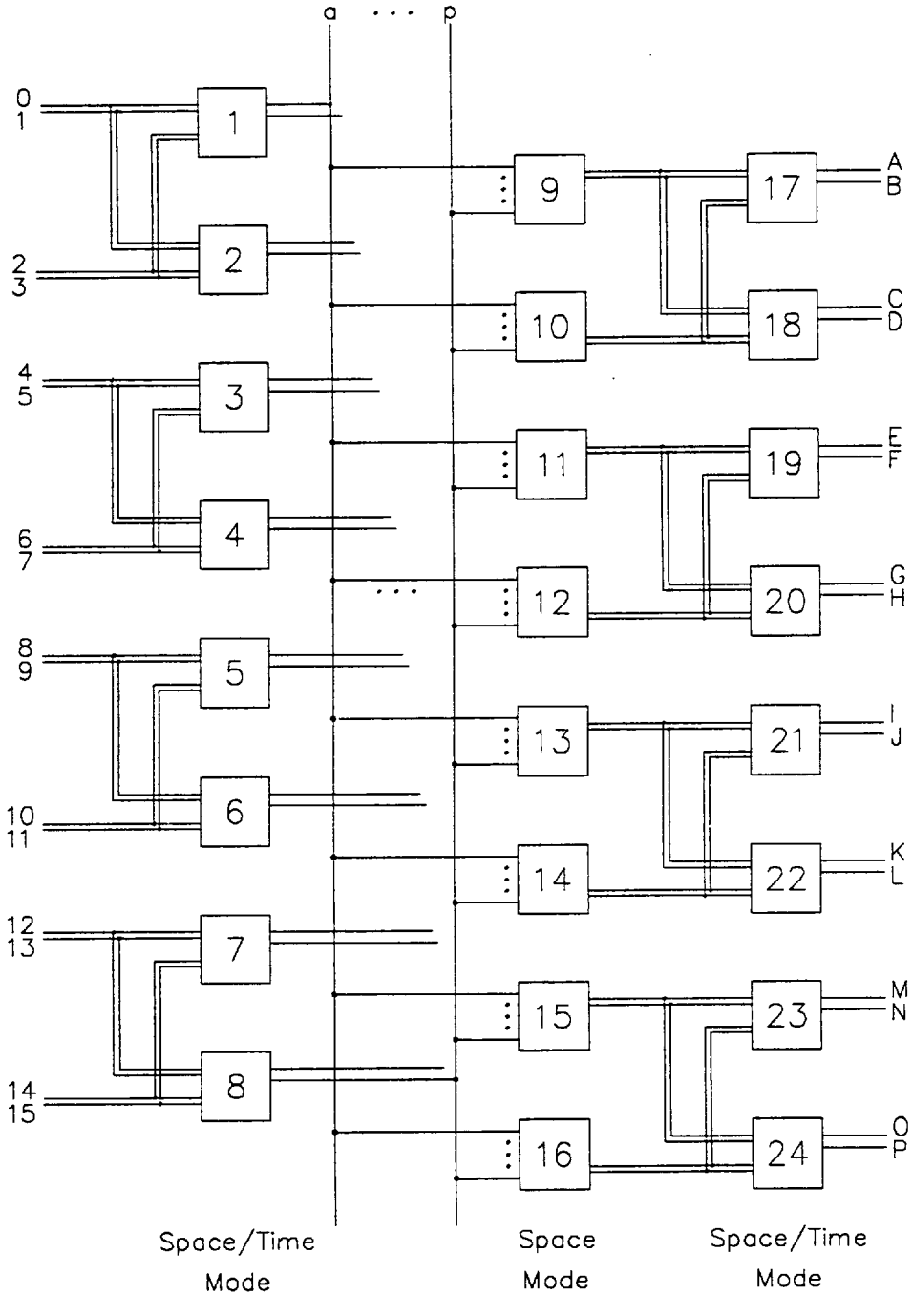


6.2.6 Three Stage Switch for 2048 Subscribers (8192 kbps)

Instead of using 32 MTSRs a non blocking switch for 2048 subscribers can also be built with only 24 devices. This configuration is a three stage switch with an input (devices 1 to 8) and output stage (devices 17 to 24) operating as space/time switch and an space switch stage (devices 9 to 16) in between, as shown in **Figure 6.18.**

The reduced device count of such a solution requires a more sophisticated software solution.

Figure 6.18: Nonblocking Three Stage Switch for 2048 Subscribers



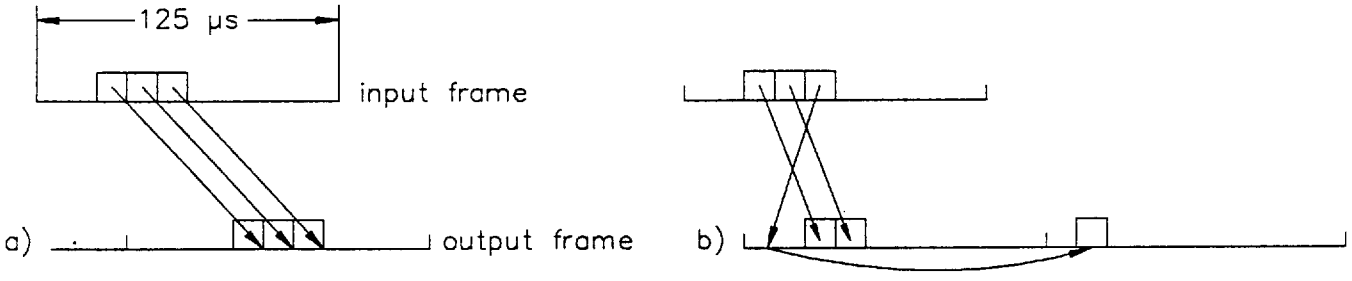
6.3 Minimum and Maximum Delay

6.3.1 Background

An important factor when using the memory time switch PEx 2041 is the delay between incoming and outgoing PCM channels.

Often the question arises whether the incoming channel is transmitted in the same or the next frame. **Figure 6.19** illustrates this problem.

Figure 6.19: Delay of Time Slots



DELTS

In **Figure 6.19a)** the 3 considered time slots are transmitted in the same frame, whereas in **Figure 6.19b)** only the first two of the three incoming PCM channels are transmitted in the same frame. The last incoming time slot is delayed until the next frame.

The considerations of the next paragraphs help to find out which frame an incoming PCM channel will be assigned to.

6.3.2 Evaluation of the Minimum Delay

The device functionality determines the minimum delay.

For a general description the data rate factor DRF is introduced according to **Table 6.1**.

Table 6.1: Data Rate Factor

data rate	data rate factor	possible R value
8192 kbaud	4	0, 1, 2, 3
4096 kbaud	2	0, 1
2048 kbaud	1	0

For any time slot number TS the remainder factor R is given by

$$R = \text{remainder}(TS/DFR) \quad (*)$$

For different systems R can assume the values shown in **Table 6.1**. Subscripts "i" and "o" will be added to differenciate between input and output.

Table 6.2 shows the minimum delay achieveable for a given Ri at a given data rate. Note that it is also dependent on the output line and on wheather the input line is even or odd.

To achieve this minimum delay an optimum shape factor N has to be found. However, N can only be chosen to minimize the delay of one particular connection. It may occur, that other connections will have a minimum delay, too.

Table 6.2: Minimum Delay in 8192 kHz Clock Periods

Input line #	even							odd						
Input [Mbaud]	2	4		8				2	4		8			
Ri	0	0	1	0	1	2	3	0	0	1	0	1	2	3
OUT 0	64	64	48	64	56	48	40	80	80	64	80	72	64	56
OUT 1	60	60	44	60	52	44	36	76	76	60	76	68	60	52
OUT 2	56	56	40	56	48	40	32	72	72	56	72	64	56	48
OUT 3	52	52	36	52	44	36	28	68	68	52	68	60	52	44
OUT 4	48	48	32	48	40	32	24	64	64	48	64	56	48	40
OUT 5	44	44	28	44	36	28	20	60	60	44	60	52	44	36
OUT 6	40	40	24	40	32	24	16	56	56	40	56	48	40	32
OUT 7	36	36	20	36	28	20	12	52	52	36	52	44	36	28

Table 6.3: SP Shape Factor N for Minimum Delay

Input line	even	odd
OUT 0	16	20
OUT 1	15	19
OUT 2	14	18
OUT 3	13	17
OUT 4	12	16
OUT 5	11	15
OUT 6	10	14
OUT 7	9	13

To calculate this N a two step method is used.

- Initially we calculate N for a connection of input time slot R_i to output time slot 0, R_i being derived from the actual input time slot using (*).
- Finally we modify this N to take into account the actual input and output time slot.

The first stage is completed by simply looking at **Table 6.3**. Note that the optimal N is dependent on the output line and on wheather the input line is even or odd. However, it is not dependend on the actual value of R_i.

In the second stage the optimal N for minimum delay (N_{min}) is modified by adding a time slot difference factor (N_{tsd}) to the value obtained from the table (N_{tab}).

$$N_{min} = N_{tsd} + N_{tab}$$

N_{tsd} is calculated from the actual input and output time slots, the input remainder factor and DFR_i and DFR_o

$$N_{tsd} = 8 * [(TS_i - R_i/DFR_i - (TS_o/DFR_o)]$$

6.3.3 Examples for Minimal Delay

The following three examples explain the procedure:

Example 1

In a 2048 kbaud system PCM IN 12, time slot 0 shall be connected to PCM OUT 1 time slot 1 with minimal delay.

In 2048 kbps systems the data rate factor is 1 and hence from (*) R is always 0.

Table 6.3 shows that N_{tab} = 15 in systems with even input lines and output line 1. N_{tab} has to be increased by:

$$N_{tsd} = 8 (TS_i - R_i - TS_o)$$

$$= -8$$

So

$$N_{min} = N_{Table} + N_{tsd} = 7.$$

Table 6.2 states the delay. It is sixty t_{CP8} = 7.32 µs.

Example 2

In an 8192 kbit/sec system the PCM IN 13, time slot7 shall be connected to PCM OUT 1, time slot 98.

The data rate factor is 4 and R is 3. N_{tab} from **Table 6.3** equals 19

$$N_{tsd} = 8 (7 - 3 - 98)/4$$

$$= -188$$

$$N_{min} = N_{tab} + N_{tsd} = -169$$

Since N is periodical with a period of 256 the correct N_{min} = 256 - 169 = 87.

The minimum delay from **Table 6.2** is fifty two t_{CP8} = 6.35 µs.

Example 3

Time slot 38 of PCM IN 14 of a 8192 kbps system shall be connected to time slot 25, OUT 6 of a 2048 kbps system.

The rest of input time slot 38 is 2, the input data rate factor is 4, the output data rate factor is 1. Ntab from **Table 6.3** equals 10.

N_{tsd} = 8 ((38 - 2)/4 - 25)=

= -128

N_{min} = -128+ 10=-118 =^ 138

The minimum delay is twenty four t_{CP8} = 2.93 µs.

6.3.4 Evaluation of the Maximum Delay

Similar considerations apply to the determination of the maximum delay.

To achieve the maximum delay the shape factor Nmin has to be decreased by 1.

N_{max} = N_{min} - 1

The according maximum delay is one thousand and twenty t_{CP8} longer than the minimum delay.

6.3.5 Examples for Maximum Delay

For the three examples of **paragraph 6.3.3**. the pulse shaping factor N_{max} and the appropriate maximum delay would be:

Example 1: N_{max} = 6; t_{max} = 131.9 µs;

Example 2: N_{max} = 86; t_{max} = 130.9 µs;

Example 3: N_{max} = 137; t_{max}= 127.4 µs;

6.4 Operation in 1536/1544 kbps Systems

The main applications of the PEx 2041 are in systems with a bit rate of 2048, 4096 or 8192 kbps. However, it also operates in systems with other bit rates, e.g. 1536 or 1544 kbps (T1).

To program the connection memory correctly in T1 applications, naming conventions different form those known from T1 have to be used. The T1 time slot numbers have to be decreased by one. The lowest time slot number is time slot 0, the highest time slot number 23.

The SP pulse has to be applied in every frame. In standard configuration the rising edge of the SP pulse has to be applied with the beginning of time slot 0. The falling edge follows according to section 2.

The operation mode **MOD:MI1,MI0,MO1,MO0** = 0_H is recommended. Using mixed modes will result in output data rates which are not standard.

To reset the connection memory **MOD:RC** has to be reset for at least 1 frame (125 µs). It must be set to logical 1 again with a seperate instruction. In this application **MOD:RC** is not set automaticly by the PEx 2041 after the connection memory reset has been completed.

Alternately all interesting CM locations may be written with an appropriate value by a software routine (e.g. 200H for D9 ... D0 in the CM programming sequence).

The following paragraphs state the exact behaviour of the device in 1536/1544 kbps applications.

6.4.1 Operation in 1536 kbps Systems

1536 kbps correspond to T1 systems without a framing bit. The PEx 2041 can handle this data rate if a 6144 kHz clock is provided at the CLK pin.

The restrictions applying to 1536 kbps systems are:

- input time slot 23 has to be programmed as time slot 31 for the odd input lines.
- output time slot 0 has to be programmed as time slot 24.
- output time slot 1 has to be programmed as time slot 25 for the output line 0.

6.4.2 Operation in 1544 kbp (T1) Systems

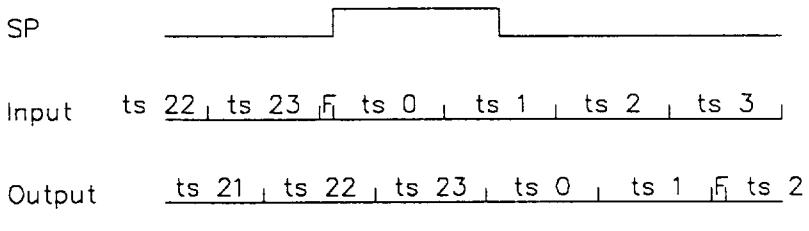
1544 kbps systems consist of 24 time slots plus 1 framing bit. The clock frequency has to be adjusted to 6172 kHz.

The restrictions applying to this mode are:

- the input framing bit can not be switched.
- input time slot 23 for the odd input lines has to be programmed as time slot 31.
- output time slot 0 has to be programmed as time slot 24.
- output time slot 1 has to be programmed as time slot 25 for output line 0.
- output line 7, time slot 1 cannot be used for switching.

As for the input there also exits a spare bit in the output time slot sequence. The position of it is shown in **Figure 6.20**. It is located between output time slot 1 and 2.

Figure 6.20



OPERINT1

6.5 Adapting the Output AC Characteristics to a C_L Different from 150 pF

The output DC Characteristics (t_{RD}, t_D and t_T) change for reference load capacitanes different from 150 pF according to below formula.

$$t(C_L)[ns] = t_{Spec}[ns] + (C_L[pF]/15) - 10$$